Utilizing Reverse Short Channel Effect for Optimal Subthreshold Circuit Design

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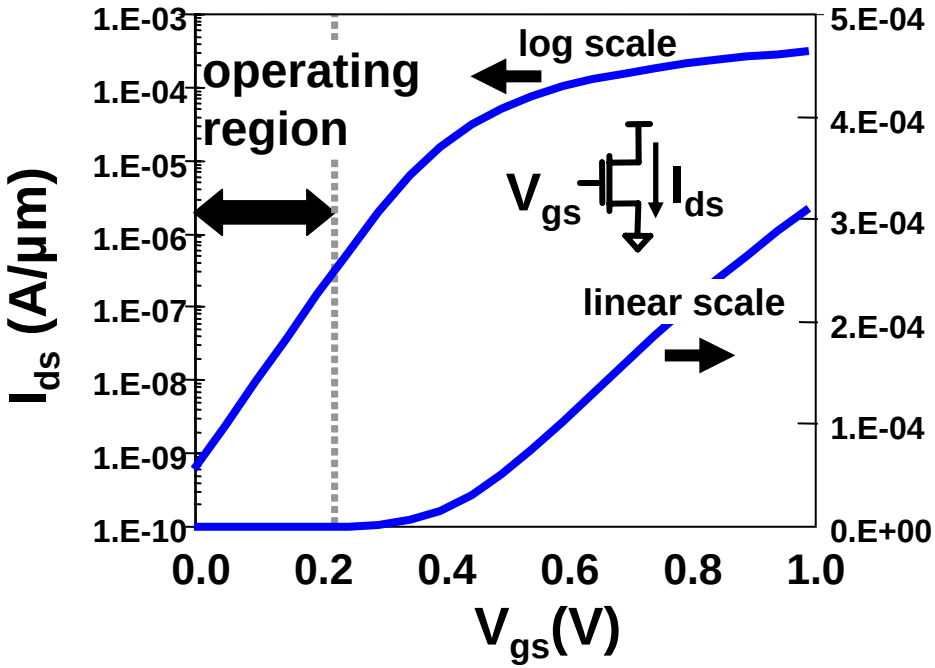
Outline

- Subthreshold Operation
- HALO Impact in Subthreshold Region
- Proposed Transistor Sizing Considering RSCE
  - Optimal Channel Length for Maximum Current
  - Optimal Channel Length for Minimum Capacitance
  - Process Variation Tolerance
  - Subthreshold Swing & I_{on}-to-I_{off} Ratio
- Test Chip Measurement Results
- Conclusions

Subthreshold Operation

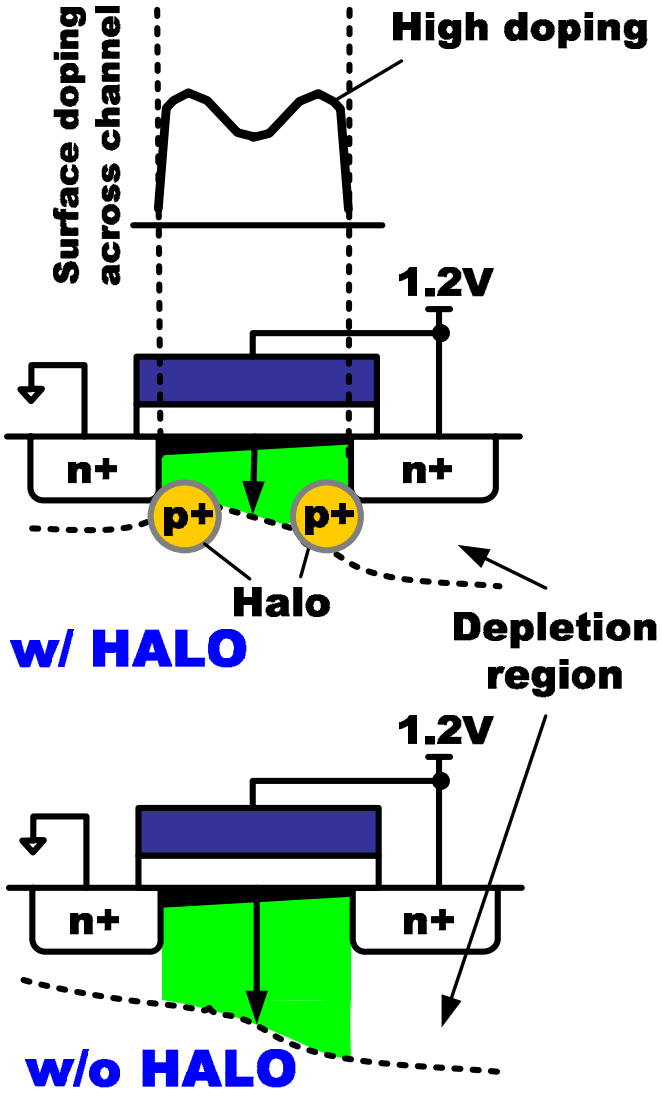


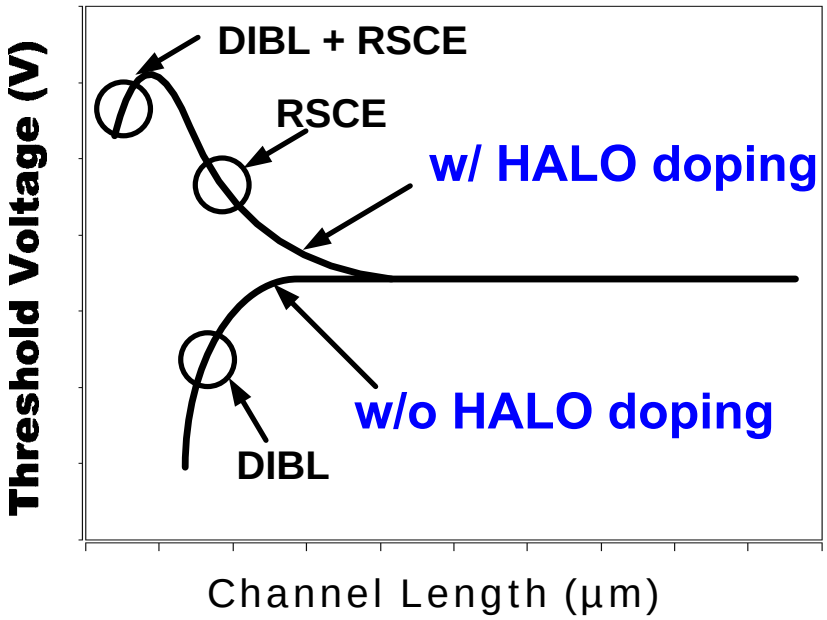
- **Main Benefit**
  - Super-linear power savings

$$P_{total} = \alpha \cdot f \cdot C \cdot V_{dd}^{2} + I_{leak} \cdot V_{dd}$$

  - Minimum energy solution for low-performance designs
- **Limitations**
  - PVT variation
  - Interconnect delay
  - Lack of a systematic design methodology

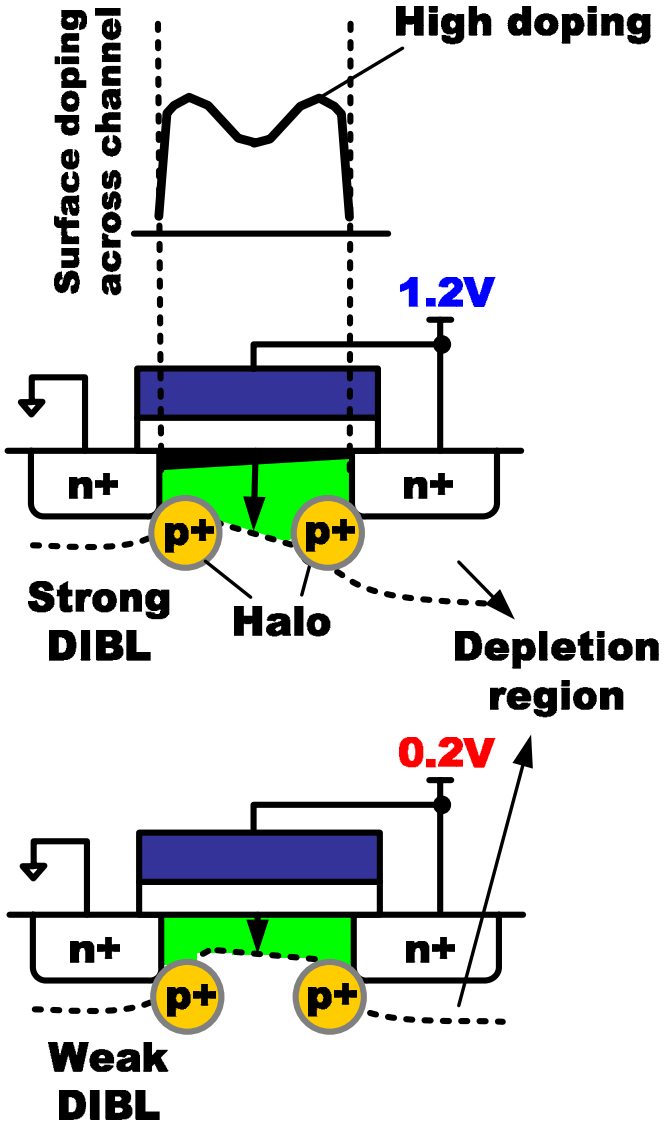
HALO Impact in Superthreshold

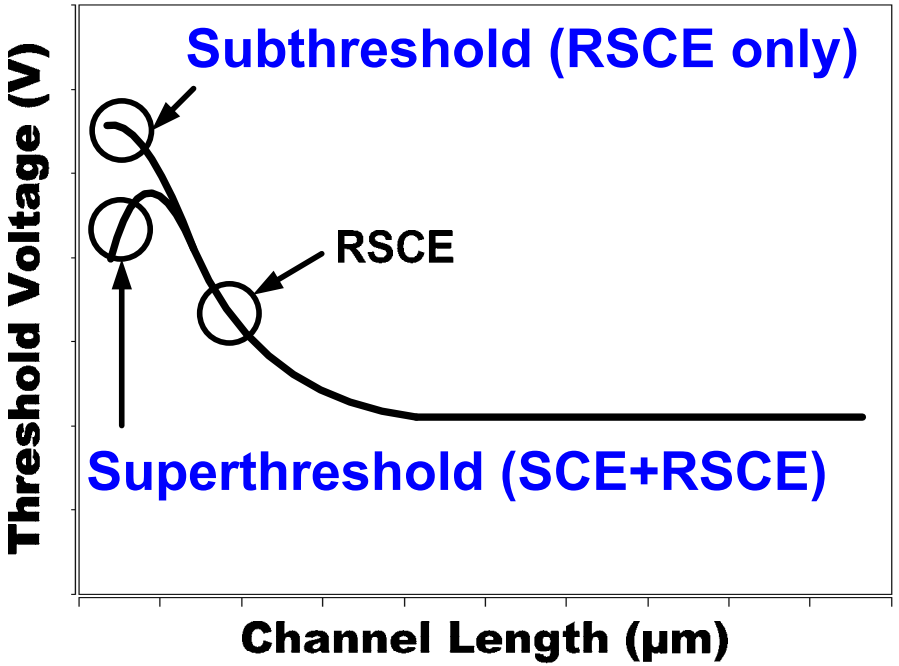




- HALO pocket implants used to mitigate the Short Channel Effect (SCE)
- Reverse Short Channel Effect (RSCE) observed due to HALO

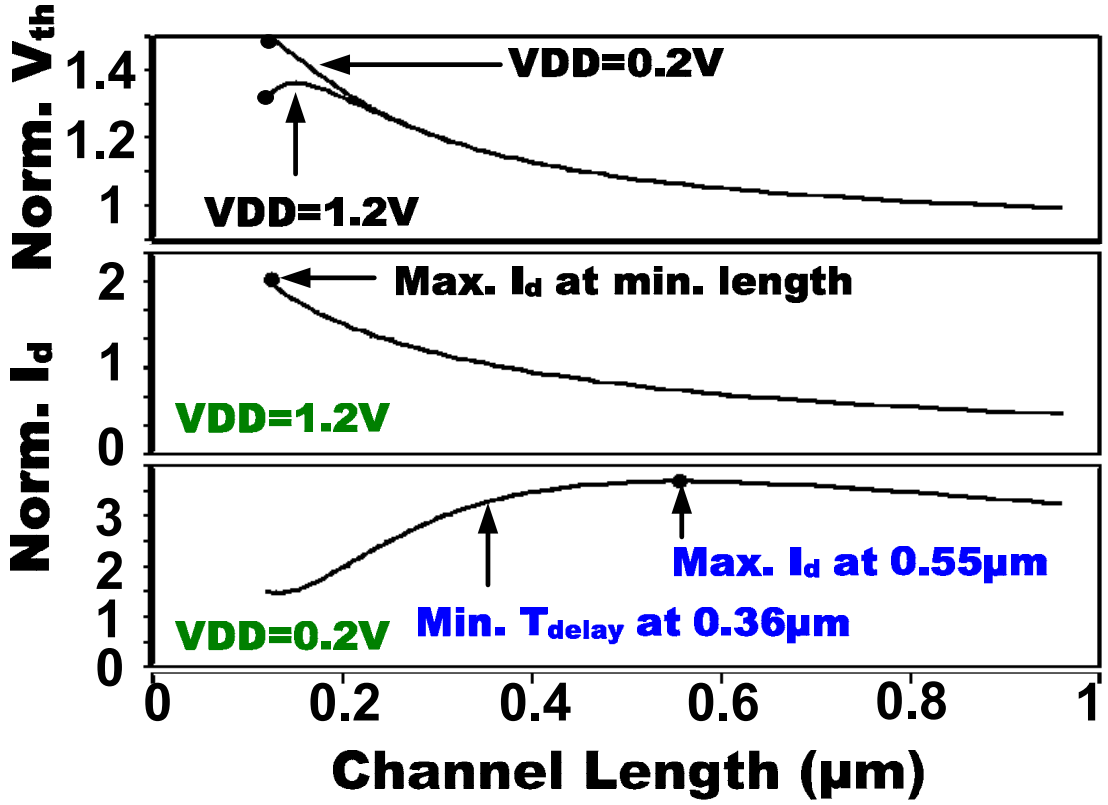
HALO Impact in Subthreshold





- SCE significantly reduced in the subthreshold region
- Only the RSCE is observed in subthreshold

Proposed TR Sizing Considering RSCE



- RSCE and the exponentially increasing current with a lower V_{th} results in
  - L_{opt}=0.55µm for max. drain current
  - L_{opt}=0.36µm for max. performance

Derivation of Optimal Channel Length

- **RSCE-affected V_{th}:** $V_{th} = V_{th0} + K_1\left(\sqrt{1+\frac{K_2}{L_{opt}}}-1\right)\sqrt{\Phi_S}$

- **Current in subthreshold operation:**

$$I_D = I_{D0}\frac{W}{L_{eff}} e^{\frac{V_{GS}-V_{th}}{mV_t}}\left(1-e^{\frac{-V_{DS}}{V_t}}\right)$$

- **Derivative of current:**

$$\frac{\partial I_D}{\partial L_{eff}} = 0 \quad , \quad L_{opt}^{\ 2} + K_2 L_{opt} + K_3 = 0$$

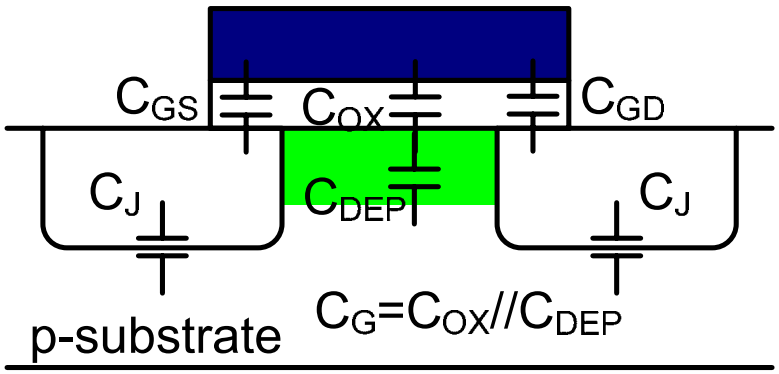
- **Optimal channel length:**

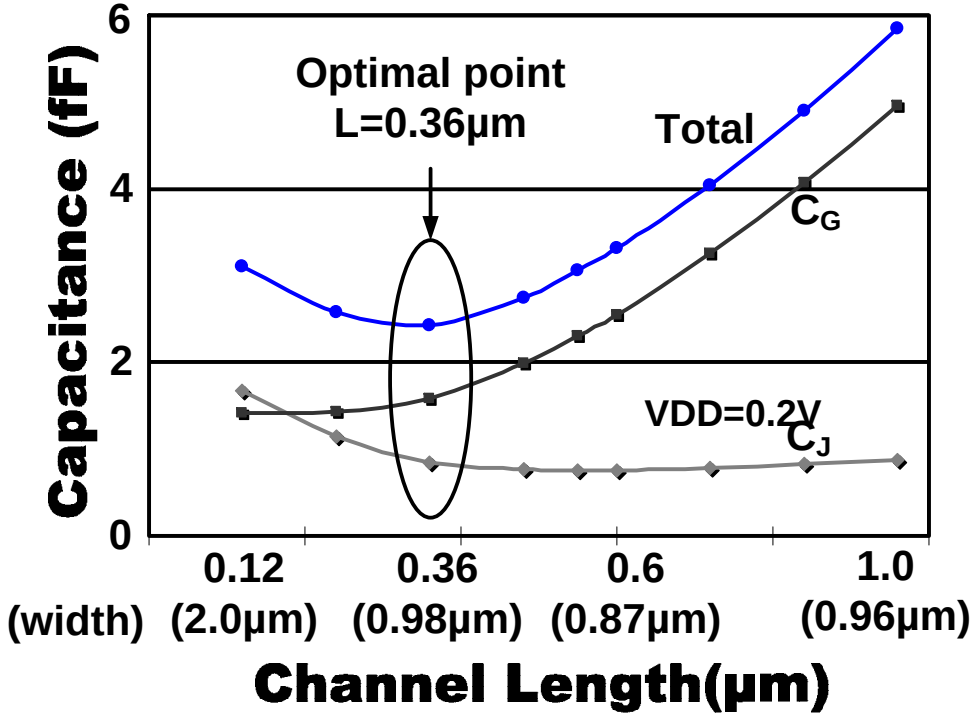
V_{th0} : *zero-bias threshold voltage*
K_1, K_2, m : *technology parameters*
L_{eff} : *effective channel length*
Φ_S : *surface potential*
V_t : *thermal voltage*

$$L_{opt} = \frac{-K_2 + \sqrt{K_2^{\ 2} - 4K_3}}{2} \quad , \quad K_3 = -\frac{K_1^{\ 2}\Phi_S}{m^2 V_t^{\ 2}} K_2$$

Closed form solution for optimal channel length (fixed device width)

Optimal Channel Length for Min. Cap.

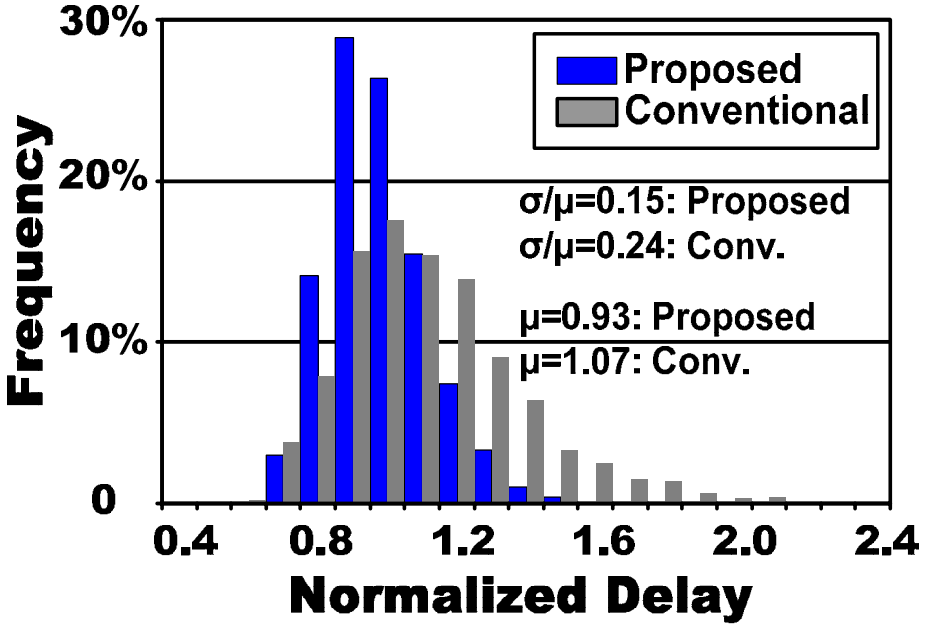


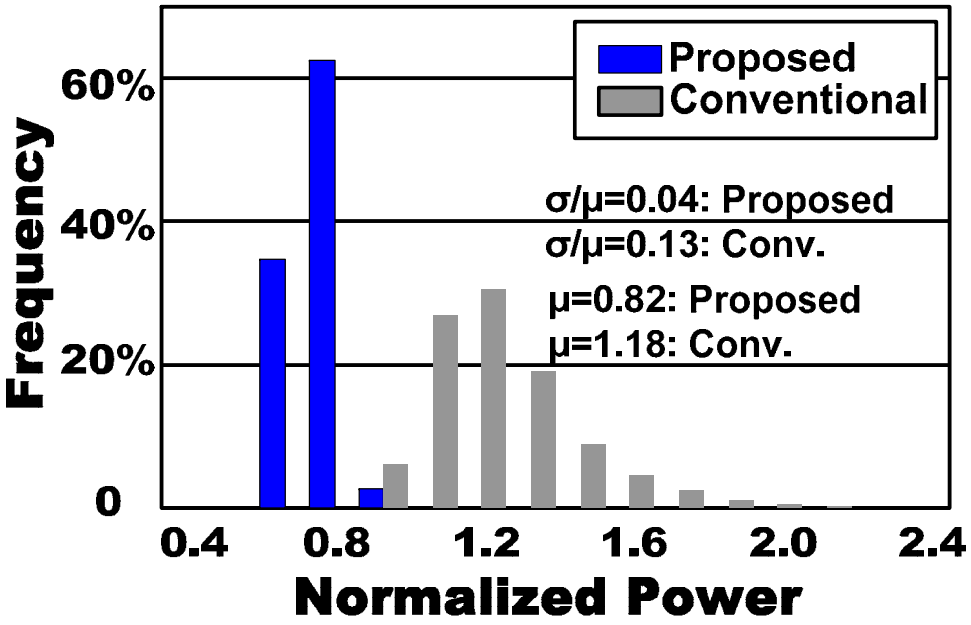


- Moderate increase in C_G due to depletion capacitance
- Significant reduction in C_J due to smaller width
- Net effect: minimum capacitance at longer channel length

Process Variation Tolerance

- Increased transistor gate area with optimal sizing reduces the impact of random dopant fluctuation
- Delay variation (σ/μ) reduces from 0.24 to 0.15
- 30% average power reduction due to reduced junction capacitance



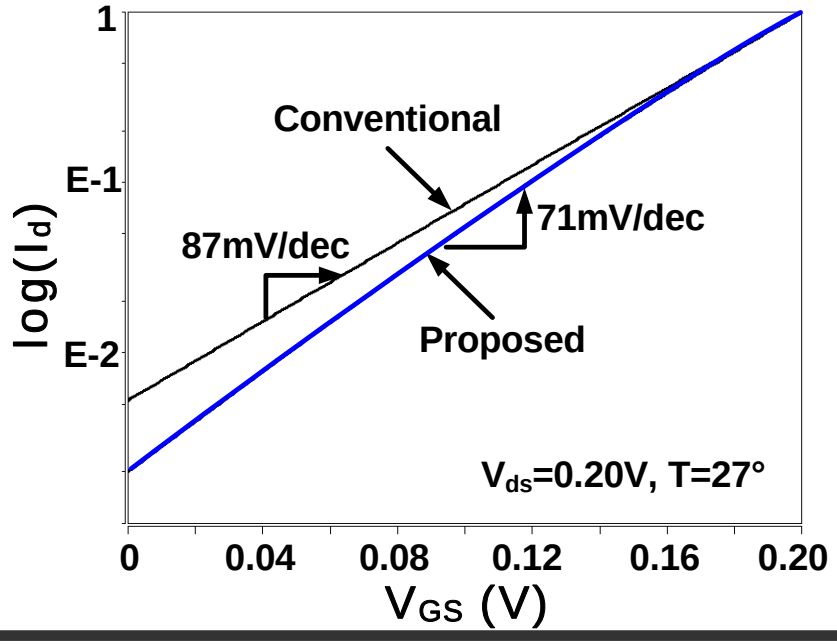


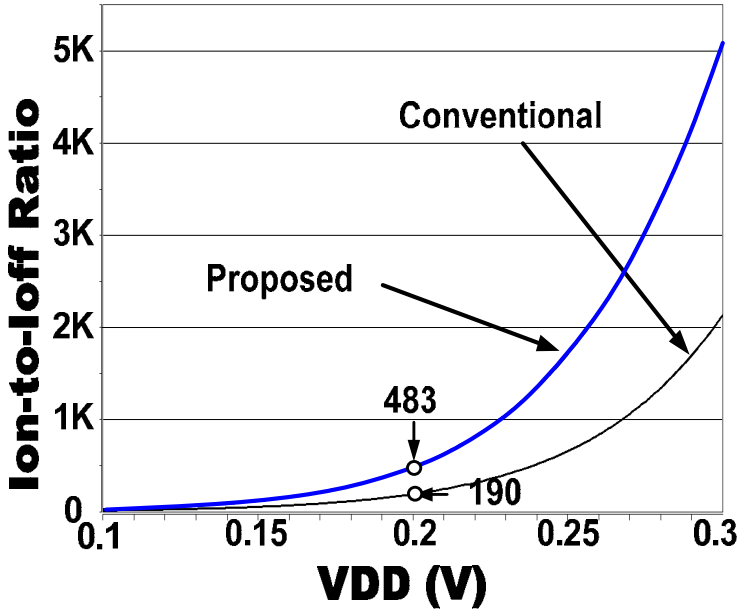
Subthreshold Swing & I_{on}-to-I_{off} Ratio

- **71mV/dec subthreshold swing due to decreased depletion capacitance at optimal channel length**
- **I_{on}-to-I_{off} ratio improves from 190 to 483 at 0.2V**

$$S = m\frac{kT}{q}\ln 10 \quad (mV/dec), \text{ where } m = 1 + \frac{C_{DEP}}{C_{OX}}, \quad C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}, \quad C_{DEP} = \frac{\varepsilon_{si}}{W_{DEP}}$$

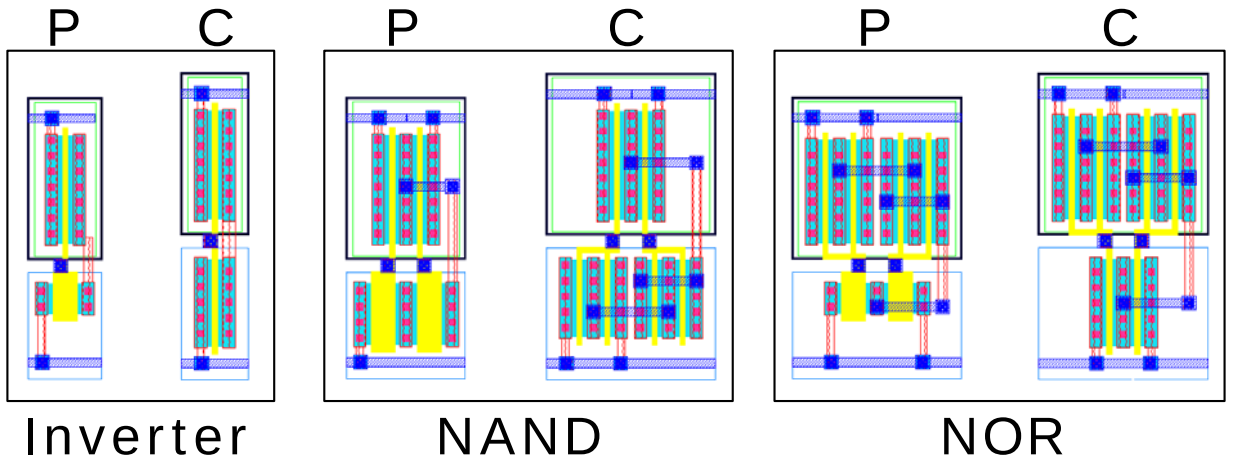
C_{DEP} : depletion capacitance
C_{OX} : oxide capacitance
W_{DEP}: depletion width

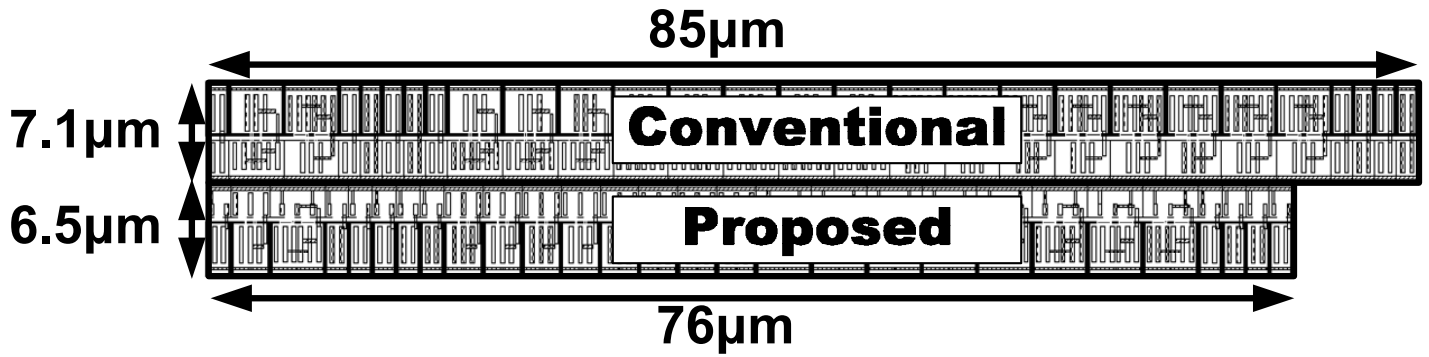




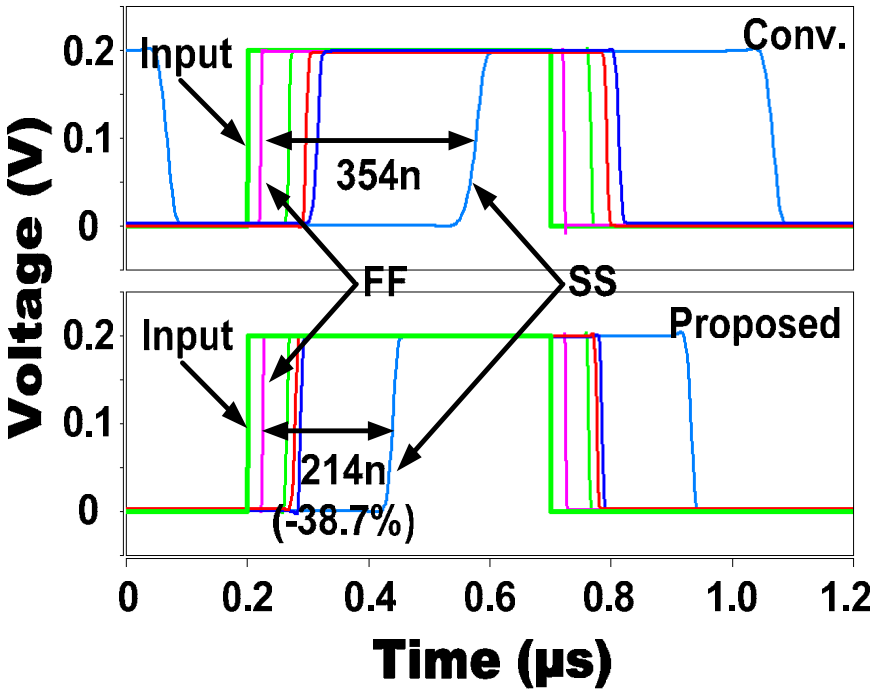
Layout Comparison

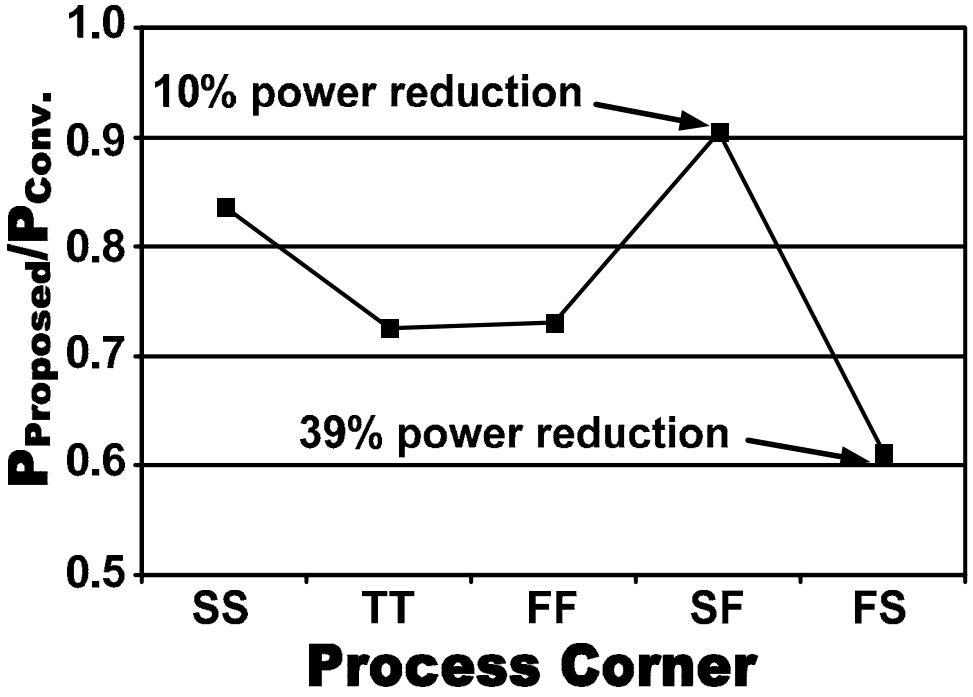
- **Smaller layout area and junction capacitance**
- **'Fat' transistors with longer L and smaller W**





Delay and Power Simulation Results





- 38.7% reduction in delay variation for corner parameters
- 10-39% reduction in power consumption due to reduced junction capacitance

ISCAS Benchmark Simulations

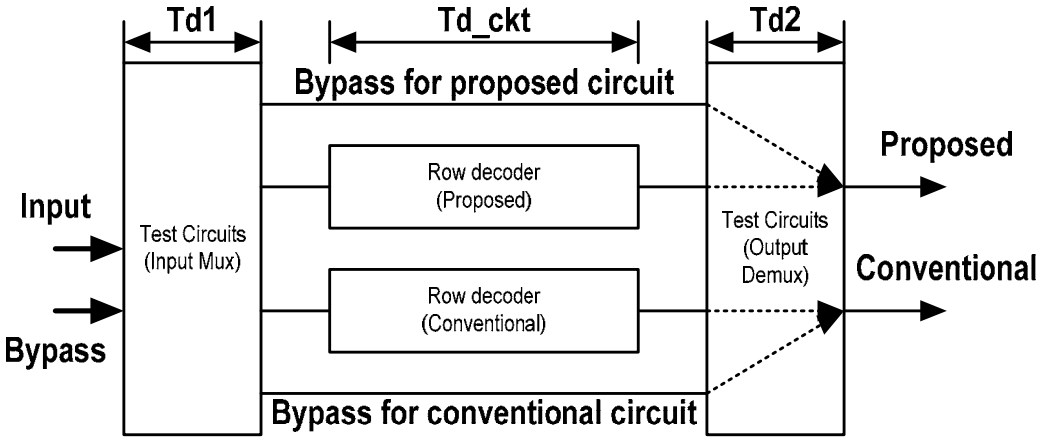
- Two sets of libraries for delay and power comparison
- 7.8-10.4% reduction in delay due to reduced junction capacitance
- 8.4-34.4% power savings due to reduced junction capacitance

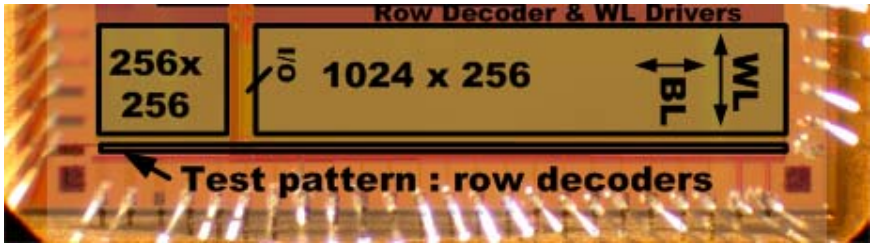
Circuit	0.2V, Temp=27°		
	Conv. (ns)	Proposed (ns)	Improve-ment
C6288	119	107	10.1 %
C1355	443	397	10.4 %
74283	231	207	10.4 %
74L85	121	110	9.1 %
74182	103	95	7.8 %

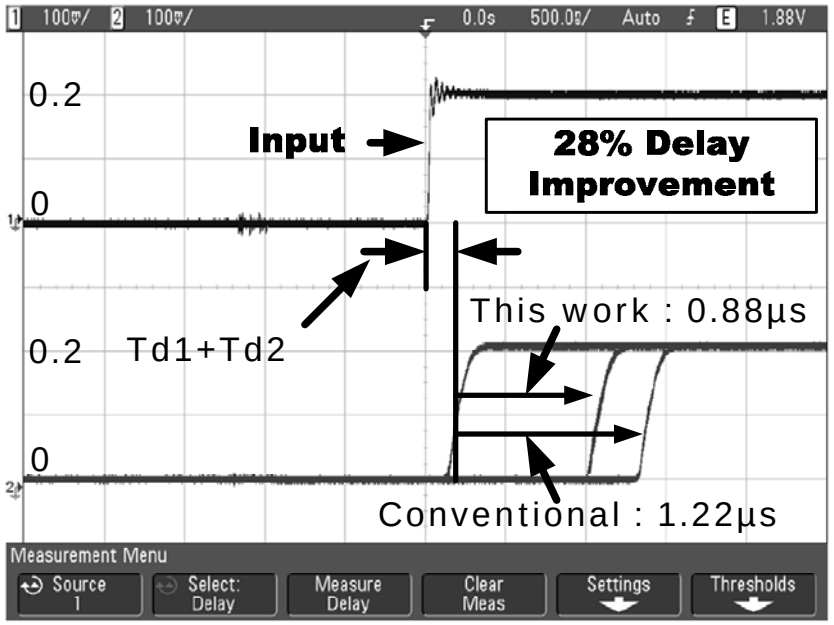
Circuit	0.2V, Temp=27°		
	Conv. (µW)	Proposed (µW)	Improve-ment
C6288	2.24	1.50	33.0 %
C1355	0.64	0.42	34.4 %
74283	1.60	0.14	13.8 %
74L85	0.38	0.26	31.6 %
74182	0.40	0.38	8.4 %

Test Chip Measurements

- 0.2V SRAM row decoder path
- Differential delay measurement
- 28% measured delay improvement







Conclusions

- **RSCE opportunistically utilized for subthreshold circuits**
- **Reduced V_{th} at longer channel length increases operating current due to exponential behavior**
- **Junction capacitance reduced by using a smaller device width for the same current drivability**
- **Proposed transistor sizing scheme achieves**
  - **7.8~28% delay improvement**
  - **8.4~34.4% power savings**
  - **38.7% less delay variation**
- **0.13µm test chip confirms the benefits**