Electromigration Test Chip Experiment From Realistic Power Grid Structures: Failure Trend Comparison and Statistical Analysis


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Purpose

• Study electromigration (EM) aging behavior in realistic power grid structures
• Monitor IR drop aggravation from EM-induced void growth in power grids
• Analyze layout-dependent time-to-failure (TTF) and failure locations
Outline

• Motivation and 28nm Power Grid EM Test Chip Overview
• Experiment Flow and Measurement Methodology
• EM Failure Data and Analysis
• Conclusion
EM Measurement in Realistic Power Grids

- Realistic power grid EM silicon data measurement and analysis
- Special test-chip design is required for the EM experiment
  - High EM stress current and extreme temperature conditions


Slide 4
28nm Power Grid EM Test Chip Overview

- CMOS logic cells are replaced by equivalent resistive loads
- Voltage scanning circuits for monitoring the power delivery
- On-chip heaters and DUT temperature sensor
Four Different Layouts

- Four DUTs with different cell via counts, rail widths, and rail densities are implemented to compare EM failure behaviors.
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Accurate Temperature Control with On-chip Heaters

- Heater elevates the DUT temperature
- Measurement is done only if the temperature is stable
Time to Failure and Failure Location Analysis

- TTF criterion: 5% DUT resistance shift
- Earlier voltage shifts in VSS nodes
Measured Supply Voltage Maps

DUT2 fresh chip cell voltages

After EM stress

- 488 cell VDD and VSS values are monitored
- VDD and VSS values gradually increase
  - Excessive IR drop in VSS net

1.2V constant voltage stress, 350°C DUT
• IR drop is aggravated after the EM stress

Voltage Shift After EM Stress

DUT2, 1.2V Stress
Fresh State

2.3 h

5% grid resistance increase
4.6 h
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Failure Location Depends on Grid Geometry

- DUT1 & DUT2 showed earlier VSS net EM degradation
- DUT3 & DUT4 have fast VDD net EM degradation
Failure Location Analysis and Validation with Simulation

- Physics-based EM simulator confirms the VSS degradation dominant aging behavior
- Largest void counts predicted in VSS net
Conclusion

• The power grid’s lifetime is longer with wider, denser power rails and more via redundancy
• Cell via count didn’t show noticeable aging behavior differences
• The EM-induced local resistance increase is faster in the VSS net due to high tensile stress in the metal interconnect

Acknowledgment: This work was supported in part by the Semiconductor Research Corporation (SRC) through the Texas Analog Center of Excellence (TxACE) and Programme d’Investissements d’Avenir, IRT Nanoelec under grant ANR-10-AIRT-05