Electromigration Test Chip Experiments From Realistic Power Grid Structures: Failure Trend Comparison and Statistical Analysis

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***Abstract*—This work presents electromigration (EM) silicon data from realistic power grid device-under-tests (DUT). Power grids featuring logic gate equivalent quasi-load cells were generated by an automatic place-and-route tool to compare the EM failure location and lifetime behaviors. IR drop shifts and voiding location trends inside the grids were measured. Four different power grid EM characteristics are analyzed to explain the layout-dependent aging from 33 DUTs.**

***Index Terms*—Electromigration, power grid, BEOL, on-chip heater, reliability, void, TTF.**

I. Introduction

Electromigration in power grids is a critical back-end-of-line (BEOL) reliability concern due to high direct current and Joule heating. Especially in cutting-edge technology nodes, the scaling down of transistor feature sizes and metal routings results in high current density in interconnects in a power delivery network (PDN), which could lead to earlier EM-induced void formation. Such EM aging phenomenon could locally increase the grid interconnect resistance, which results in excessive IR drop and power delivery failure.

However, experimentally characterizing an on-chip PDN's EM behavior with silicon data is not trivial. One major difficulty is that typical CMOS logic gates placed in a power grid cannot withstand extreme experimental conditions. Since the grid failure must be accelerated by a large stress current and extreme (also accurate) DUT temperature (e.g., > 300°C), the load cells should be specially designed. Another difficulty is monitoring the power delivery from power pads to each logic cell in the grid for local EM aging analysis. Such power delivery data collection after EM-induced voiding often requires voltage scanning schemes with a specially designed test chip. Thus, previous works have analyzed EM effects in metal grids but were limited to simple test structures [1] or relied entirely on simulation models [2].

In this work, we present a test-chip-based novel end-to-end

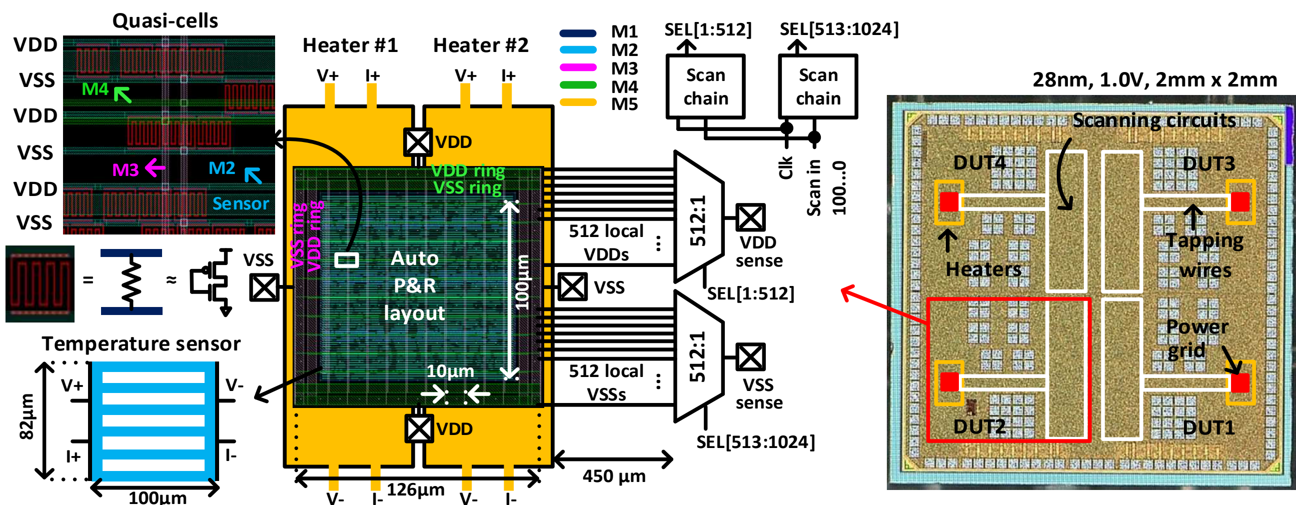

Fig. 1. 28nm power gird EM test chip overview. DUT includes a power grid (M2-M4) and quasi-cells with gate equivalent poly resistances. The heating area is covered by two metal heaters (M5) and a temperature sensor (M2). The voltage measurement circuit includes two scan chains and two 512:1 analog muxes.

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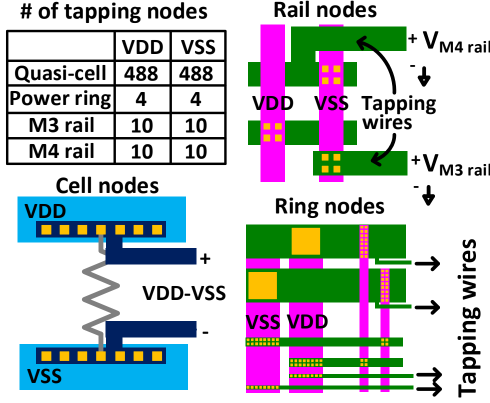

Fig. 2. Breakdown of voltage tapping nodes and tapping locations in quasi-cells, power rings, and power rails. The tapping nodes allow measuring voltage delivery from rings and rails to each cell.

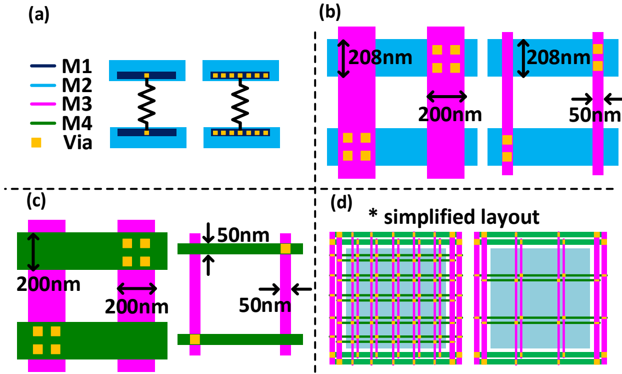

Fig. 3. Designed power grids' structural difference details. (a) Cell via counts. Min vs. max cell via (b) M2, M3 rail widths and M2-M3 vias. (c) M3, M4 rail widths and M3-M4 vias. (d) Number of M3 and M4 rails (rail density)

Power grid		DUT1	DUT2	DUT3	DUT4
# of cell via		1	7	7	7
M3, M4 rail width (nm)		200	200	50	50
# of rails	M3 VDD	10	10	10	2
	M3 VSS	10	10	10	2
	M4 VDD	10	10	10	2
	M4 VSS	10	10	10	2

Fig. 4. Comparison table of four different DUTs. DUT2 is the baseline design with maximum via and rail strengths.

power grid EM characterization methodology. The EM test vehicle consists of four different grid types with 1024 voltage tapping points per grid for measuring the power delivery status. The voltage measurement circuit is capable of tracking IR drops in power rings, power rails, and quasi-cells. An accurate DUT temperature control loop with a maximum temperature error of 2-3°C was implemented using on-chip metal heaters and a DUT temperature sensor [3]. Structure-dependent degradation behaviors are compared since we have four grid structures with different via and rail strengths. The comparison between the silicon data and an industry-grade EM mechanical stress simulator explains such failure trends with void-forming locations and statistics.

II. Design Description

A. *Test Chip Design Overview*

An overview of the 28nm power grid EM test vehicle is given in Fig. 1. The metal interconnects used in this technology are copper (Cu). We first synthesized a digital functional block and generated a 100µm x 100µm layout using an automatic place-and-route tool. Then, we replaced the individual logic gate cells with equivalent poly resistor cells so that the load circuits could withstand the stress temperature required for EM acceleration. The equivalent loads are custom-designed thin snake-shaped silicided poly resistors. The automatically generated power grid consists of three metal layers (M2-M4), including power rings and rails, with poly-based quasi-cells. Two upper rails (M3, M4) are connected to the power rings (also M3 and M4), delivering power to the lower M2 rails and quasi-cells. The power grids were placed inside the heating area, whose temperature is controlled by two on-chip metal heaters (M5) with individual control. A dedicated M2 metal temperature sensor was used for the temperature feedback. The power grid's internal voltages are measured using a voltage tapping method. The 512 local VDD and 512 local VSS voltages are tapped from across the power grid and routed to two 512:1 analog multiplexers, which are controlled by a 1024-stage scan chain. As explained in Fig. 2, 488 of the 512 voltages were measured from the quasi-load cells. The calculated VDD-VSS of 488 loads helps in understanding the power delivery status after EM. The remaining 24 voltages were measured from various points of the power rails and power rings.

B. *Power Grid DUT Comparison*

As illustrated in Fig. 3, the four power grid types have different cell via counts, rail widths, and rail densities. The DUT2 is a baseline design with the strongest vias and rails, as shown in Fig. 4. The purpose of the four different grid designs is to compare the layout-dependent EM failure behavior. For example, by comparing DUT1 with one cell via (M1-M2 via) and DUT2 with seven cell vias, the impact of the cell via on the EM degradation could be studied (Fig. 3 (a)). Similarly, the comparison of DUT2 and DUT3 (Fig. 3 (b-c)) can explain the rail via or rail width-dependent aging since DUT3 has narrower rails and fewer vias. Finally, as illustrated in Fig. 4 (d), DUT3 and DUT4 analysis provide the rail density-dependent EM.

III. Power Grid EM Experimental Methodology

A. *Experiment Flow*

Fig. 5 shows the overall experiment flow, including the heater control loop and voltage measurement loop running concurrently. The heater control loop maintains a consistent target DUT temperature by applying and updating heater

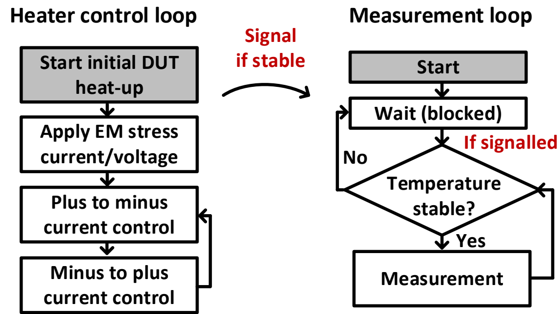

Fig. 5. Experiment flow with two concurrent controls. The heater control loop maintains consistent DUT temperature. The measurement loop that controls the voltage scanning circuits and external measurement experiments runs only if the DUT temperature is fully stable.

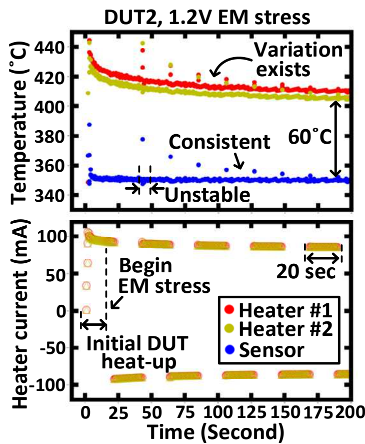

Fig. 6. (Top) Temperature control logs and heater current data. (Bottom) Measured heater currents.

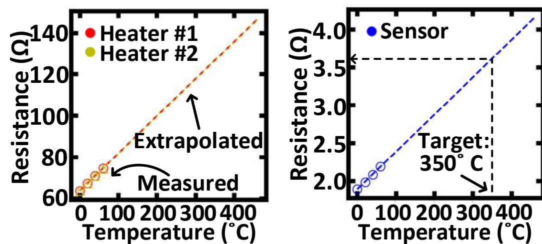

Fig. 7. (Top) Temperature control logs and heater current data. (Bottom) Measured heater currents.

currents (Fig. 6). Before applying the EM stress current, the heaters elevate the DUT temperature until the temperature becomes stabilized. The target DUT temperature for this experiment is 350°C (±1°C). Then, the EM stress current/voltage is applied to the power grid. The direction of the current applied to the heaters changes every 20 seconds to ensure the lifetime of the metal heaters by avoiding EM damage from the unidirectional heater current. The measurement loop controls the voltage scanning circuit and

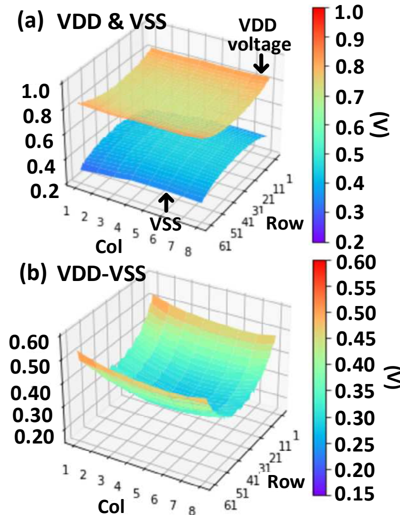

Fig. 8. (a) Measured fresh chip DUT2 cell VDD & VSS voltage map. (b) Time zero cell VDD-VSS voltage map.

the external measurement instruments. The measurement is done only if the DUT temperature is stable.

B. Temperature Control and Voltage Measurement

The accuracy of the DUT temperature is critical because the grid resistance and the IR drop profile can fluctuate with inconsistent grid temperature. One of the temperature inconsistencies comes from alternating heater current that results in short temperature variation, as shown in Fig. 6 (top). To overcome the possible measurement inaccuracy, dual-threaded control software performs the voltage measurement only when the temperature is stable. For example, the heater control thread monitors the DUT temperature and signals the measurement loop if the temperature is stable. The measurement thread is blocked when the DUT temperature is unstable and resumes measurement only if it is signaled.

The temperature coefficient of measurement (TCR) method was used to translate the heater and sensor resistance to the corresponding temperatures (Fig. 7). The heater and the sensor resistances are measured at 0, 20, 40, and 80°C using a temperature chamber and source meter units with 4-wire Kelvin sensing methods for accurate measurement. The TCR is then extrapolated to the higher temperature regions for the heater and sensor temperature measurement during the experiment.

IV. Data Analysis

A. Power Grid Failure Data Analysis

Fig. 8 (a) is a measured fresh chip voltage map of 488 cell VDDs and VSSs. By subtracting the VDD and VSS of each cell, the power delivery status is visualized (Fig. 8 (b)). Note that VDD-VSS values are higher at the edge due to the IR drop. Since the power starts from the power ring, the load

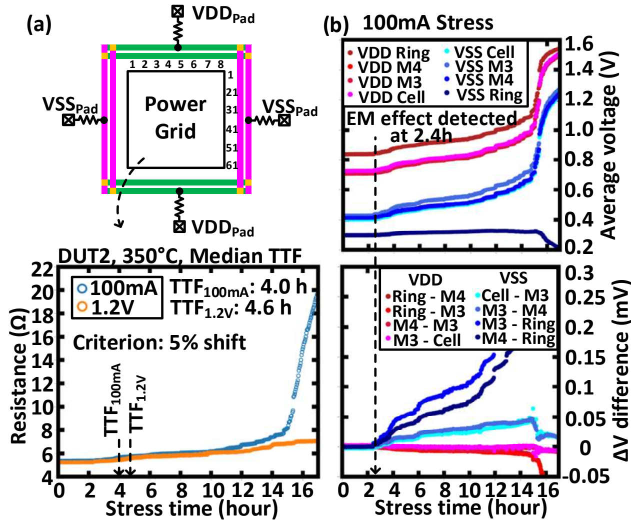

Fig. 9. (a) Power grid resistance shifting profiles are plotted for TTF measurement. The TTF criterion is a 5% resistance shift. (b) Breakdown of voltage traces. The ring, rail, and cell voltages are averaged (top). The voltage differences between the rings, rails, and cells for capturing subtle EM effect detection times and locations (bottom).

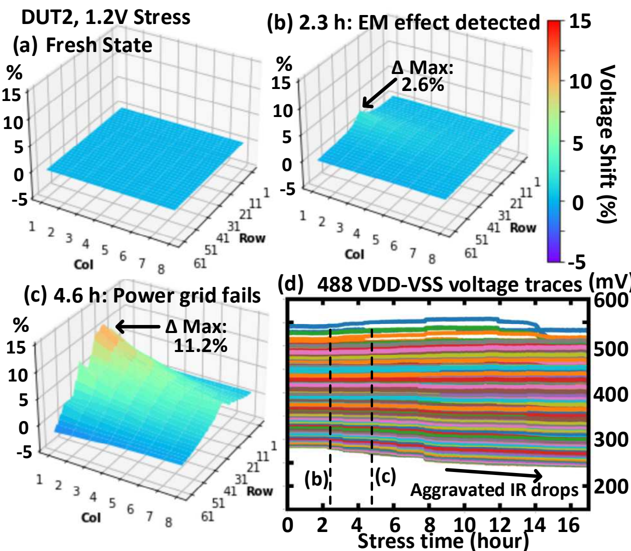

Fig. 10. Error map (voltage shift) of each cell VDD-VSS at (a) fresh state, (b) beginning of EM detection, and (c) when the power grid fails (TTF). (d) The power delivery is gradually aggravated after the EM stress.

cells located at the center of the grid have the lowest VDD-VSS.

Fig. 9 explains how the time to failure (TTF) was measured and the EM effect detection point was captured. As illustrated in Fig. 9 (a), the grid resistance from the VDD power ring to the VSS power ring (i.e., pad resistances are excluded) increases gradually due to the growth of EM voids in the grid. We defined the TTF criterion as a 5% resistance shift. Also, the ring, rail, and cell voltages are averaged and plotted to capture the subtle EM-induced local resistance shift, as shown in Fig. 9 (b). For example, if the 100mA stress

DUT1-3: 100mA
DUT4: 10mA, 350°C Temp.

Grid type	Average TTF (hour)	# of chips
DUT1	4.1	10
DUT2	4.0	13
DUT3	1.3	5
DUT4	3.8	4

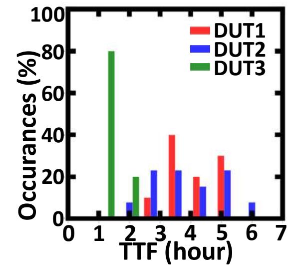

Fig. 11. Measured TTFs of different types of grids.

current is applied (to the power pads), EM is detected at 2.4h, and the grid resistance increases by 5% after 4.0h (i.e., TTF_{100mA} is 4.0h). Similarly, with 1.2V voltage applied to the pads, the EM is detected at 2.3h, while the $TTF_{1.2V}$ is 4.6h (Fig. 10). For DUT2, the 1.2V pad voltage is equivalent to 100mA total current at 350°C. The grid degradation of the voltage mode is slower than the current mode since its stress current becomes smaller with the increase of the grid resistance (Fig. 9 (a) bottom). The voltage shifts of VDD-VSS in Fig. 10 suggest that the excessive IR drop is relatively small at the beginning of EM detection (2.6% error, Fig. 10 (b)) but fails completely after TTF (>10% error, Fig. 10 (c)). The 488 cells' VDD-VSS values are plotted in Fig. 10 (d) to show the aggravated IR drops.

B. *Layout-Dependent Failure Analysis*

The reliability of a power grid highly depends on its via counts, rail widths, and rail densities. Thus, four different DUTs are tested with constant stress currents for layout-dependent failure analysis. Fig. 11 shows that DUT2's TTF is longer than DUT3 since it has wider power rails and more rail vias (Fig. 3 (b-c)). However, there are no clear lifetime differences between DUT1 (minimum cell via count) and DUT2 (maximum cell via) (Fig. 3 (a)). The detailed trend is shown in Fig. 12 voltage plots. As seen in the data, the voltage traces of DUT1 and DUT2 are very similar, which suggests that the number of vias inside the quasi-load cell doesn't play a major role in the EM voiding trend. We suspect this is due to each quasi-load cell's relatively small current density for early EM-induced voiding. The DUT1 and DUT2's voltage shifts in the VSS rails are greater than those in the VDD grid. On the other hand, DUT3 and DUT4 show significant voltage changes in the VDD nets. This suggests that the voids can hurt the power delivery not just locally but also in multiple power nets if the rail widths and rail spacings are poorly chosen.

Detailed EM behavior analysis in M2 and M3 rails is explained in Fig. 13. Note that the EM-induced atomic flux is maximized at the left and right edges of the M2 rails. For a downstream scenario (Fig. 13 (a)), since the power delivery starts from the power rings, electron wind is minimized in the middle of the power rails due to the electrons escaping to the resistive loads. As a result, in the M2 VSS net, high tensile strength is formed near the power ring regions. Therefore, the early void nucleation occurs on the left and right edges of the

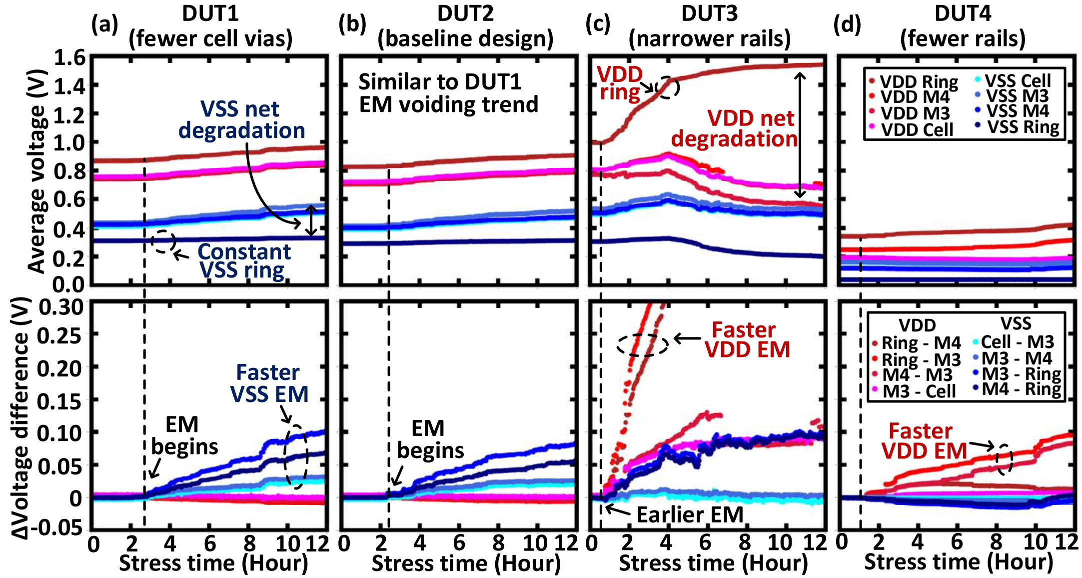

Fig. 12. Measured voltage traces at 350˚C. (a-c) 100mA stress current. (d) 10mA stress current.

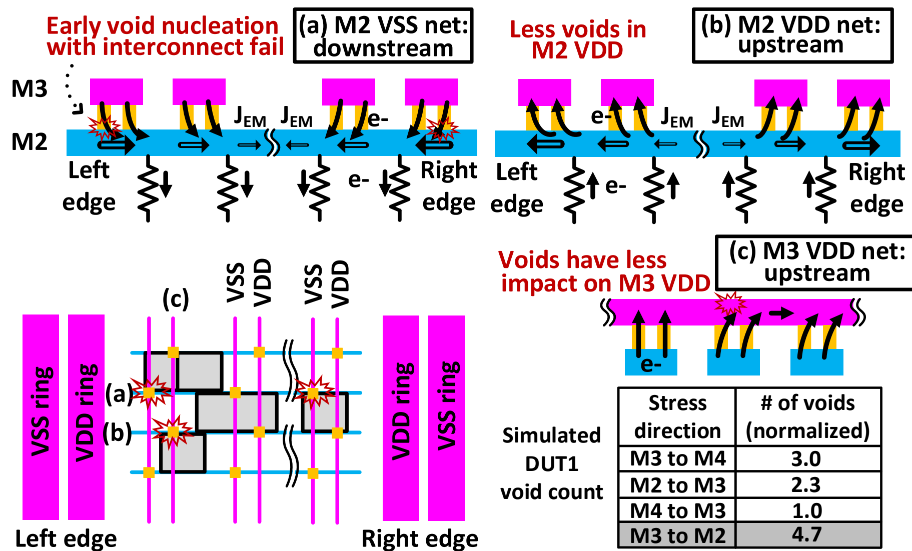

Fig. 13. EM void locations for M2 and M3 rails. (a) Void formation in VSS net and (b-c) VDD nets. The number of voids predicted by an industry-grade EM void simulator for validation of earlier EM in DUT1 VSS nets (bottom right).

M2 VSS rails, especially under the vias, which causes abrupt IR drops. On the other hand, in the M2 VDD net, the compressive stress is maximized at the edge regions, and the middle region has lower tensile stress due to the lower current density from the current distribution (Fig. 13 (b)). Furthermore, in the VDD nets, high tensile stress is not formed inside the M2 rails but in M3 (Fig. 13 (c)). Such above-via voids may have less impact on IR drop, which can explain the asymmetry in the VDD and VSS degradations. Also, an industry-grade EM simulator (Fig. 13 (bottom right)) [4] predicts that the number of M3 to M2 downstream voids (i.e., voids in M2 VSS net) is the largest, which explains why EM is more dominant on the VSS side.

V. Conclusion

This work presents a test chip design and experimental methodology for EM failure characterization in an on-chip power delivery network. The purpose of the test chip is to compare the power grid's layout-dependent EM lifetime behavior. As expected, the power grid's lifetime is longer with wider, denser power rails and more via redundancy due to lower current density. However, the cell via redundancy didn't show noticeable aging behavior differences since the current density in each cell is significantly lower than that in the upper power rails. The EM-induced local resistance increase is faster in the VSS net due to high tensile stress in the power nets resulting from more material depletion near the power ring regions. The EM voiding simulator also

proved that the VSS net dominates the grid resistance increase.

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