

On-chip Heater Design and Control Methodology for Reliability Testing Applications Requiring over 300°C Local Temperatures

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Abstract—This paper presents the design details and control methodologies for on-chip heaters that can provide fast and accurate local temperature control for reliability testing applications. The on-chip heater uses the Joule heating effect of a metal or poly line to heat the surrounding devices-under-test (DUT) to a target temperature as high as 300°C. Many generations of on-chip heaters, including different heater positions, heater areas, and heater layers, have been demonstrated in technology nodes from 350nm to 16nm. To accurately operate the heater and extend the heater's operation lifetime for long-term reliability testing, we have also developed control methodologies for precise and reliable heater control.

Index Terms— On-chip heater, reliability testing, heater lifetime, reliable heater control

I. INTRODUCTION

Precise control of the device under test (DUT) temperature is essential for variability and reliability studies. At elevated temperatures, failure mechanisms such as electromigration (EM) and bias temperature instability (BTI) are accelerated, allowing reliability parameters to be characterized in a manageable time frame. For example, studies have shown that EM failures can be studied within a few days of DC stress under a stress temperature of 300-350°C [1-8]. On the other hand, special applications such as automotive, aviation, oil and gas exploration, and space electronics often require ICs to operate beyond the temperature range of consumer products. Circuit qualifications at high temperatures [9] are required for IC designs targeting these special applications.

For high-temperature testing, the entire testing set up is usually placed inside a temperature chamber or oven. However, conventional setups expose the critical measurement circuits and package/board components to high stress temperature which can introduce measurement noise/errors or data drift. Another limitation of existing approaches is that commercial temperature chambers have a limited temperature range (e.g., -40°C to 120°C). To stress/characterize IC outside of this region, expensive and specialized equipment is required. Furthermore, these temperature chambers take tens of minutes to switch from one temperature to another [10], mainly because the entire space inside the chamber needs to be cooled or heated. This introduces extra wait time for measurements and is not desirable for time-sensitive measurements such as BTI

characterization.

On-chip heaters are attractive due to their fast, highly efficient temperature control, as well as simple implementation compared with expensive testing equipment. On-chip heaters rely on the Joule heating effect to heat up the surrounding components. Polysilicon gates, for example, have been used for on-chip heaters [11, 12]. The polysilicon heater is suitable for fast temperature change of a DUT with limited size, but it will also completely block any other logic in that heater area and introduce layout design rule challenges, making them sub-optimal for large and complicated DUT structures. On the other hand, metal heaters can be placed either above or below the DUT, providing more flexibility in terms of circuit placement. Moreover, this type of flexibility makes it possible to overlap the heater with the DUT thereby increasing the heat transfer efficiency. Four terminal Kelvin measurement of the heater provides accurate reading of the heater resistance. The metal heater, combined with dedicated temperature sensors near the DUT, can provide accurate heater temperature feedback control.

In this paper, we summarized the on-chip heater designs we have used in many test chips for fast and accurate local temperature control. We will also discuss the control methodology for operating the on-chip heater reliably. The on-

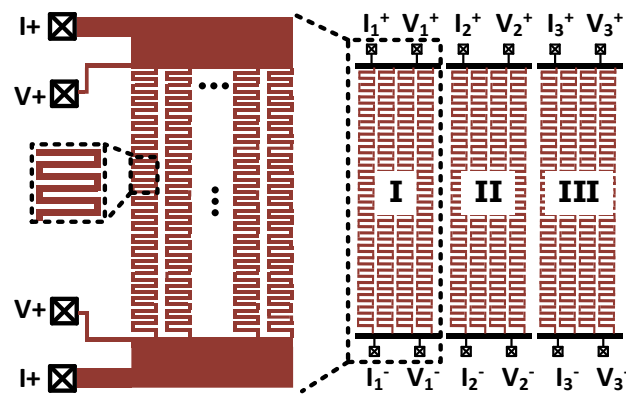


Fig. 1. (Left) On-chip heater with four-terminal Kelvin testing connection. (Right) Multiple heaters can be used to raise the temperature of a larger circuit area.

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chip heater concept has been used in different process nodes from 350nm to 16nm and for different testing purposes. The on-chip heater based temperature control solution has proven to be efficient, versatile, easy to implement, and compatible across different technology nodes.

II. ON-CHIP HEATER DESIGN STEPS

As shown in Fig. 1, The heater uses parallel and serial connected snake-shaped metal wire to cover a large enough area and maintain a reasonable resistance simultaneously. In addition, the heater uses four terminal Kelvin connection, with the voltage tapping points placed as close to the heater core as possible. This can prevent the parasitic resistance of the connection wire from corrupting the heater resistance measurement. Next, we will describe the specific guidelines for designing an on-chip heater that meets the design goals.

A. Design Considerations

The key parameters to consider while designing an on-chip heater are:

- 1) Heater layer
- 2) Target heater power density
- 3) Heater area
- 4) Heater resistance

To maximize the heat transfer efficiency from the heater to the DUT, the on-chip heater should be placed as close to the DUT as possible. However, a densely placed metal wire in the heater will completely block any routing spaces in that area. Therefore, a practical suggestion is to place the heater one layer above the DUT's highest metal.

conductance of the materials surrounding the heater is complicated and most of the time unknown to circuit designers, especially in scaled technologies. With a high thermal conductance, the generated heat is transferred outside of the chip easier than in the lower thermal conductance case; therefore, a higher power density is required for the heater to reach the same target temperature. We have provided our measurement data in Table 1 for the reader's reference. It includes the power density required for a heater to reach its target temperature in four different process nodes. We can see that this number varies significantly in different technologies. The general trend is that for more advanced technologies, the required power density is lower. We believe this is a result of lower thermal conductivity as technology scales. Limited by the simplicity of our testing setup, we cannot measure the thermal conductivity data by ourselves across different technologies. However, there has been extensive research in related materials/self-heating area [13,14].

Once the target power density is determined, a spreadsheet calculation using metal's sheet resistance (as shown in section II. B) could give us choices of width, length, and area of the heater to cover the DUT. We have found the heater resistance prediction based on the sheet resistance value provided by the foundries to be pretty accurate. The maximum power of one heater is limited by the maximum voltage and current that the chip can tolerate. From our testing experience, a voltage between 10 to 12 volts and a current up to 140mA is a safe range for most technologies we have used. If a single heater is not enough to cover the entire DUT area, multiple heaters can be implemented, with each heater having a four-terminal Kelvin connection, as shown in Fig.1.

Because on-chip heaters operate at extremely high temperatures, EM failures will occur inevitably; however, to minimize the effect of EM, a heater design with higher resistance and smaller current density is generally preferred. Another way to extend the heater lifetime is to periodically toggle the direction of the heater current so that the "electron wind" is not always blowing in the same direction. With our carefully designed heater controlling methodology, the heater's lifetime could be significantly extended in all of our designs, making the heater lifetime longer than the testing timeframe, which can be as long as several weeks. The following section will give an example calculation showing how to determine the heater layout based on a hypothetical target temperature and DUT area requirement.

TABLE I

REQUIRED ON-CHIP HEATER POWER DENSITY IN DIFFERENT TECHNOLOGIES

Technology	Current (mA)	Voltage (V)	Area (mm ²)	Power Density (W/mm ²)	Δ Temp (°C)
16nm [5]*	62	3.5	0.016	13.6 (left)	305
	59	3.3	0.016	12.2 (mid)	
	64	3.6	0.016	14.4 (right)	
28nm	73	10.4	0.020	38.0	380
65nm [9]	91	14.8	0.010	134.7	325
350nm	144	9.5	0.013	105.2	275

*: Measured Data from a 3 heater system

To serve special testing purposes, polysilicon heater structures have been used for back-end-of-line electromigration (EM) measurement [1]. For polysilicon heaters, thick poly strips are used instead of snake-shaped poly wire because polysilicon has a significantly larger sheet resistance compared to metals.

The target power density of the heater is another important consideration for designing an on-chip heater and is usually hard to determine accurately. A higher power density is desirable as it can help reach a higher DUT temperature; however, this is always limited by the maximum voltage and current a heater or the IO pad can withstand. It is non-trivial to determine the required power density since the thermal

B. On-chip Heater Design Example

As an illustrative example, let us assume that the target heater temperature is 300°C, the operating ambient temperature is 0°C, and the area of the heater is 100μm x 100μm in a 65nm technology. From table I, we know the power density should be 134.7 W/ mm² for a 325°C ΔT in the heater. We can select the same number here. Then, the total heater power can be calculated as follows:

$$134.7 \frac{W}{mm^2} \times (0.1mm)^2 = 1.347W$$

Next, for a heater voltage range from 1V to 12V, the required current and resistance under target temperature can be calculated, and the result is listed in Fig. 2 (a). Based on the safe operation region, the possible voltage and resistances are shown

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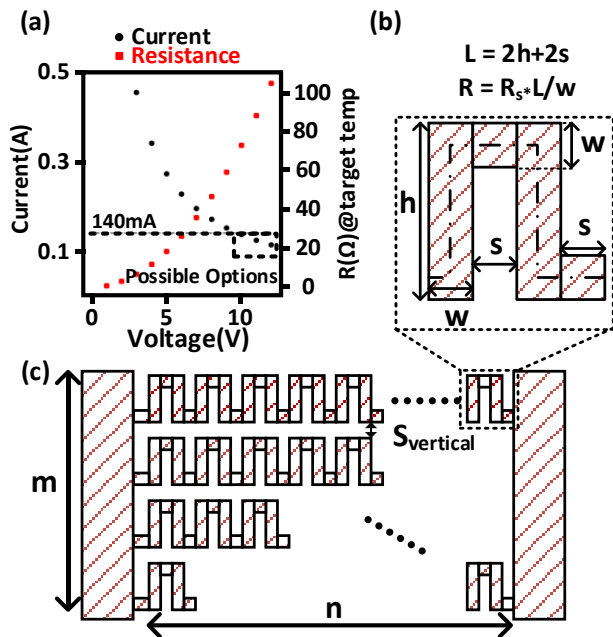


Fig. 2. (a) Determining the safe heater current, heater voltage and target resistance for a given target temperature. (b) Heater unit cell, with length and resistance calculations. (c) Layout of a heater with $m \times n$ unit heater cells.

as well. To make sure we are operating the heater under safe conditions, we prefer an operating voltage of 11V and an operating current of 124.5mA, with a resistance of 88Ω at the target temperature (300 °C). Based on the Temperature Coefficient of Resistance (TCR) relationship provided by the foundry, we can calculate its resistance R' under room temperature.

The third step is to design the heater's layout which requires us to find a set of design parameters (h, w, s, m, n in Fig. 2) that meet our area and power consumption requirements. We first construct a unit cell of the squared-shaped metal heater, as shown in Fig. 2 (b). The dotted line length is used as the wire length (L), and the width of the wire is denoted as w . We then

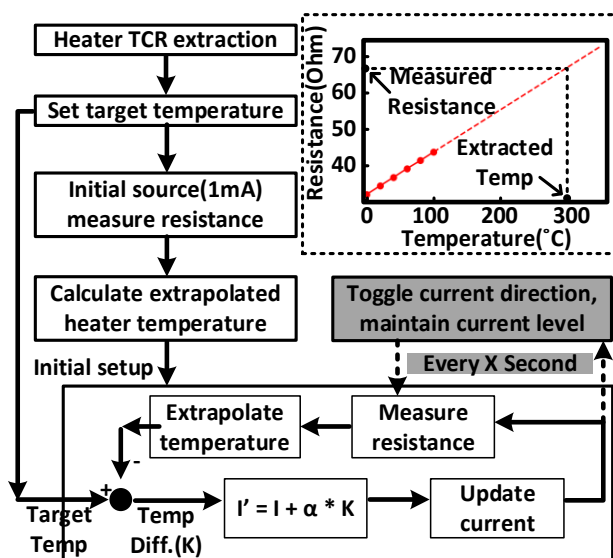


Fig. 3. Heater temperature control loop.

concatenate the unit cell n times to form one string and m strings in parallel with a gap $S_{vertical}$ to form the heater area. The generated heater area should meet the $100 \times 100 \mu m^2$ area requirement. Solving the following equation gives us the heater layout dimensions.

$$m \times h + (m - 1) \times S_{vertical} = 100 \mu m$$

$$(2w + 2s) \times n = 100 \mu m$$

$$R_s * \frac{L_{unit}}{w} * \frac{n}{m} = R'$$

It is obvious that the solution is not unique, and any combination should be able to meet the temperature and area requirements. The final step is to add a wide and strong connection to the IO pad. To accurately sense the heater's resistance, four-terminal Kelvin connection needs to be used (as shown in Fig. 1). The voltage sensing points should be placed as close to the heater core as possible. If a safe voltage and current combination cannot be found for a target temperature, one should consider placing multiple heaters to cover the entire area.

III. HEATER CONTROL METHODOLOGY

A. Negative Feedback Control Flow

In order to perform fast and precise local temperature control, we have developed a set of control methodologies based on a first-order negative feedback control system, as shown in Fig. 3. For each heater, we will first extract the TCR relationship. The TCR of the heater will be extracted inside a benchtop temperature chamber, which has precise temperature control from $-20^\circ C$ to $120^\circ C$. During the measurement of the TCR, we will first wait for the temperature chamber to reach a stable state at a given temperature for 5 minutes, then apply a 1mA current and measure the resistance using a source meter unit (SMU). A 1mA current was low enough to ensure that the metal wire's Joule heating will not affect the resistance measurement accuracy. Furthermore, with the resistance (60~80Ω under room temperature) we have designed, 1mA of current generates enough voltage difference for the SMU to sense accurately. Because our work focuses on the circuit-based test structure comprising the DUT, the supporting circuitry, and a standard test board, we are unable to calibrate the TCR at temperatures higher than $120^\circ C$, as extremely high temperatures might damage the off-chip components. The TCR of the metal heater shows high linearity over the calibration temperature range (Fig. 3), and dedicated metal measurements conducted by other groups [15] have shown high linearity up to $300^\circ C$.

When driving the heater, for a given target temperature, a 1mA current will be applied through the heater to check the initial temperature, and then the heater will be controlled based on the negative feedback loop as shown in Fig. 3. Because the heater will be driven by a strong current and will reach a very high temperature, EM will happen very quickly. To extend the heater's lifetime, we need to toggle heater's current direction periodically around every 10 to 20 seconds. Prior to switching the current direction, the program will first record the previous heater's current level and provide the same current density but

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in the opposite direction. The resulting heater control log file is plotted later in this paper (Fig. 7). Generally, it takes less than 30 seconds for the heater to reach its target temperature, and after that, the heater temperature will be maintained at the target temperature until the end of the measurement. A few additional improvements can be considered for special high-temperature measurements: 1) When switching the current direction, there is an instantaneous temperature fluctuation. 2) During our measurement, we observed a $\sim 1^\circ\text{C}$ temperature difference between the two current directions. We believe this is because the SMU we use has a slight mismatch between positive and negative current measurements. 3) There is always a temperature difference between the heater and the DUT due to the physical distance. In the following section, several advanced methods will be introduced to the reader, which provide more accurate and stable heater control.

B. Feedback Loop Based DUT Temperature

The ultimate goal of an on-chip heater is to regulate the DUT temperature and not the heater temperature. However, in many experiments, we saw discrepancies in the heater and DUT temperatures due to the vertical distances. Fig. 4 (a) shows a back end of line (BEOL) EM test structure that includes metal heaters on M5, a DUT on M1, and a dedicated temperature sensor on M2. The sensor is placed as close as possible to the

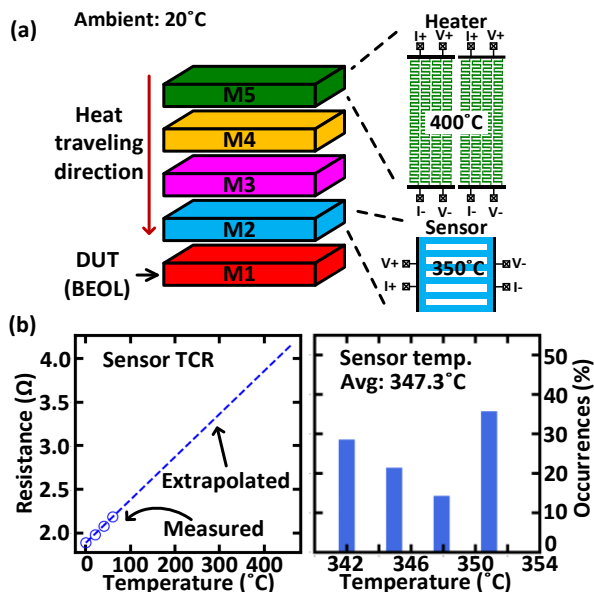


Fig. 4. (a) Vertical distance between temperature sensor and metal heaters, (b) TCR and Histogram of the sensor temperatures of 14 chips when the heater temperature is regulated at 400°C.

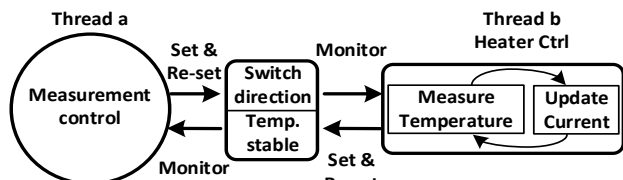


Fig. 5. Dual thread control for accurate and stable temperature and DUT measurements.

DUT to measure the DUT's temperature with maximum accuracy. The ambient temperature is maintained at 20°C by the temperature chamber, and the heater temperature is set at 400°C using negative feedback control. Based on our experiment from 14 different chips, the average DUT temperature is around 50°C lower than the heaters' temperature, indicating a strong vertical temperature gradient. Furthermore, the DUT's temperatures can vary due to the chip-to-chip variations and the DUT's Joule heating effect. Fig. 4 (b) shows the sensor temperature (M2) near the DUT (M1) measurement result of 14 different chips, showing a chip-to-chip temperature variation of up to 10°C . One solution for resolving the inconsistent DUT temperature is to use the sensor temperature as the input to the feedback loop instead of the heater's temperature. Similar to the heater, in order to accurately measure the sensor's temperature, a four-terminal Kelvin connection is must be used for the temperature sensor. Even though this approach requires a dedicated sensor near the DUT with extra IO pads and source meter units, this was required for precise DUT temperature control.

C. Separating Temperature Control and DUT Measurements

The negative feedback loop relies on frequently updating the current/voltage to maintain a stable temperature condition. If the heater control loop and the measurement control loop belong to the same program thread, then the DUT measurement operation will stall the heater current/voltage control, and vice versa. Depending on the measurement's complexity, it might significantly reduce the current/voltage update frequency.

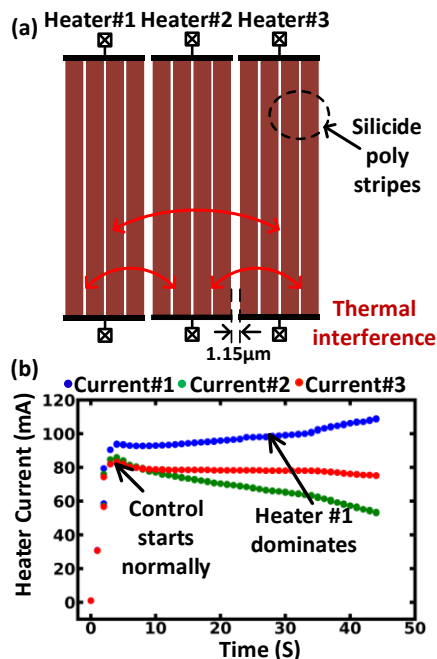


Fig. 6. (a) Thermal interferences between heaters can cause thermal runaway issues and prevent a stable temperature control. (b) Measurement results showing the left most heater dominating the temperature control. This issue was resolved by designing a new board with better thermal conductance and lowering the ambient temperature.

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Therefore, we recommend decoupling the heater control flow from the DUT measurement process using multi-thread programming to achieve the highest frequency for updating the heater's current and voltage.

Multi-threading also provides more flexibility in operating the heater. For example, if the temperature fluctuation when switching the current direction is problematic for sensitive measurements, we can add extra communication flags between the heater-controlling thread and the DUT measurement thread to perform thread synchronization. When a measurement period is finished, the measurement thread sends a signal to the heater control thread to change the current direction and pauses the measurement. Upon receiving the signal, the heater control will start toggling the current direction and allow the negative feedback loop to reduce the temperature fluctuation until the temperature is stable again. Then, an indicator signal will be sent to the measurement thread and resume the DUT measurement. Communication between the two threads is illustrated in Fig. 5.

D. Multiple Heater Control and Multi-Variable Control Issue

As explained in section II-B, heater structures are carefully designed based on the target power density and the safe current/voltage ranges. However, if a test structure requires a large heating area and each heater can only cover part of the DUT region, multiple heaters have to be incorporated. The heaters are often placed adjacent to each other to create a uniform stress temperature over the entire DUT area. Fig. 6 (a) shows an example of three parallel silicided poly heaters in 65nm technology. The basic idea of operating a multi-heater system is the same as single heater control.

One heater control challenge we faced with the multi-heater system was the thermal interference between the individual

heaters. During our measurement, we found that even with well-calibrated control flows, in some cases, on-chip heaters cannot reach a stable temperature if multiple heaters are closely placed due to the multi-input multi-output control issue. For example, without any thermal interference, the temperatures of adjacent heaters should depend solely on its own current. However, as illustrated in Fig. 6, the temperature of heater #2 is not only decided by current #2 but also by the "side-channel" heat from heater #1, which also depends on current #1. Thus, if one of the heaters starts to control the adjacent heater's temperature and eventually dominates the entire heating area (Fig. 6 (b)), it becomes difficult to achieve a uniform temperature condition.

The main reason for the multi-variable control issue is the inevitable thermal interference between heat sources. Such convoluted interference could be mitigated by lowering the ambient temperature or using a better heat sink which helps lower the thermal interference.

IV. MEASUREMENT RESULTS

A. Heater Temperature Profile

Fig. 7 shows the heater temperature logs from our test chips fabricated in 0.35 μ m, 65nm, 28nm, and 16nm, respectively. In fig (a, b, c), the red and blue colors denote the forward and reverse current directions. Due to different test chips with their test purposes, the ambient temperature and heater target temperatures are not the same. However, all four heaters have successfully reached their target temperature. The amount of temperature fluctuation while we switch current direction varies in different technology nodes. In 0.35 μ m technology, the fluctuation could be as high as $\sim 3^\circ\text{C}$; however, in 65nm, 28nm, and 16nm technology, the fluctuation could be controlled

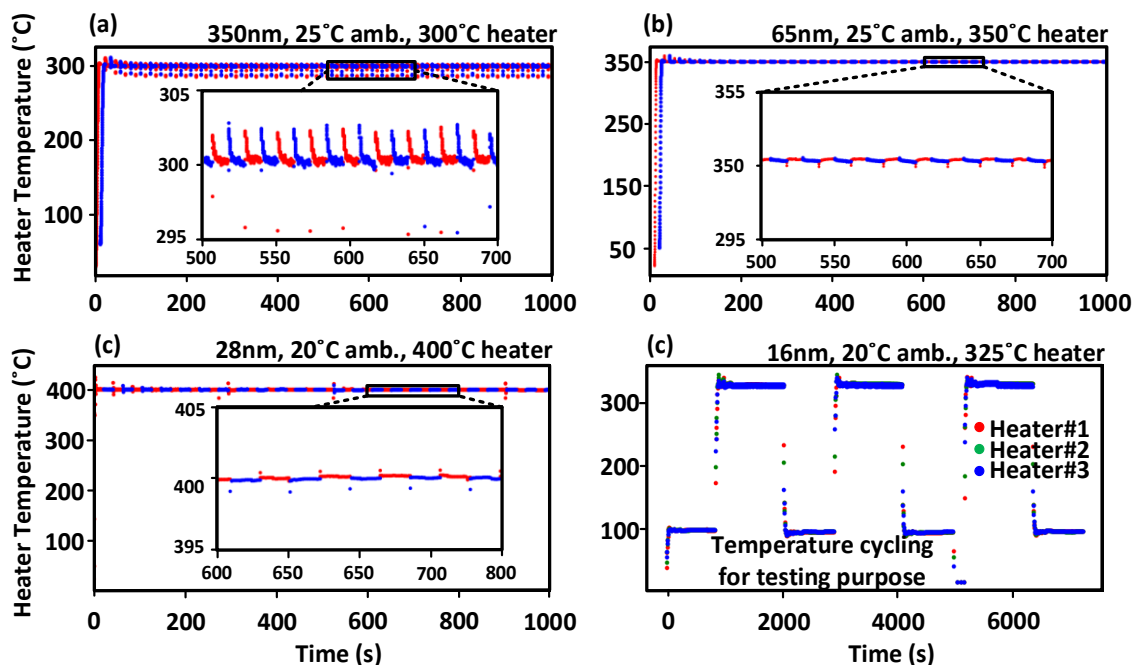


Fig. 7. Heater temperature log for 1,000 seconds measured from four test chips: (a) 350nm, (b) 65nm [9], (c) 28nm, and (d) 16nm [5]

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within $\sim 0.5^\circ\text{C}$, this is possibly due to the thermal conductance in $0.35\mu\text{m}$ technology being much higher than in the other three. When the current direction is switched, there will be a moment when no current is flowing through the heater, and the accumulated heat is quickly removed from the heater area, causing a temperature drop. The temperature fluctuates about 1% with respect to the ΔT above the ambient temperature, and the negative feedback loop can restore the heater temperature within 1 second. This small amount of temperature fluctuation is acceptable for high-temperature stress (EM, BTI), but if it is problematic for temperature-sensitive measurements, the multi-thread controlling approach with thread synchronization could be implemented.

B. Local Temperature Distribution

The resistance of a metal wire provides an accurate measure of its temperature; however, the resistance shows only a geometrical average of the temperature of the entire metal area. Moreover, because the metal heater is usually placed on higher levels, there will be a temperature difference between the heater and the DUT (vertically) and underneath the heater at different points (horizontally). There has been an extensive study on on-chip temperature measurement in self-heating research [16-18]. However, none of them have reached a temperature above 140°C . In this section, we will present our effort to measure the

spatial temperature distribution underneath an on-chip heater.

This measurement is performed on a $0.35\mu\text{m}$ test chip. The back end of this technology has four metal layers, M1 to M4, and the heater is placed on M3. Six M1 sensors are placed under the heater with four-terminal Kelvin connection to ensure accurate resistance measurements, and each sensor could be individually selected using individual select switches. Among the six sensors, four of them are directly under the heater, and two of them are outside of the heater at a $30\mu\text{m}$ distance from the edge of the heater. The schematic of the sensors and their relative positions are shown in Fig. 8 (a). The M1 metal sensor was chosen because it can track the temperature of the junction, and the TCR linearity is near-ideal. The TCR curve of one of the six sensors is also shown in Fig. 8. Similar to the metal heater, the M1 metal sensor also has excellent linearity in the TCR measurement range ($0^\circ\text{C}\sim 100^\circ\text{C}$). This setup has been evaluated under a 40°C ambient temperature controlled by a temperature chamber and heater temperatures from 300°C to 450°C with a 50°C step. Compared to the center of the heater (sensors #2 and #3), at the edge of the heater, the temperature drops 10% (sensors #1 and #4). $30\mu\text{m}$ outside of the heater, the temperature drops to 57% (sensors #0 and #5) compared with the hottest region. We have also measured another set of temperature sensors outside the heater area. For this chip, $800\mu\text{m}$ away from the heater's edge, the temperature remains 40% of the hottest region. From this set of data, we can see that in the measured technology, there is roughly a 10 percent temperature difference within the heater and that the heater not only heats the DUT but also some of the peripheral circuits away from the DUT due to the escaped heat. Designers should use caution a peripheral circuits far away from the heater area may also be exposed to a high temperature.

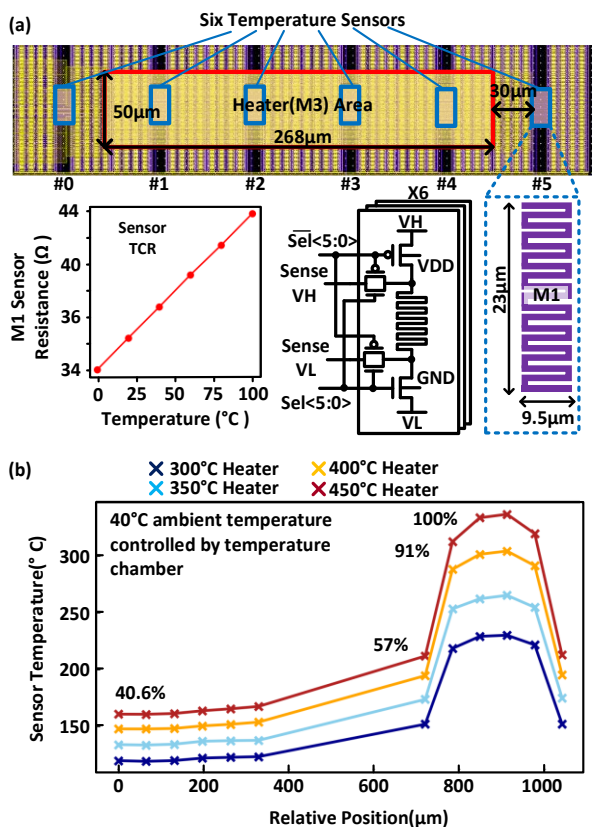


Fig. 8. (a) Six on-chip temperature sensors using M1 resistor. (b) Local temperature measurement results from 6 temperature sensors underneath the heater area and 6 sensors far away from sensor area showing lateral heat spread.

C. Metal Heater Resistance Change and Lifetime Concerns

Due to the narrow snake-shaped wire geometry and the high

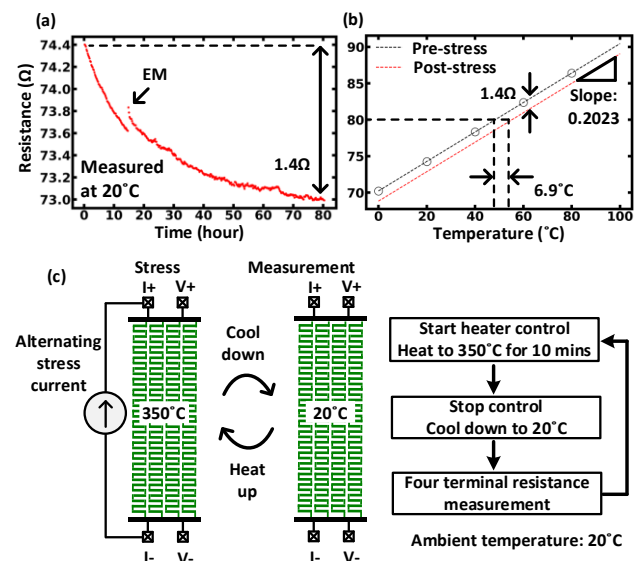


Fig. 9. (a) Metal heater resistance's change over its lifetime in a 28nm technology test chip. (b) Impact of heater degradation on temperature measurement accuracy. (c) Heater lifetime experiment.

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current density used to reach high temperatures, metal heaters generally face reliability issues. Such heater lifetime issues manifest as an increase or decrease in heater resistance. Fig. 9 (c) shows the heater lifetime experiment flow. In this experiment, we operate the heater normally but periodically turn off the heater and re-check its resistance at ambient temperature. The metal heater is stressed by a current higher than 70mA with alternating directions. Fig. 9 (a) shows that the metal heater's resistance gradually decreases by 1.4Ω over 80 hours of heater runtime. Also, in the middle of the resistance degradation, an EM-induced abrupt resistance jump occurs around 15 hours of heater operation. Both heater damages shift the TCR, resulting in inaccurate temperature measurement. For example, as illustrated in Fig. 9 (b), a 1.4Ω resistance decrease translates to a 6.9°C temperature overestimation. Thus, after 80 hours of experiment, the heater temperature is 356.9°C , which is slightly higher than the target. One approach to address the resistance drift issue is recalculating the TCR right before starting the heater control. Since the slope of the TCR generally doesn't change even after the resistance shift, by measuring the resistance at 20°C , TCR could be recalibrated based on the new data point. However, instead of recalibrating the TCR, the best solution is using the DUT temperature-based control with a dedicated temperature sensor, as introduced in section III-C. By using such a strategy, heater damages and inaccuracies can be overcome.

V. CONCLUSION

In this paper, we have provided the design details and control methodology of on-chip heaters (polysilicon/metal) for fast and accurate local temperature control. It is suggested that on-chip heaters be implemented together with a temperature sensor near the DUT for the most accurate temperature control. We have demonstrated that on-chip heater structures are capable of high-temperature stressing and characterization in different chips and technology nodes. A set of heater-controlling methodologies have been designed for reliable, fast, and accurate local temperature control and can fit multiple testing purposes. The temperature profile under the heater is characterized using separate metal line based temperature sensors. The heater's lifetime concern is addressed by toggling the current direction, and the heater's resistance change during its lifetime is profiled. We hope this paper can serve as a design reference for other group's interested in utilizing on-chip heaters for various testing purposes.

REFERENCE

- [1] C. Zhou, R. Fung, S. Wen, R. Wong, and C.H. Kim, "Electromigration Effects in Power Grids Characterized from a 65 nm Test Chip", *IEEE Trans. On Device and Materials Reliability (TDMR)*, pp. 74-83, 2019.
- [2] N. Pande, C. Zhou, MH Lin, R. Fung, R. Wong, S. Wen, and C.H. Kim, "A 16nm All-digital Hardware Monitor for Evaluating Electromigration effects in Signal Interconnects through Bit-Error-Rate Tracking", *IEEE Trans. on Device and Materials Reliability*, pp. 194-204, 2022.
- [3] V. Sukharev, A. Kteyan, J. Choy, F. N. Najm, Y. Yi, C.H. Kim, "Experimental Validation of a Novel Methodology for Electromigration Assessment in On-chip Power Grids", *Design Automation Conference (DAC)*, pp. 4837-4850, 2022.

- [4] N. Pande, C. Zhou, M.H. Lin, R. Fung, R. Wong, S. Wen, and C.H. Kim, "Electromigration-Induced Bit-Error-Rate Degradation of Interconnect Signal Paths Characterized from a 16nm Test Chip", *VLSI Technology Symposium*, pp. 1-2, 2021.
- [5] N. Pande, C. Zhou, MH Lin, R. Fung, R. Wong, S. Wen, and C.H. Kim, "Characterizing Electromigration Effects in a 16nm FinFET Process Using a Circuit Based Test Vehicle", *IEEE International Electron Devices Meeting (IEDM)*, pp. 5.3.1-5.3.4, 2019.
- [6] C. Zhou, R. Fung, S. Wen, R. Wong, and C.H. Kim, "Electromigration Effects in Power Grids Characterized from a 65 nm Test Chip", *IEEE Trans. On Device and Materials Reliability (TDMR)*, pp. 74-83, 2019.
- [7] C. Zhou, R. Wong, S. Wen, and C.H. Kim, "Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points", *VLSI Technology Symposium*, pp. 19-20, 2018.
- [8] C. Zhou, X. Wang, R. Fung, S. Wen, R. Wong, and C.H. Kim, "A Circuit based Approach for Characterizing High Frequency Electromigration Effects," *IEEE Trans. on Device and Materials Reliability (TDMR)*, pp. 763-772, 2018.
- [9] H. Yu*, G. Park*, and C.H. Kim, "Extreme Temperature Characterization of Amplifier Response Up to 300 Degrees Celsius Using Integrated Heaters and On-Chip Samplers", *European Solid-State Circuits Conference (ESSCIRC)*, pp. 411-414, 2021, *equal contribution.
- [10] S. Jeong, J. Kim, A. Kim, B. Kim, M. Lee, J. Chang, I.H. Baick, H. Kang, Y. Ji, S. Shin, S. Pae, "Optimal design of dummy ball array in wafer level package to improve board level thermal cycle reliability (BLR)," *2018 IEEE International Reliability Physics Symposium (IRPS)*, pp. P-3D.1-1-P-3D.1-4, 2018.
- [11] T. Aichinger, M. Nelhiebel, S. Einspieler and T. Grasser, "In Situ Poly Heater—A Reliable Tool for Performing Fast and Defined Temperature Switches on Chip," *IEEE Transactions on Device and Materials Reliability*, pp. 3-8, 2009.
- [12] R.-P. Vollertsen, G. Georgakos, K. Kolpin, and C. Olk, "A fwlr test structure and method for device reliability monitoring using product relevant circuits," in *International Reliability Physics Symposium (IRPS)*, pp. CA.3.1-CA.3.6, 2015.
- [13] O. D. Restrepo, D. Singh, M. Rabie, P. Paliwoda, and E. C. Silva, "Ab Initio Electrical, Thermal Conductance, and Lorenz Numbers for Advanced CMOS Interfaces," *Transactions on Electron Devices*, pp. 2579-2584, 2022.
- [14] G. Garegnani, V. Fiori, G. Gouget, F. Monsieur, and C. Tavernier, "Wafer level measurements and numerical analysis of self-heating phenomena in nano-scale SOI MOSFETs", *Microelectronics Reliability*, pp. 90-96, 2016.
- [15] A. Roy, "Fabrication and characterization of copper interconnects of line-width down to 100nm using a specially designed phase shift mask", *Microelectronic Engineering*, pp. 152-156, 2014.
- [16] P. Paliwoda, P. P. Manik, D. Singh, Z. Chbili, A. Kerber, J. Johnson, and D. Misra, "Self-heating assessment on bulk finfet devices through characterization and predictive simulation," *IEEE Transactions on Device and Materials Reliability (TDMR)*, pp. 133-138, 2018.
- [17] C. Prasad, L. Jiang, D. Singh, M. Agostinelli, C. Auth, P. Bai, T. Eiles, J. Hicks, C. H. Jan, K. Mistry, S. Natarajan, B. Niu, P. Packan, D. Pantuso, I. Post, S. Ramey, A. Schmitz, B. Sell, S. Suthram, J. Thomas, C. Tsai, and P. Vandervoorn, "Self-heat reliability considerations on intel's 22nm tri-gate technology," *International Reliability Physics Symposium (IRPS)*, pp. 5D.1.1-5D.1.5, 2013.
- [18] R. Aggarwal, L. Jiang, S. Patra, N. Lajo, E. Kabir and R. Kasim, "A Novel Approach for Assessing Impact of Temperature Hot-Spots on Chip-Package Interaction Reliability," *International Reliability Physics Symposium (IRPS)*, pp. 4C.4-1- 4C.4-5, 2022.

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