A 32Gb/s Digital-Intensive Single-Ended PAM-4 Transceiver for High-Speed Memory Interfaces Featuring a 2-Tap Time-Based Decision Feedback Equalizer and an In-Situ Channel-Loss Monitor

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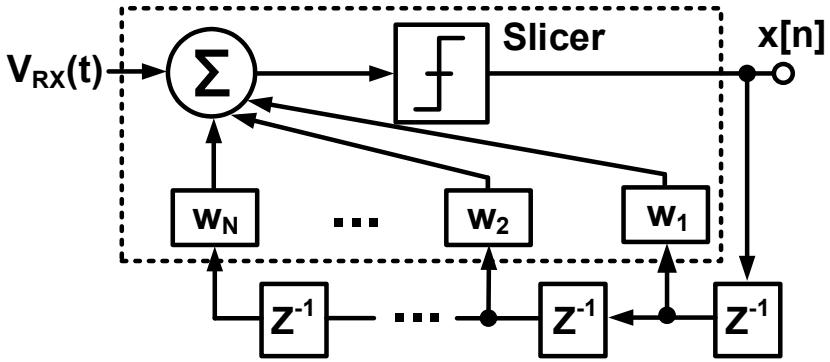
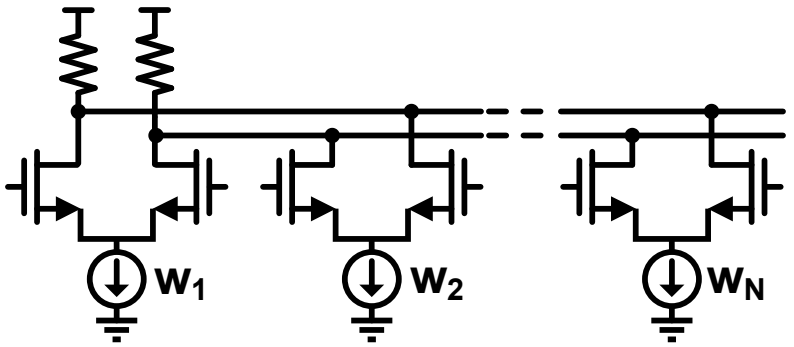
Outline

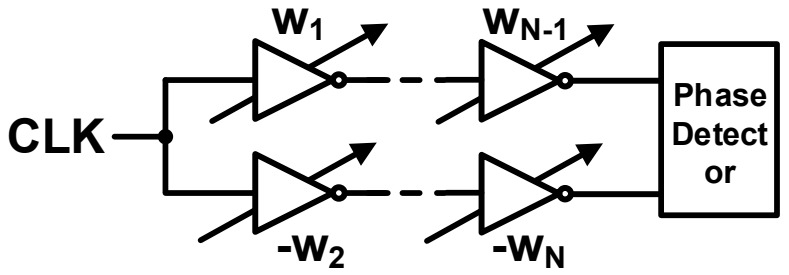
- Introduction
- Time Based PAM-4 Decision Feedback Equalizer
- In-situ Channel Loss Monitor
- 65nm Test Chip Results
- Summary

Voltage-based vs. Time-based DFE

DFE: Decision Feedback Equalization

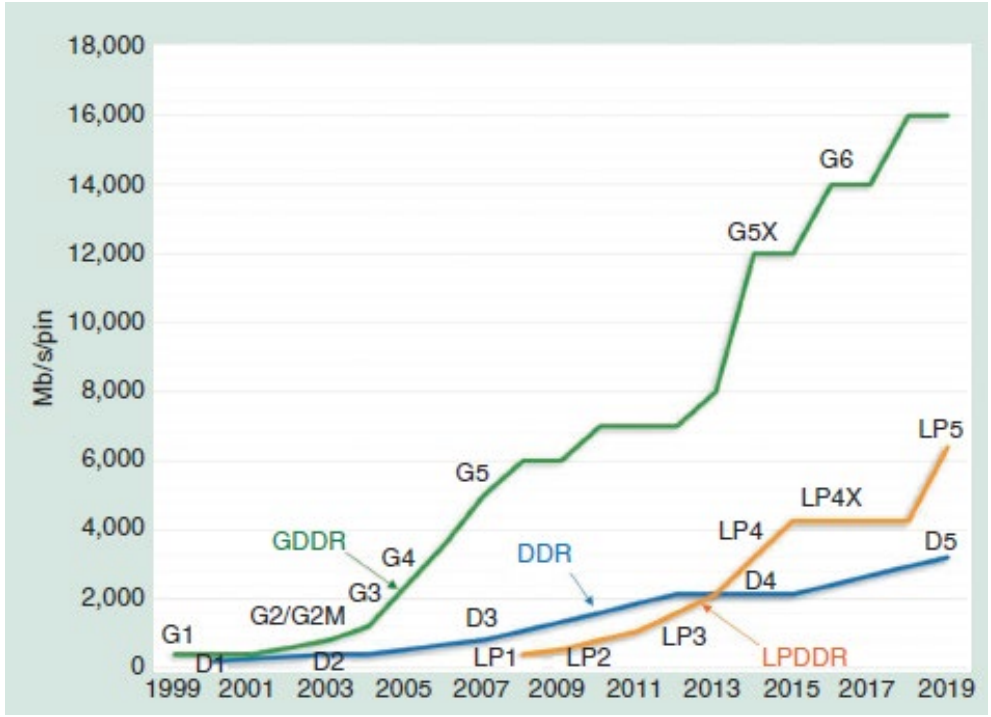


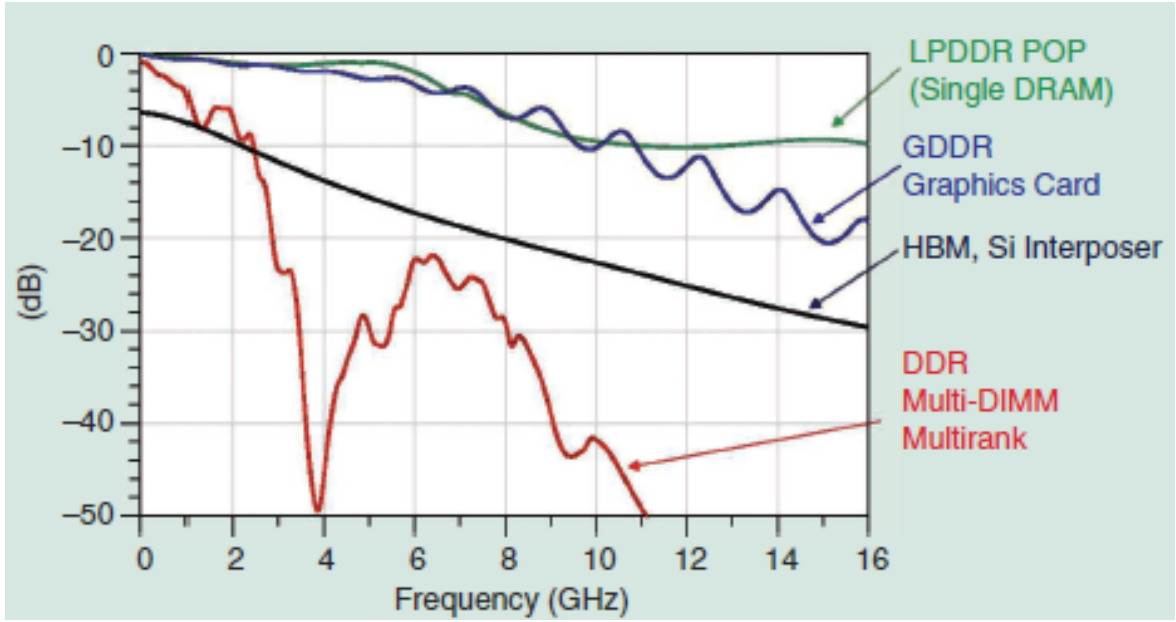




	Voltage-based DFE	Time-based DFE
Circuit	Current mode logic Differential	Inverter delay line Single-ended
Pros	Ultra high speed	Scalable to large number of taps, low power consumption
Cons	Headroom issues, limited taps, large power consumption	Moderate speed

Memory Interface Trends



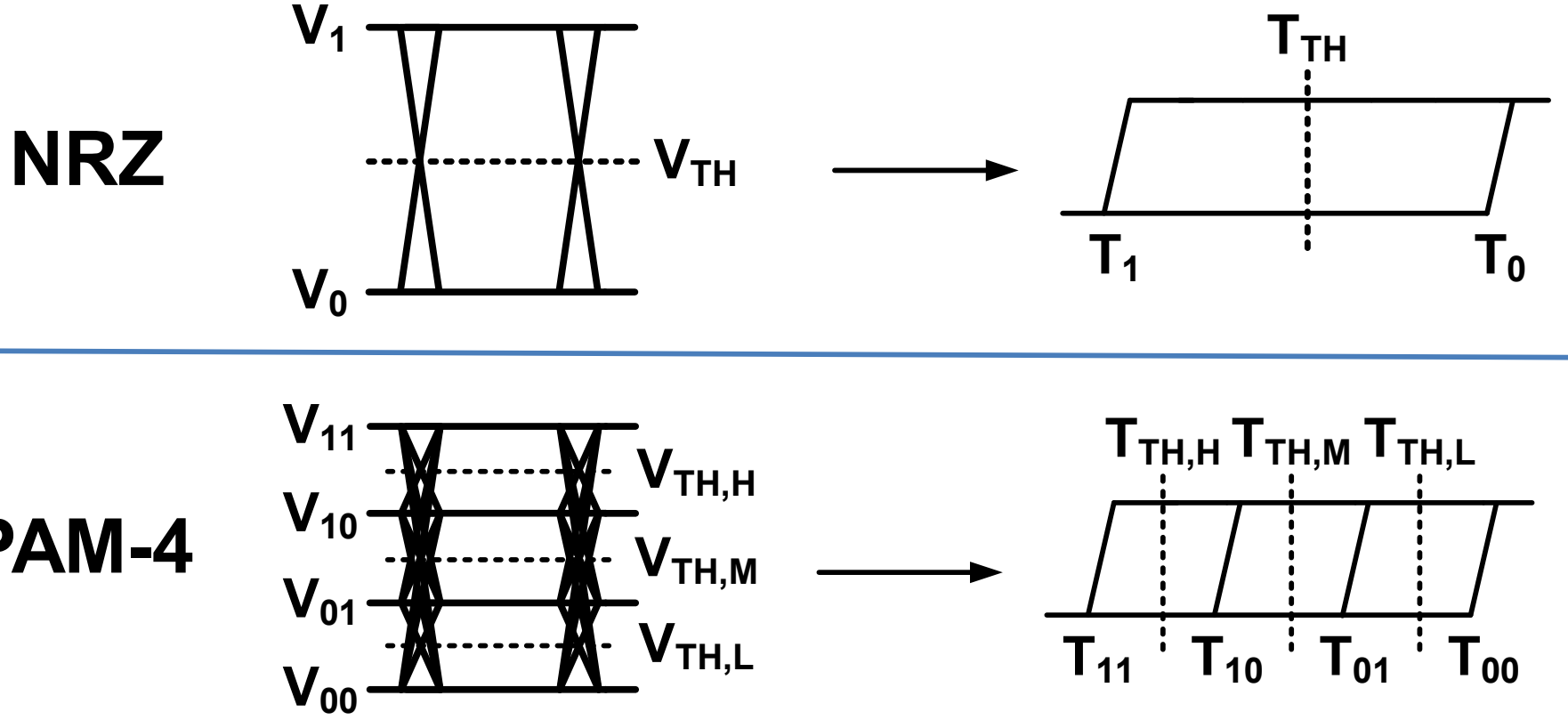


T. Hollis, Solid-State Magazine, 2019

- **Single-ended signaling, lower supply voltage**
- **Data rate higher than 16 Gb/s**
- **Multi drop memory bus with more reflection**

Time-based DFE becoming an attractive alternative

Pulse Amplitude Modulation (PAM)



- **PAM-4 overtaking NRZ but requires more accurate conversion from voltage signal to time delay signal**

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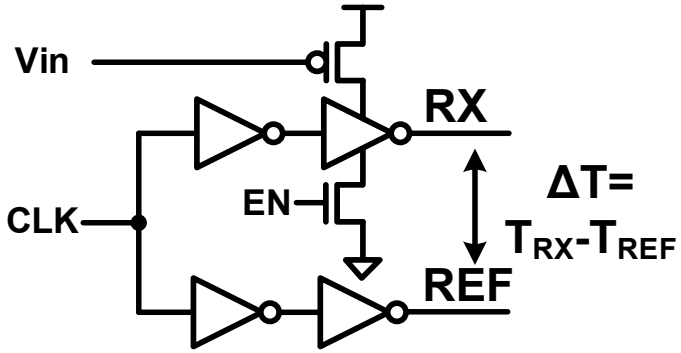
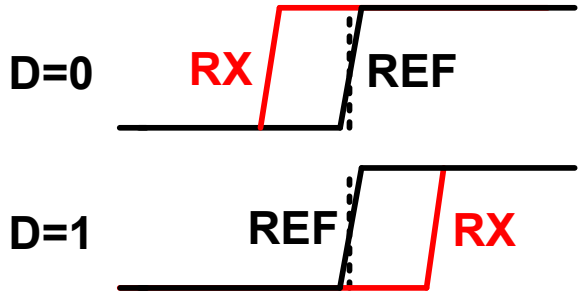
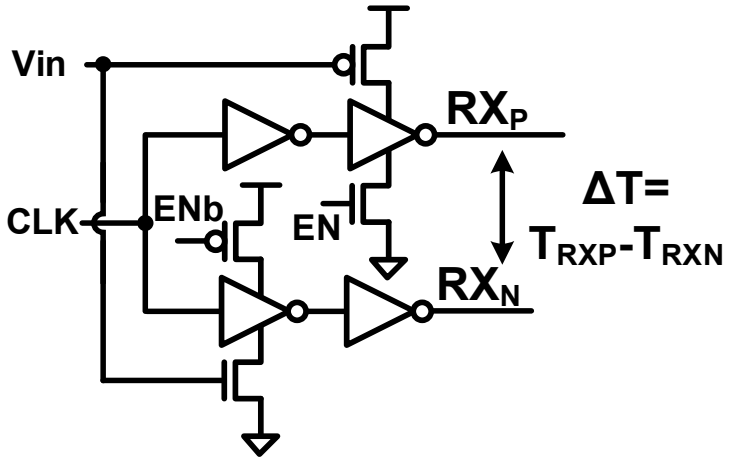
Differential Voltage to Time Converter

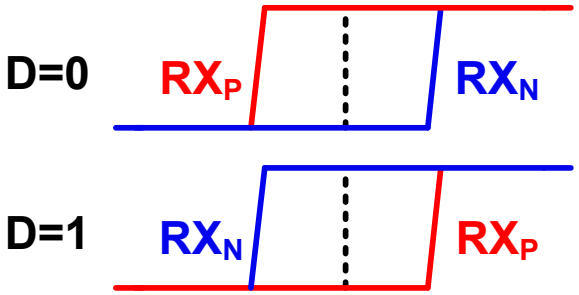
VTC (Prior art)





DVTC (This work)



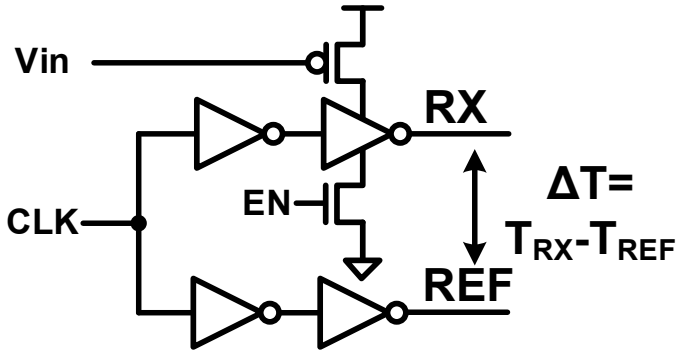


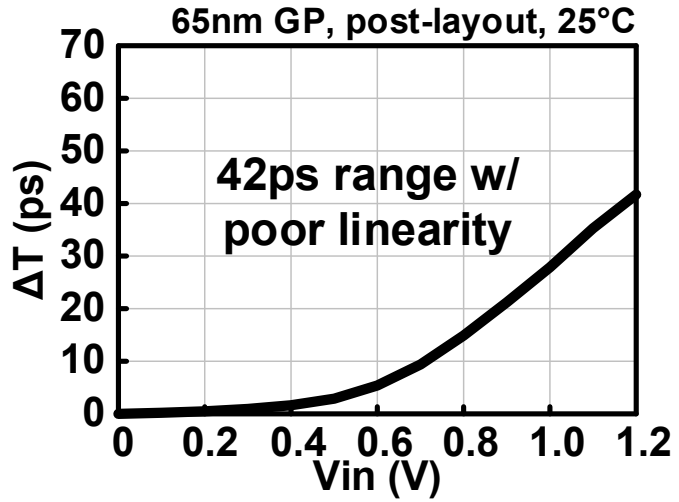
DVTC:
Differential VTC

- **Two path delays change with opposite polarity**
- **Non-linearity cancelled out by subtracting delays**

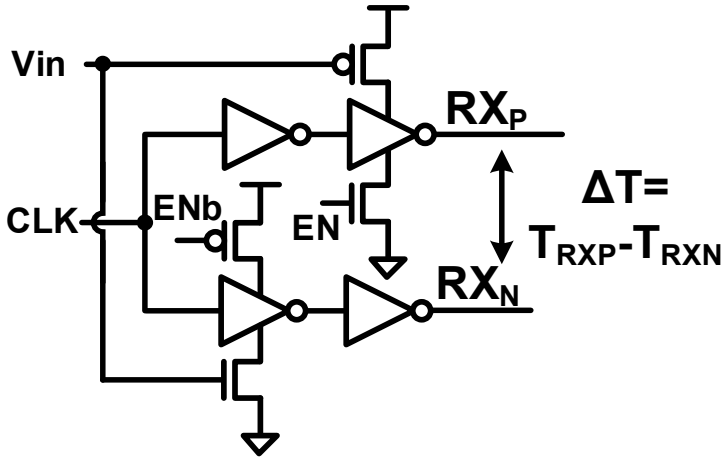
Differential Voltage to Time Converter

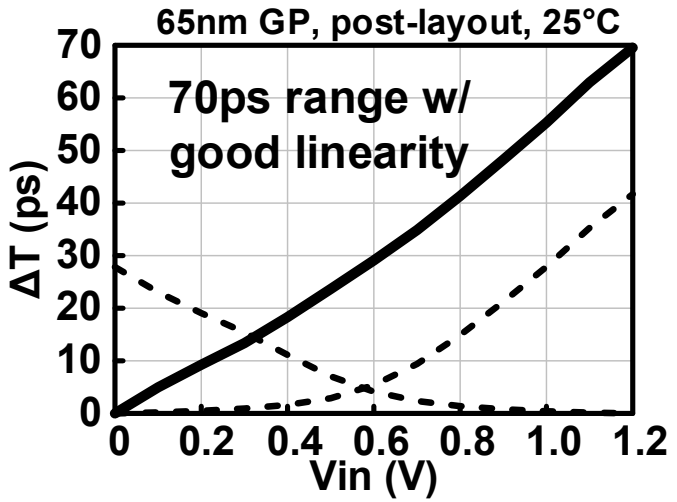
VTC (Prior art)





DVTC (This work)

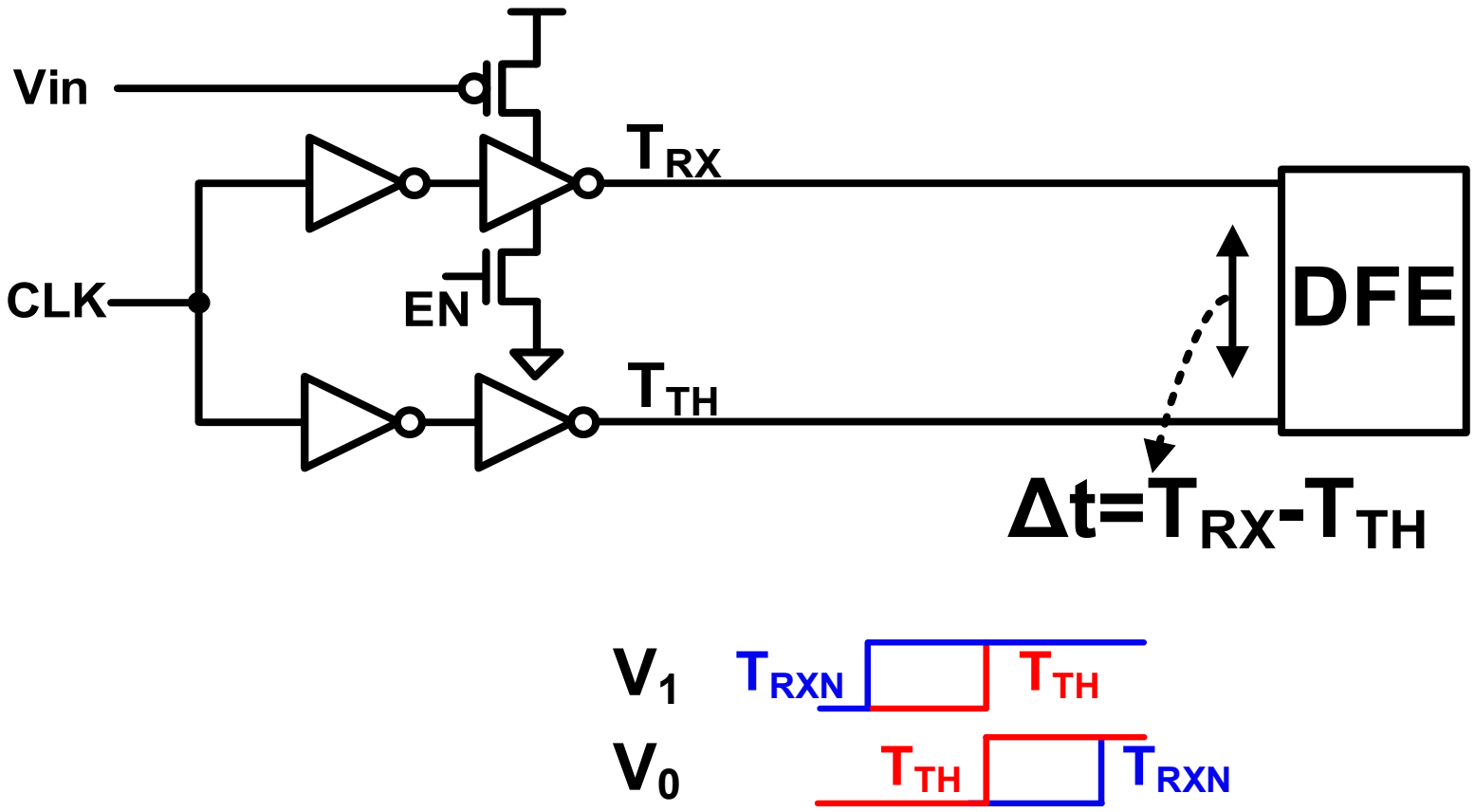




DVTC:
Differential VTC

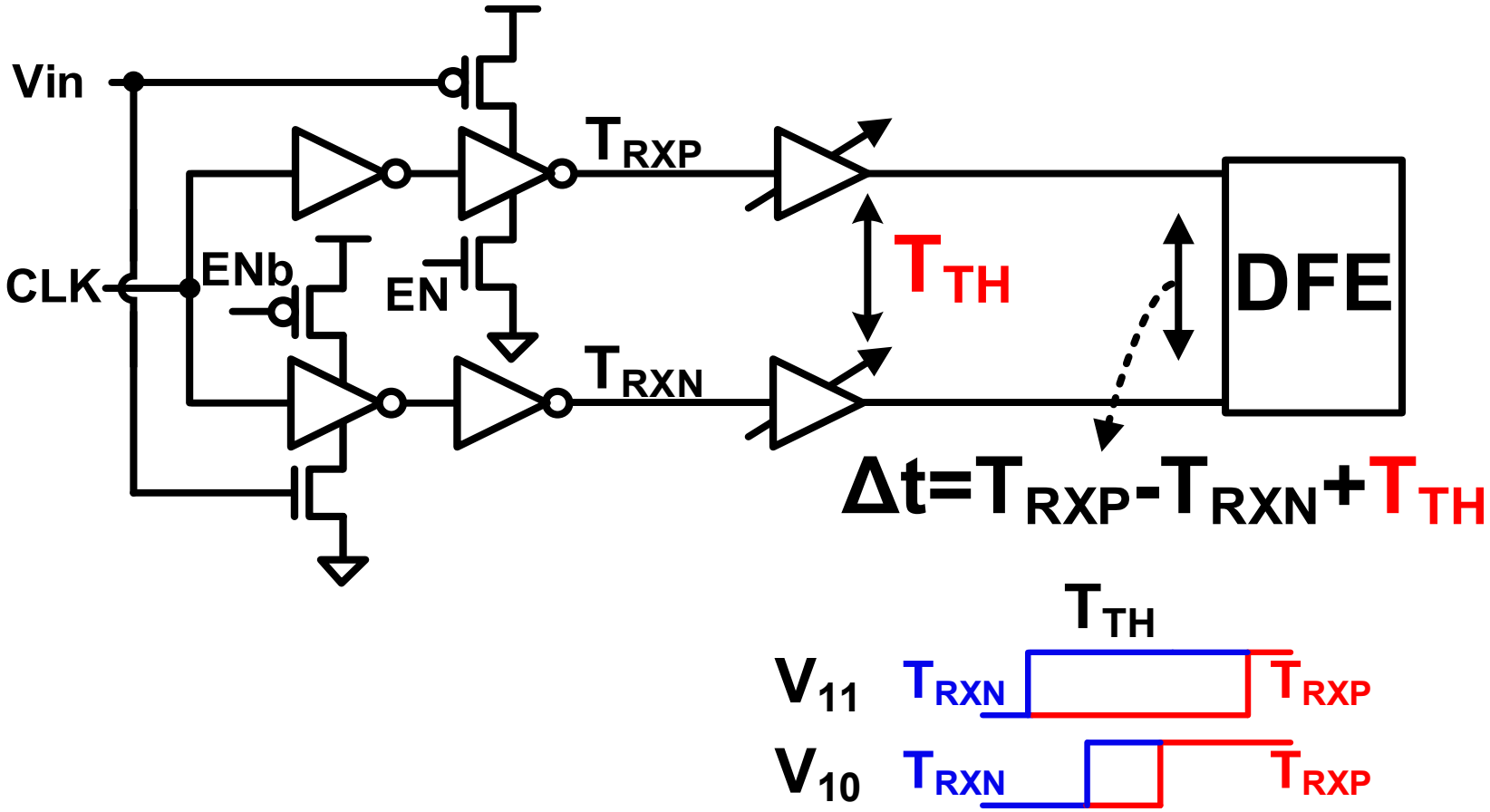
- **Delay range improves from 42ps to 70ps**

NRZ Signal Comparison



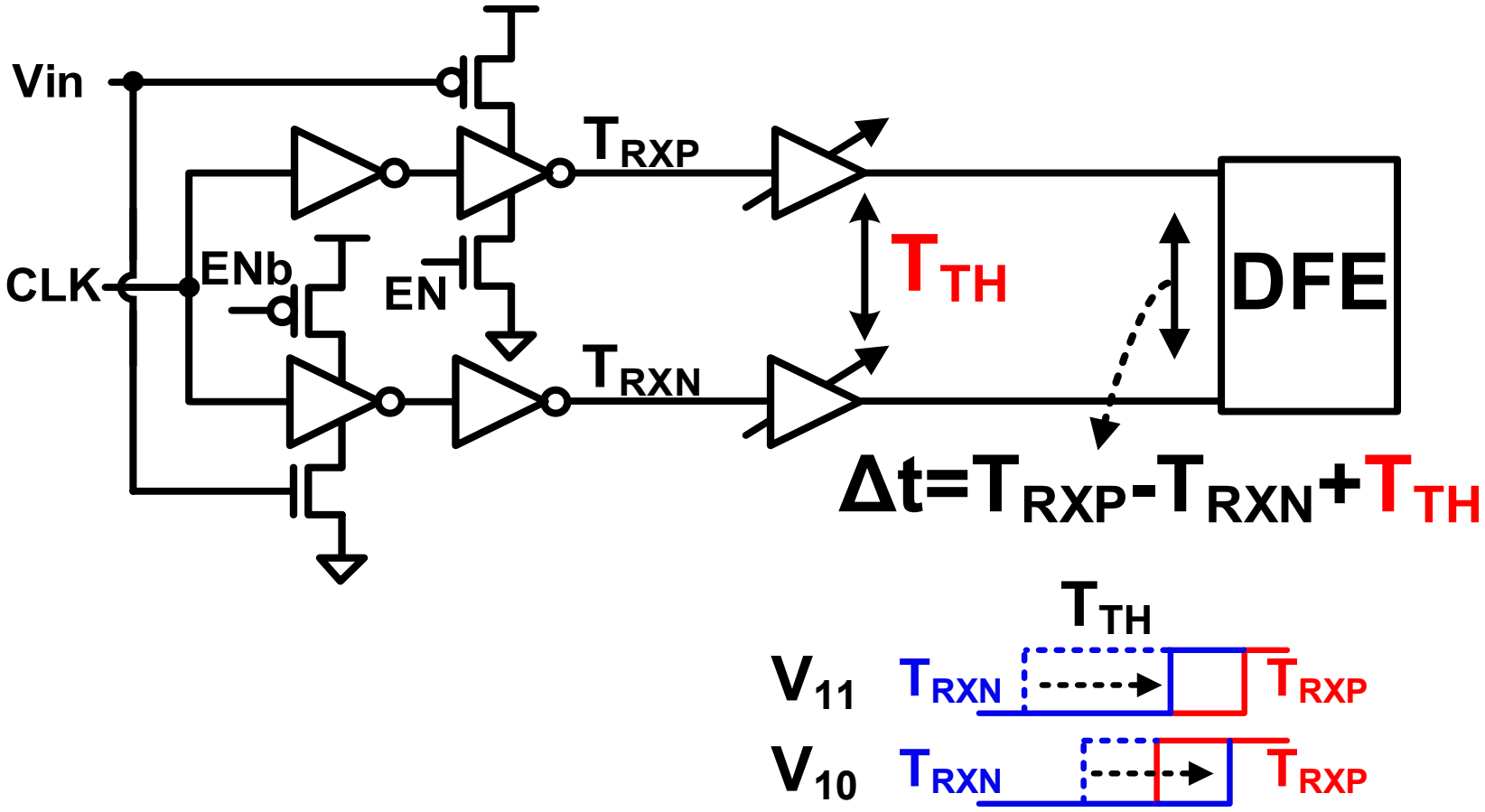
- **Threshold delay generated by VTC in reference delay line**

PAM-4 Signal Comparison



- **Simple buffer can generate the different threshold delays for PAM-4. Separate DAC circuit not required.**

PAM-4 Signal Comparison



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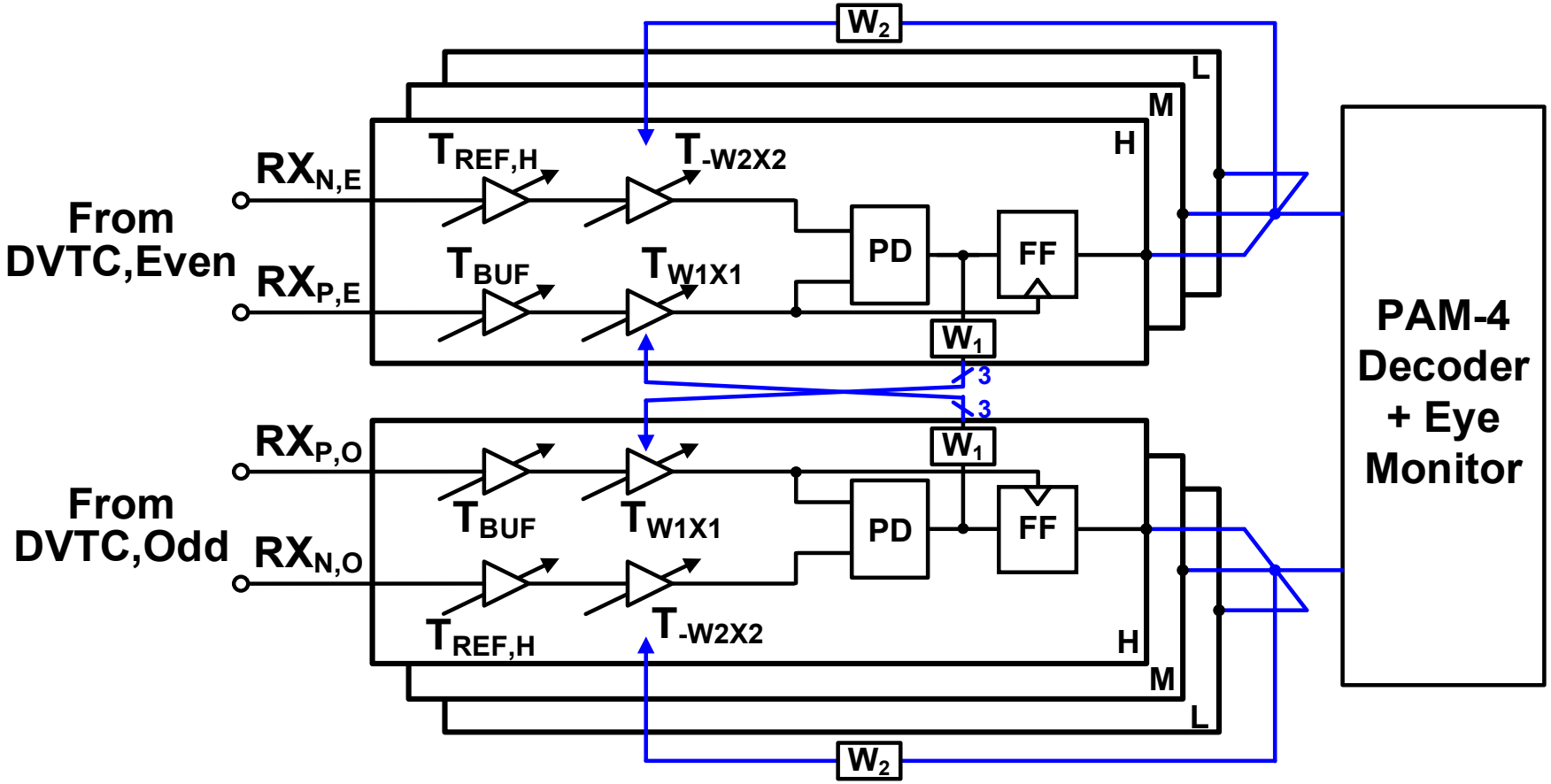
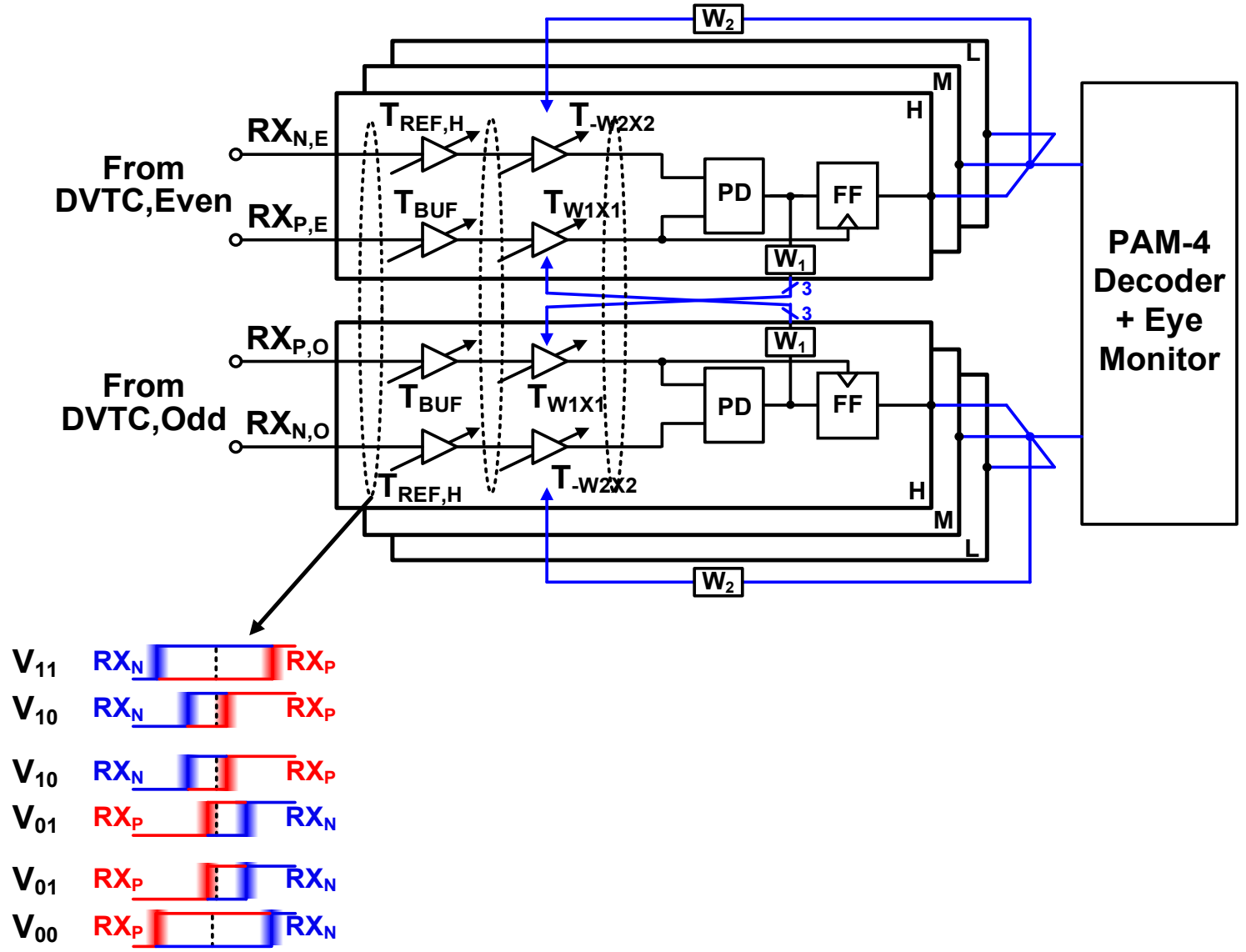
PAM-4 Time-Based Receiver

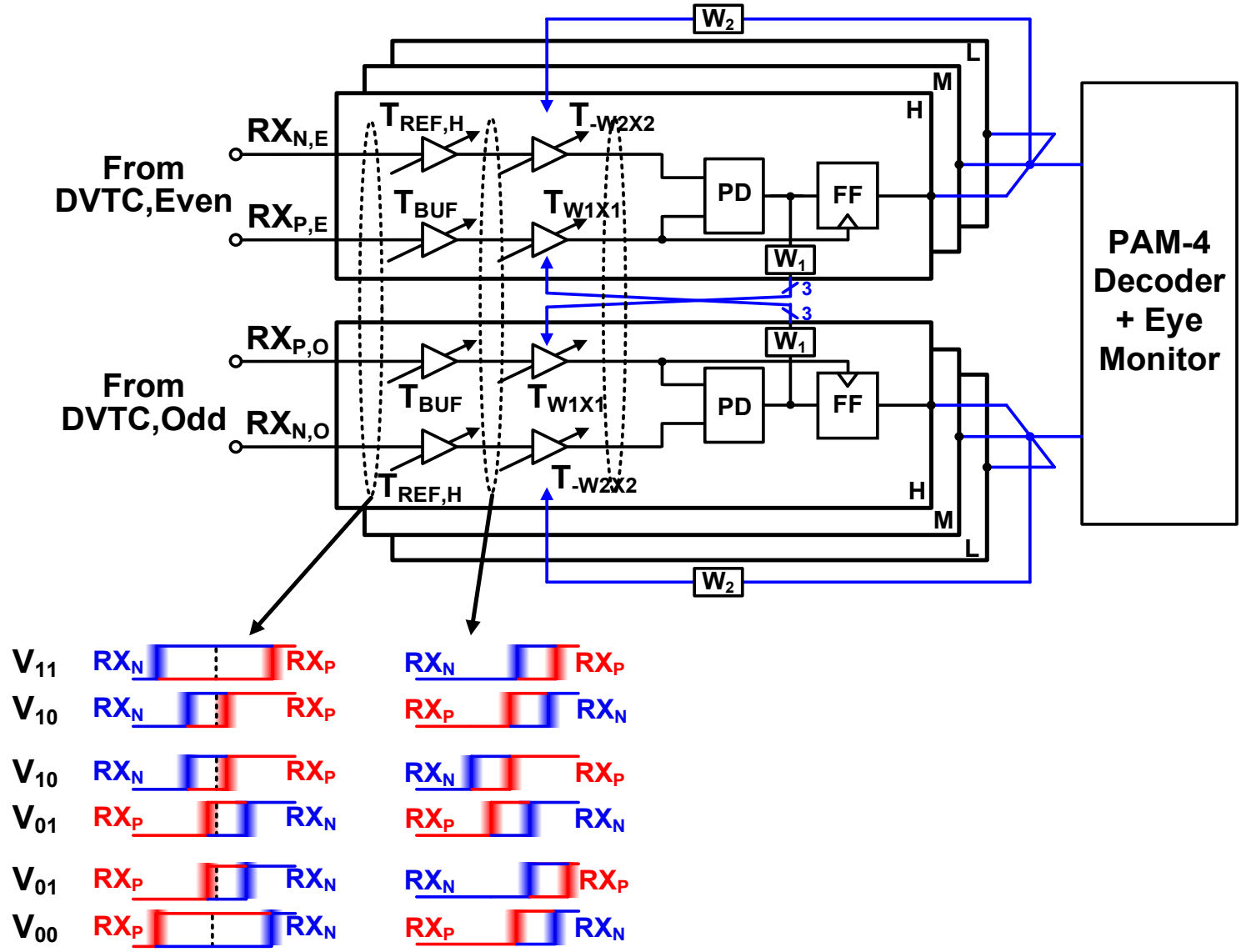


- **Half-rate operation**
- **12 delay lines and 6 phase detectors (PD)**

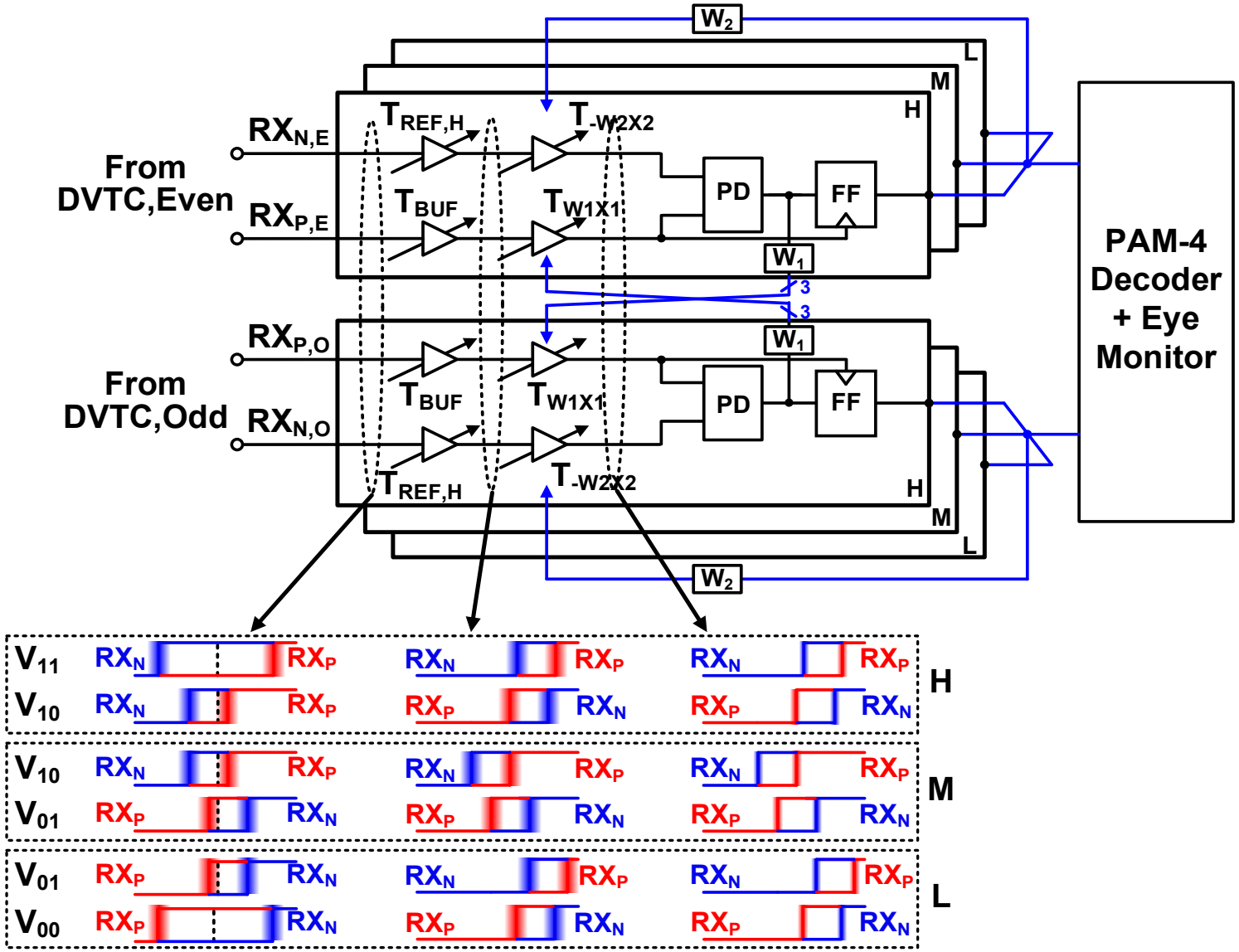
PAM-4 Time-Based Receiver



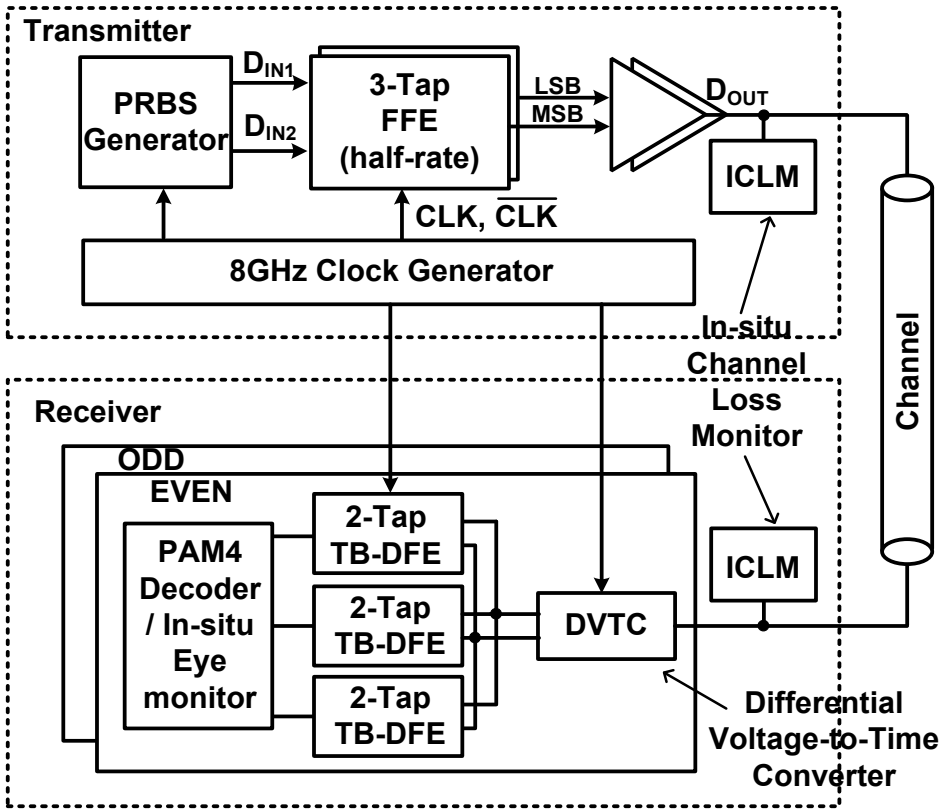
PAM-4 Time-Based Receiver

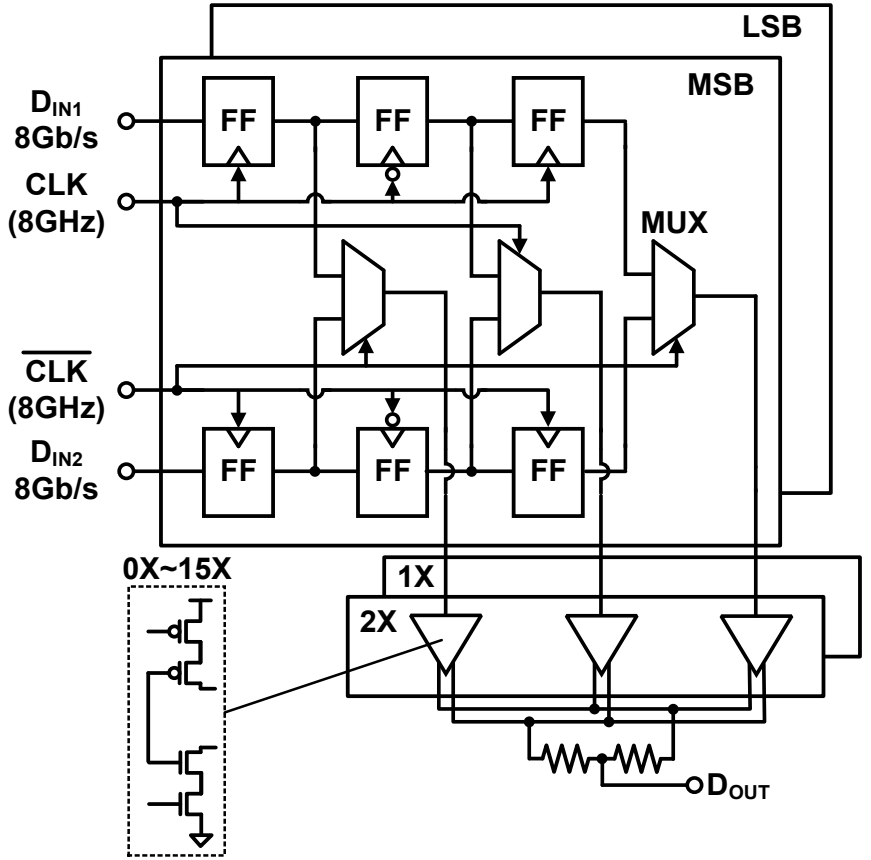


PAM-4 Time-Based Receiver



Test Chip Diagram of PAM-4 Transceiver





- **RX: DVTC, PAM-4 TB-DFE, and BER monitor**
- **TX: PRBS, clock generator, FFE, and driver**
- **In-situ channel loss monitors on both sides**

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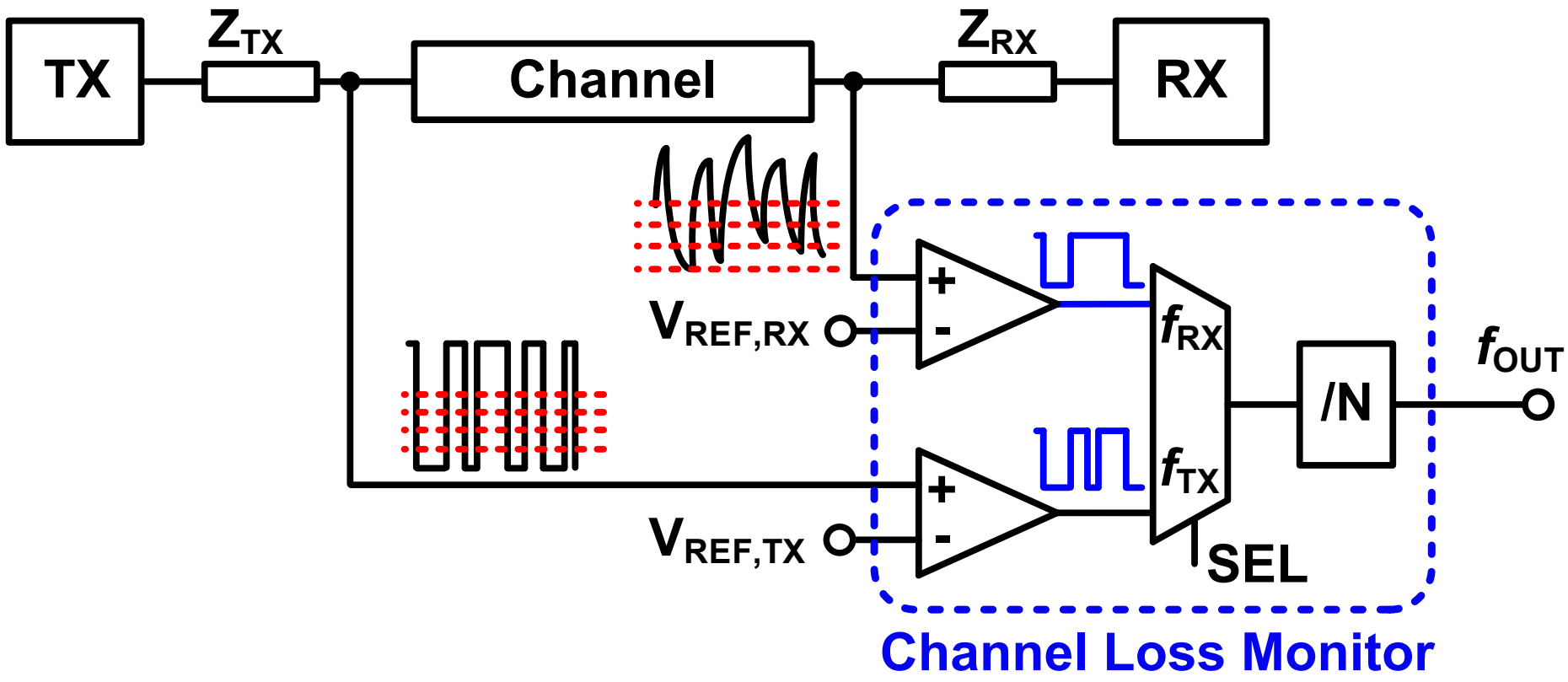
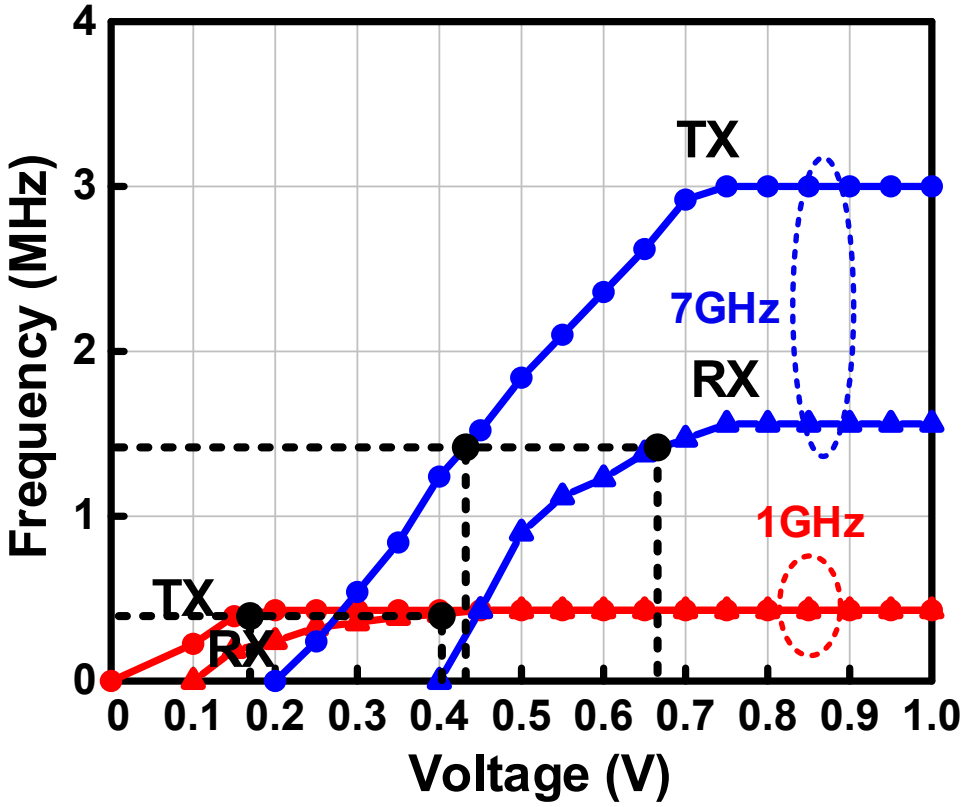
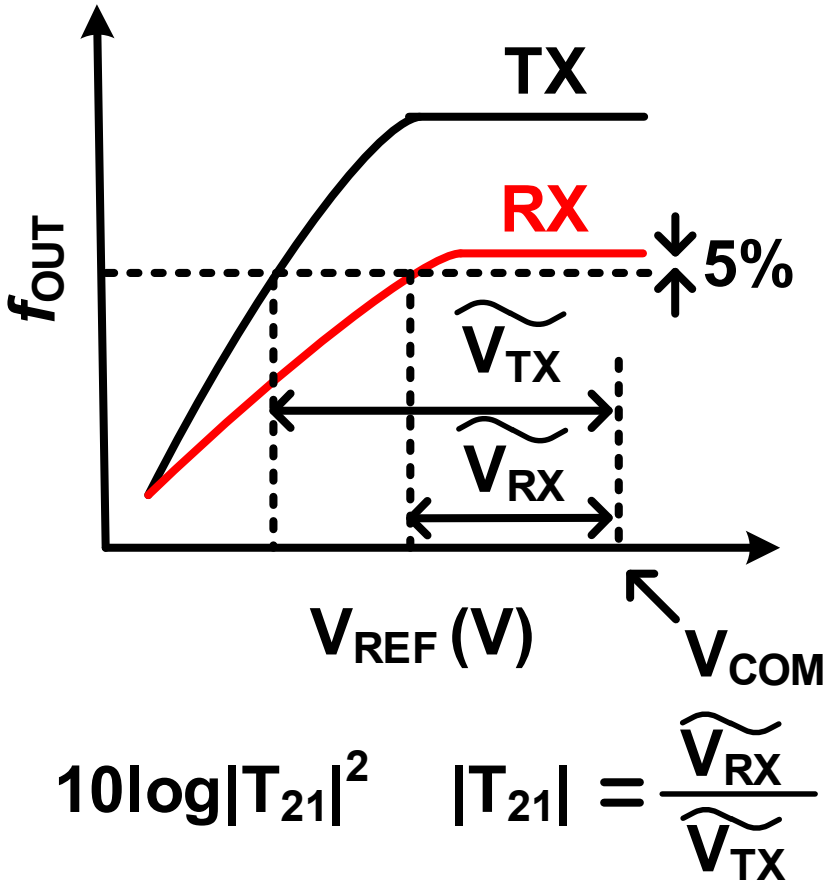
Proposed Channel Loss Monitor



- **Measure the toggling frequency of comparator output while sweeping reference voltage**

Measured Frequency vs. Voltage

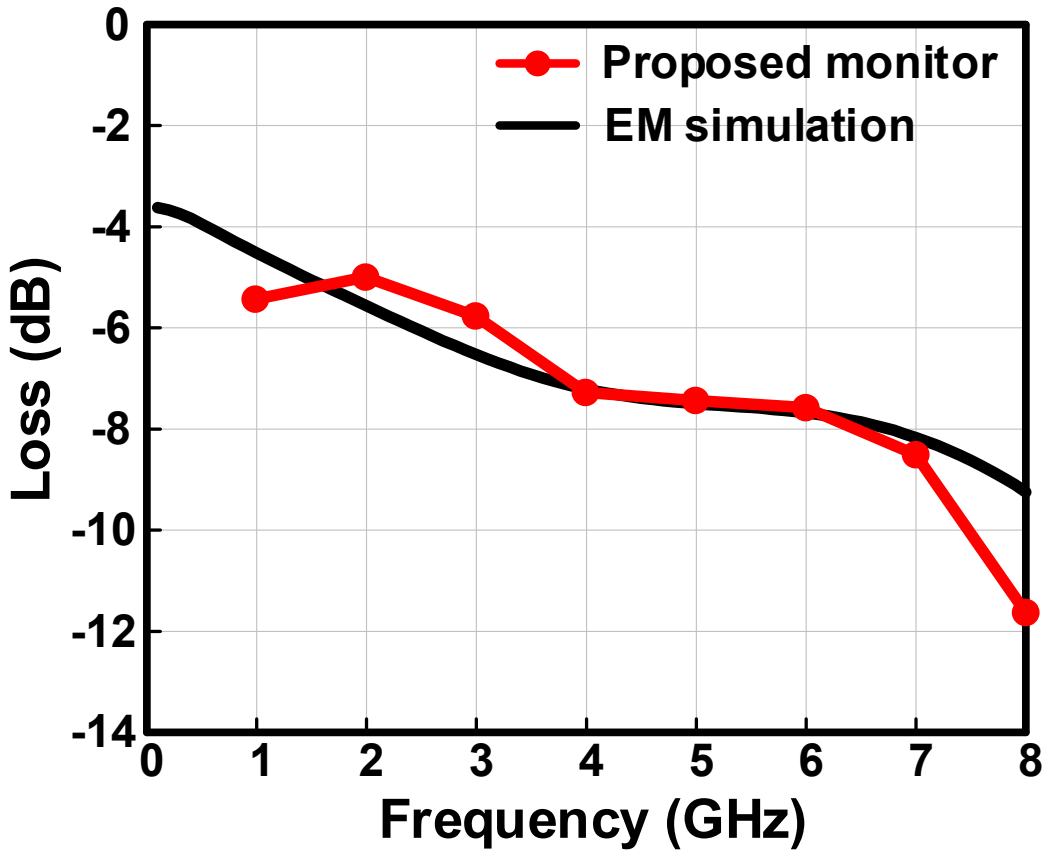




$$10\log|T_{21}|^2 \qquad |T_{21}| = \frac{\tilde{V}_{RX}}{\tilde{V}_{TX}}$$

- **Frequency decreases at higher data rates**

Measured Channel Loss



- **Small discrepancy can be attributed to random digital pattern generated by PRBS (vs. sinusoidal input)**

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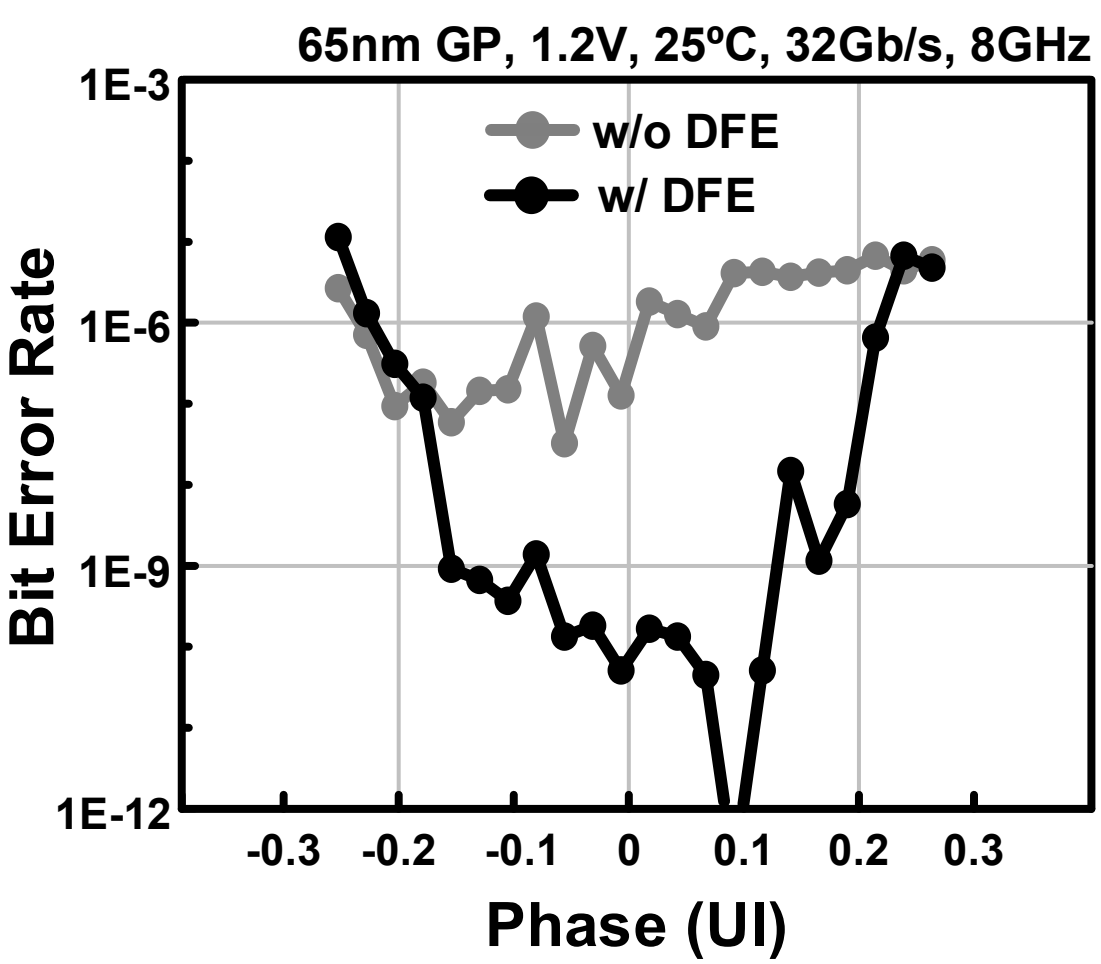
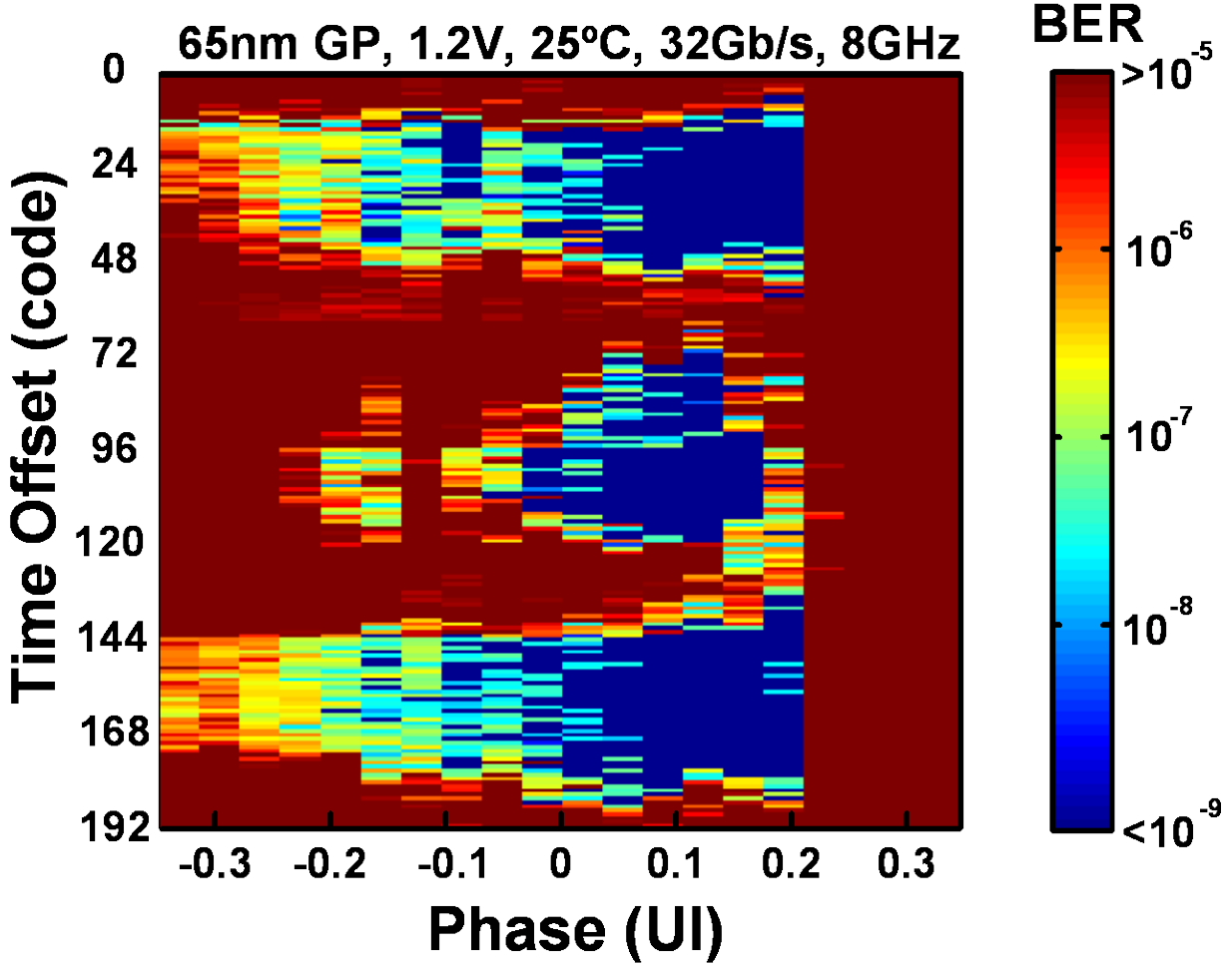
BER Bathtub and Time-Domain Eye Diagram

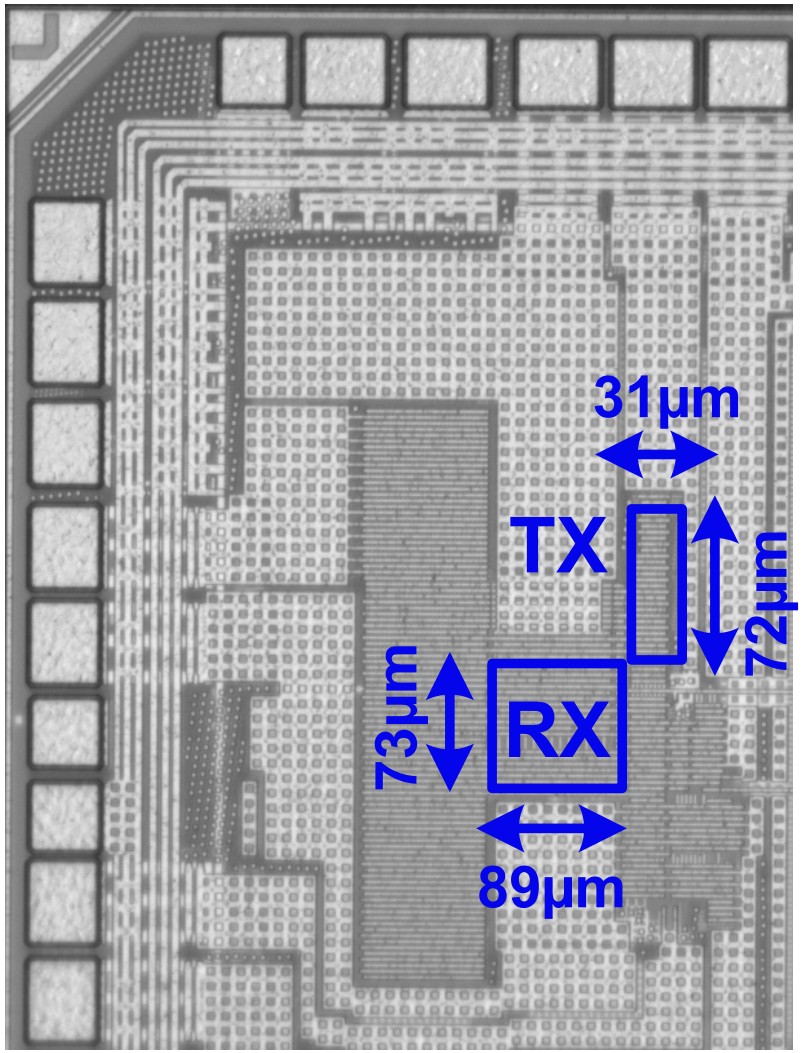




X-axis: Phase (time)

Y-axis: Time offset (time)

Die Photo and Feature Summary



Technology	65nm CMOS
Circuit Area	TX: 31x72µm^2
	RX: 89x73µm^2
VDD	1.2V
Data Rate	32 Gb/s
Channel Loss	11.6dB@8GHz
BER	<10^{-12}
Power Efficiency	0.97 pJ/b

Performance Comparison Table

	JSSC'14 [1]	ISSCC'19 [2]	ISSCC'16 [3]	JSSC'18 [4]	This work
Signaling	Duobinary	PAM-3	Muti-Band	NRZ	PAM-4
Single/Differential	Single-Ended	Single-Ended	Differential	Single-Ended	Single-Ended
RX Circuit Type	Voltage-Based	Voltage-Based	Voltage-Based	Time-Based	Time-Based
RX Equalization	1-Tap DFE	1-Tap DFE	Self-Equalization	2-Tap DFE	2-Tap DFE
Data Rate	7 Gb/s	27 Gb/s	10 Gb/s	12.5 Gb/s	32 Gb/s
Technology	65nm	28nm	28nm	65nm	65nm
Voltage	1.05V	0.6V	1.2V	0.8V	1.2V
Channel Loss	0.8dB@3.5GHz	20mm	6dB@6GHz	14dB@6.25GHz	11.6dB@8GHz
BER	<1E-12	<1E-12	<1E-12	<1E-12	<1E-12
TRX Area	0.0333 mm^2	0.0135 mm^2	0.01 mm^2	0.0094 mm^2	0.009 mm^2
TRX Power Efficiency	0.56 pJ/b	1.03 pJ/b	0.95 pJ/b	0.49 pJ/b	0.97 pJ/b

[1] S. Lee, *et al.*, JSSC, 2014. [2] H. Park, *et al.*, JSSC, 2019. [3] W. Cho, *et al.*, ISSCC, 2016. [4] I. Yi, *et al.*, JSSC, 2018.

Summary

- Digital-intensive PAM-4 time-based DFE
- Differential voltage-to-time converter with enhanced linearity and dynamic range
- In-situ channel loss monitor