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Understanding the Key Parameter Dependences Influencing the Soft-Error Susceptibility of Standard Combinational Logic

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***Abstract*—This work presents neutron radiation induced Soft Error Rate (SER) statistics and detailed analysis thereof, revealing a multitude of circuit parameters impacting the soft-error susceptibility of standard combinational logic in advanced CMOS nodes. A high density array-based soft-error characterization vehicle is presented, featuring standard logic gate chains of varying lengths. Neutron irradiation data obtained from gate variants employing devices with distinct channel widths and threshold voltage flavors is analyzed at multiple supply voltages, ranging from nominal down to near-threshold. Supplemented with first-order simulations, measured SER cross-section results obtained from test structures implemented in a 65nm planar CMOS technology node reveal the complex interplay between factors such as supply voltage, node capacitance, restore current ($I_{RESTORE}$), gate topology and logic chain length responsible in contributing towards the collective soft error susceptibility of a standard gate type, which constitutes the main focus of this work. In addition, the easy process portability of the proposed macro is demonstrated through implementation in a 16nm FinFET process.**

***Index Terms*— Circuit reliability, combinational logic, neutron irradiation, single event effects, single event transient, single bit upset, soft error rate, radiation effects.**

I. Introduction

With the miniaturization of feature sizes leading to increased on-chip device densities together with the reduction in supply voltages, radiation induced soft-errors continue to remain a critical reliability concern even in FinFET technologies where the per-device SER is known to be significantly lower than that of planar CMOS [1-3]. Single Event Transients (SETs) in combinational logic now become particularly unsettling, as the probability of a narrower pulse getting latched in a sequential element is amplified due to the improvement in circuit delays with scaling [4-5]. Understanding the key parameter dependences influencing the soft-error susceptibility of a logic block from a design perspective, is therefore a quintessential step towards engineering robust systems for mission critical applications.

To this end, we introduce a soft-error characterization vehicle featuring SER and SET pulse width measurement capabilities in the first part of this work. The proposed design is readily scalable and employs a regular, unit cell based layout featuring standard logic gate variations, enabling circuit designers to directly utilize statistically meaningful test data pertinent to specific logic gate types / path depths, thus obviating the need for indirect translations from other inaccurate representations ([6-7]). The test-circuit overhead is small, with the closely embedded measurement circuitry employing local sampling to avoid any pulse-width distortion effects [8], along with the flexibility of fine tuning the pulse width measurement resolution post-silicon. The second part of this work discusses the SER cross-section statistics mined using the proposed macro, from neutron irradiation experiments conducted at the Los Alamos Neutron Science Center (LANSCE). Multiple dependences, existing at the device, individual gate and the logic block level, as well as their intricate interaction impacting SER are explored and analyzed. The impact of logic chain length induced electrical masking / pulse quenching effect [9-16] is broken down in detail, revealing its severity on a chosen gate topology, relative drive strength and the operating voltage. The overall discussion is targeted towards developing an understanding of the factors contributing to SER from a circuit design perspective.

II. Design Idea And Test Chip Implementation

A. Proposed Concept

Fig. 1 (top) conceptually illustrates the proposed logic soft-error characterization macro. The design consists of varying chain lengths of standard combinational logic gates, essentially the Devices-Under-Test (DUTs) feeding a NAND-NOR chain functioning as clock to a string of serially connected D-Flipflops (DFFs). The NOR gates in the chain together with the DFFs have a slightly higher supply voltage (VDDH) as compared to the NAND gates in the chain and the DUTs (VDDL). This arrangement causes the drive strengths of the stacks comprising the NAND-NOR clock chain to increase, with the consequence that any transient errors entering the clock chain via the DUTs experience a controlled, consistent shrink rate as they propagate downwards along the chain, graphically illustrated in Fig. 1. The transient while travelling along the chain also clocks the string of serially connected DFFs in

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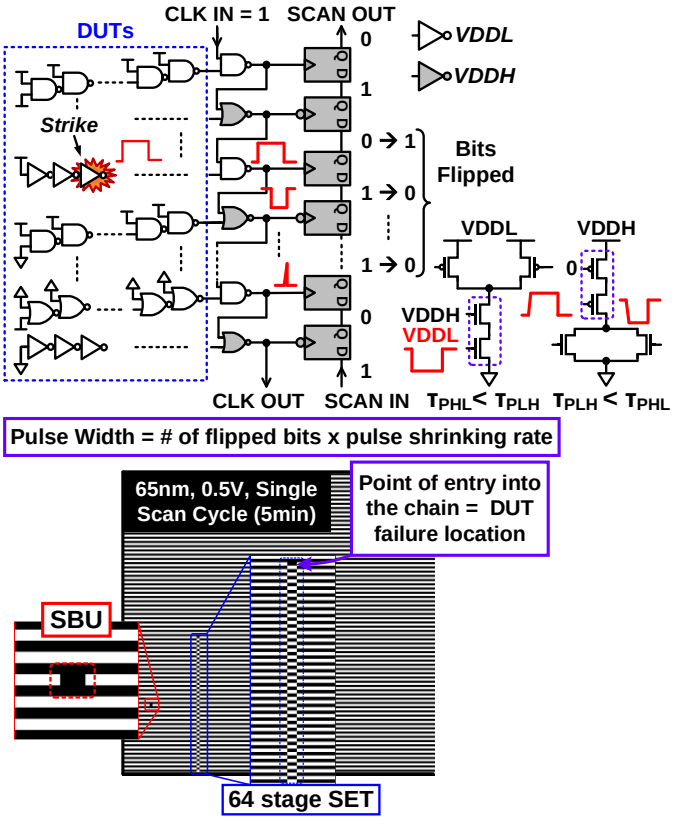


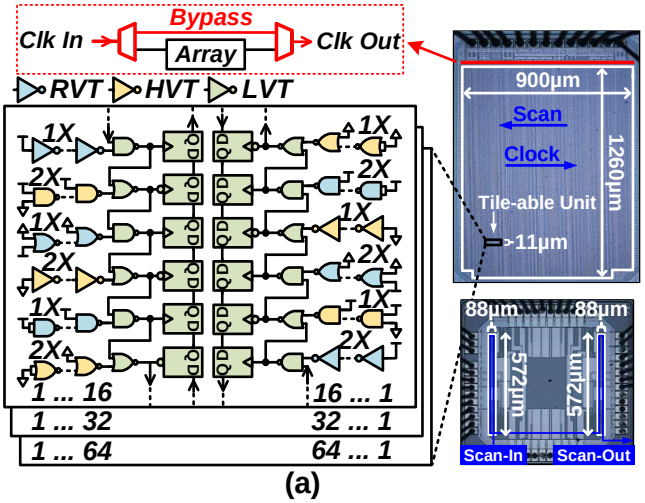
Fig. 1: Graphical illustration of the proposed concept (top) and array bit-map (bottom) showing an SET and a Single Bit Upset (SBU). The shifted portion of flip-flop bits in the scanned out data reveals the SET injection point in the chain as well as the pulse width information.

succession, which have been routed in the direction opposite to the clock to prevent any hold time violations. This causes the checkerboard sequence initially programmed into the flops to progressively shift up by one bit, until the transient pulse-width itself becomes less than the minimum detectable pulse width of the DFFs, following which the initially programmed bit sequence remains intact for the subsequent flops. Local sampling of the transient by the closely embedded DFFs prevents any possibility of pulse-width modulation in the test structure. Furthermore, the measurement circuit supply (VDDH) in conjunction with the DUT supply (VDDL) provides the designer with a differential, high resolution post-silicon tuning knob, independent of the technology used for implementation. Unlike the back sampling chain technique [7], a single on-chip matched path (Fig. 2) consisting of a MUX De-MUX unit provides for a robust, one-time calibration routine for determining the net pulse contraction for specific values of the two supply voltages, while also cancelling any unwanted (routing, I/O, on-board interconnect) delays. This calibration routine was performed prior to irradiation for the DUT voltages of interest (VDDL), and the corresponding VDDH values were tuned such that the resulting stage delay values were appreciably higher compared to the measured standard deviation in the per stage delay values obtained from multiple boards. This ensured that any variation induced differences in the per stage shrink rate were insignificant compared to the stage delay itself and that the pulse shrinking was consistently controllable within tolerable margins for the transient error studies.

Fig. 1 (bottom) shows the experimentally obtained array bit map corresponding to a single scan run highlighting the SET, manifested as a trail of shifted DFF bits with the point of entry into the NAND-NOR chain and the end points demarcated by consecutive '1's or '0's and the single bit upset (SBU), manifested as an isolated bit flip. The collective failure location statistics obtained from thousands of such scanned bit maps at multiple supply voltages constitute the SER specifics for the different DUT types, which is the focus of this work. To summarize, the proposed characterization vehicle presents a highly scalable solution, offers pico-second order post silicon resolution trimming, employs local sampling to avoid any pulse width distortion, and facilitates statistically meaningful characterization of both SER and SET events for the relevant circuits of interest.

B. Implementation Specifics

Fig. 2 presents the test chip die micrographs and the implementation specifics. The circuit architecture is based on a unit tile-able cell, schematically illustrated for the 65nm implementation in Fig 2(a), consisting of the three standard logic gate types with both the PMOS and NMOS devices identically sized: either 1X or 2X and implemented in two V_{TH} flavors: Regular V_{TH} (RVT) or High V_{TH} (HVT) leading to total



Process	65nm GP CMOS
Core VDD	1.0V
Irradiation VDD	0.45V – 1.0V
Core + Test Area	1.26mm x 0.9mm
Gate Count	0.53M
Device Widths	120nm(1X), 240nm (2X)
Gate Flavors	RVT, HVT
Chain Lengths	16, 32, 64 Total = 16,272

Process	16nm FinFET
Core VDD	0.8V
Irradiation VDD	0.4V
Core + Test Area	572µm x 177µm
Gate Count	0.419M
Number of Fins	2 Fins (1X), 4 Fins (2X)
Gate Flavors	RVT, HVT
Chain Lengths	INV = 128, NAND/NOR = 96

(b)

Fig. 2: (a) Die micrographs together with the schematic illustration of the unit tile-able cell (b) 65nm and 16nm feature implementation summaries.

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12 unique chains in 65nm and 16nm, with unit cells of varying chain lengths: 16, 32 and 64 distributed uniformly to cover the complete die area for the 65nm implementation. Non-minimum sized Low V_{TH} (LVT) devices were used to improve the NAND-NOR chain and DFF resiliency to soft-errors. Presented later in Fig. 6, irradiation results on a dummy version comprising only the NAND-NOR chain and DFFs show negligible soft errors in the read out circuit.

The 16nm version consists of chains of fixed lengths: 128 for Inverters (INV) and 96 for NAND and NOR gates and is a demonstration of the easy process portability of the proposed design-concept. With a negligible test area overhead, the design can be easily accommodated in constrained spaces making it ideal as a scribe line test-structure, for potential use as a technology characterization vehicle. Two isolated arrays can be tiled together simply by daisy chaining the scan and clock, as can be seen from the 16nm die micrograph. Furthermore, the I/O requirements for implementing the design are also modest, limited to a total of six pads.

III. Neutron Test Setup

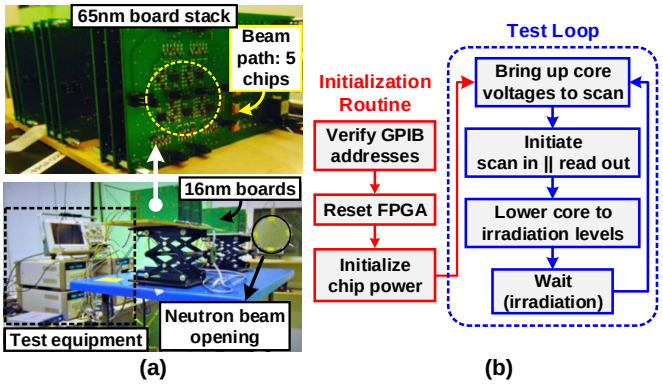

Fig. 3: (a) Neutron testing details at LANSCE and (b) FPGA based test-flow.

As shown in Fig. 3 (a), nine 65nm boards and five 16nm boards were stacked vertically and subjected to spallation neutron beam irradiation. Each 65nm board consists of 5 chips (total 45 chips, 24M gates) placed within a beam diameter of 2" while each 16nm board has one chip (2M gates). The chips on each board are serially connected through a single scan data and single scan clock signal. The chips were exposed to a neutron beam for five effective days. The beam energy ranged between 1.38 - 750MeV while the average beam flux was 2.03×10^6 neutrons/cm^2/sec.

Fig. 3 (b) shows the FPGA based control used for digital I/O (DIO). Following a one-time initialization procedure, a checkerboard map (752Kbits) was written to all 50 chips simultaneously while reading out the stored data in parallel. This was then followed by irradiation for 5 minutes, with the cycle continuously looped.

IV. Technology Analysis

In this section, we present simulation results of key 65nm circuit metrics, insightful in understanding the SER data shown in section V. These simulations were performed on the Typical-Typical (TT), Fast-Fast (FF) and the Slow-Slow (SS) process corners, however, the results presented in this section correspond to the TT process corner, as they were found to correlate well with the measured data trends.

A. Restore Current Simulations

Fig. 4 presents the simulated transistor restore current $I_{RESTORE}$ for the different pull-up network (PUN) and pull down network (PDN) topologies corresponding to standard gate variants implemented in the 65nm test-chip. Due to the low mobility of p-channel devices in this process, the PUNs exhibit 0.41~0.59X lower drive current compared to their PDN counterparts. Stacked topologies exhibit lower $I_{RESTORE}$, with the effect compounded at low voltages (0.45V, 0.5V) and for PMOS devices. From Fig. 4, it can also be observed that the HVT devices are especially vulnerable at low voltages, with even the 2X sized devices displaying lower drive currents compared to the 1X RVT versions. As the supply voltage increases beyond half VDD, the increase in gate overdrive offsets this effect, with the 2X HVT flavors now exhibiting a higher drive current than 1X RVT flavors as expected. The above observations will be useful in analyzing the experimentally obtained results, discussed in subsequent sections.

B. Critical Charge Analysis

Fig. 5 details the simulated critical charge (Q_{CRIT}) trends,

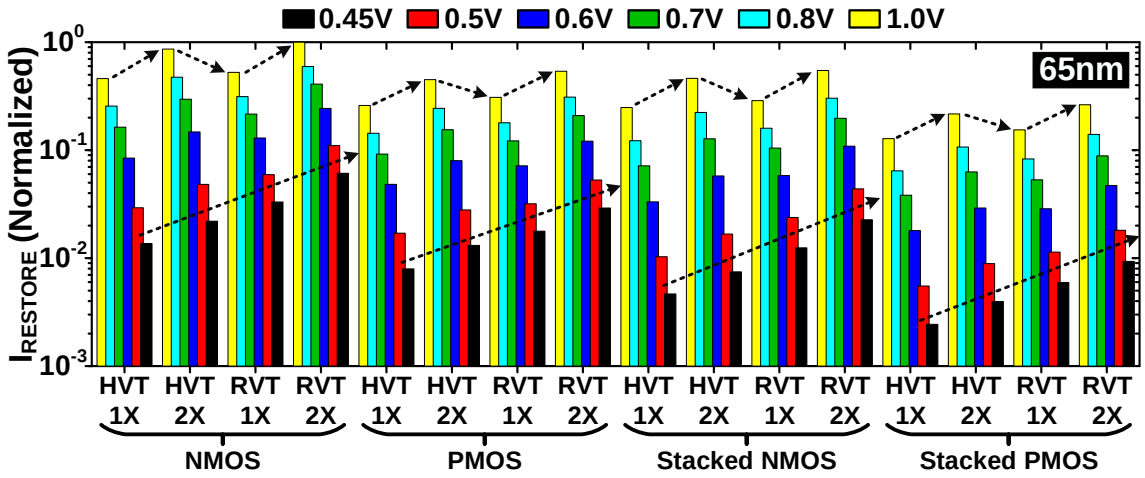

Fig. 4: Simulated $I_{RESTORE}$ for PUN and PDNs for the different gate topologies and different supply voltages.

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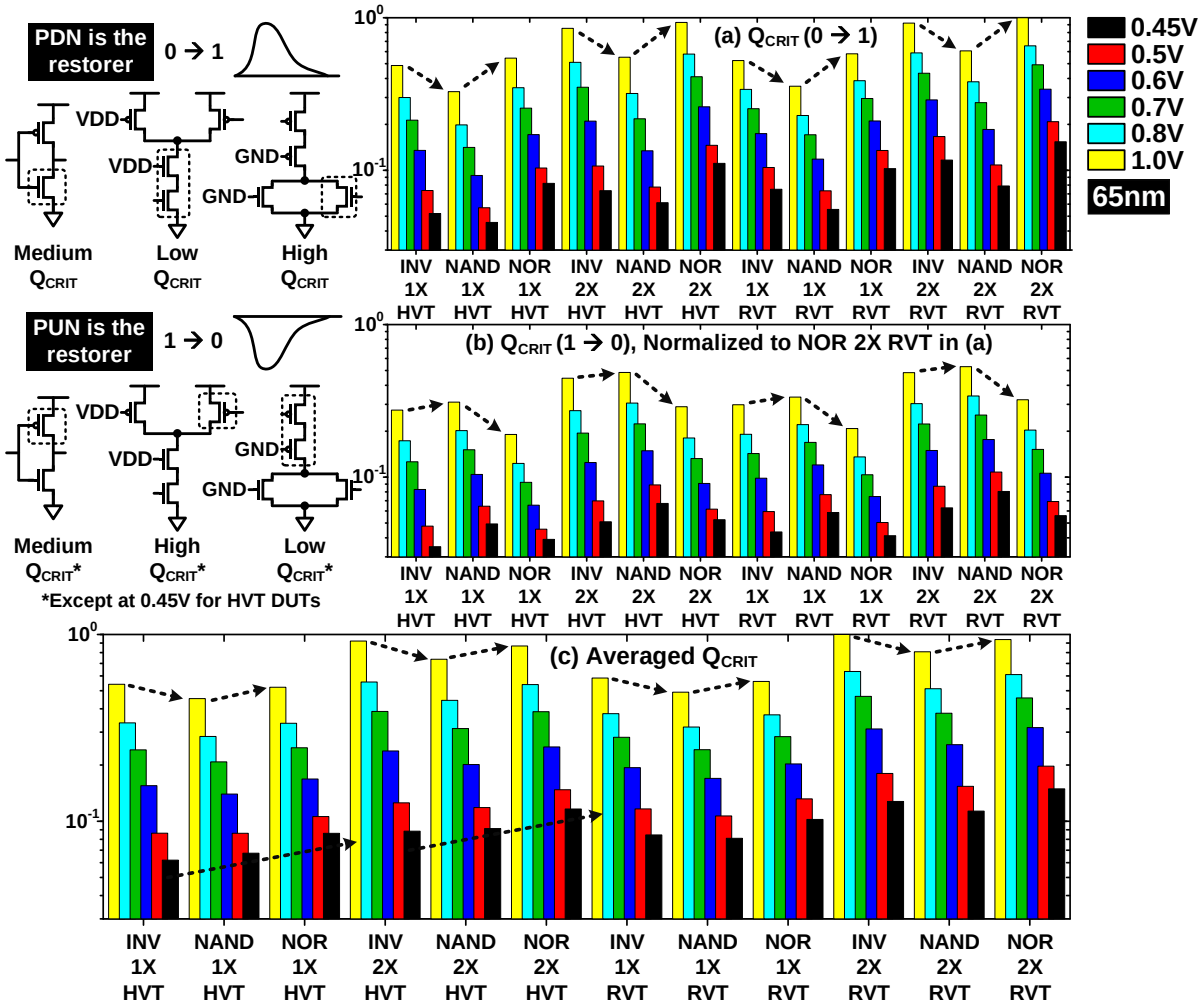

Fig. 5: Simulated Q_{CRIT} trends: (a) 0→1 Q_{CRIT}, (b) 1→0 Q_{CRIT}, (c) averaged Q_{CRIT}, assuming a uniform strike rate for both '0' and '1' nodes.

insightful in revealing the collective SER susceptibility for the standard gate types. We define Q_{CRIT} as the minimum amount of charge required to generate a transient at the output node of the subsequent gate in a logic chain with a peak amplitude of 0.5 times the DUT supply voltage for the simulation. This definition accounts for the drive strengths of the PUN or the PDN of interest for the simulation, the gate output loading as well as the switching threshold of the subsequent stage. The SER sensitivity pertaining to the PUN and the PDN for a gate type is analyzed separately using a current source model in Verilog-A following the double exponential transient shape for modeling both the high-going (with τ_r = 10ps, τ_f =100ps [17-21], Fig. 5(a)) and the low-going (with the source polarity reversed, Fig. 5(b)) transients. The simulations were performed on the post-layout circuit netlists of the unit tile-able block, to carefully account for the layout introduced parasitics, which become crucial elements for determining the SER vulnerability of a node particularly in the low voltage regime. No impact on the relative Q_{CRIT} distributions was observed for sweeping the rise (5ps to 15ps) and fall (50ps to 150ps) time constant values [17]. From our perspective, the relative Q_{CRIT} distributions among the different gate types are more relevant to this work in comparison to accurately estimating the absolute Q_{CRIT} magnitudes or the corresponding SER cross-sections, since we are interested in understanding the SER susceptibility of a gate type relative to others from a circuit design standpoint. Although the simple double exponential model used for this analysis systematically overestimates the Q_{CRIT} / SER cross sections by 10-15% [17], its use still results in a reasonably accurate estimation of the relative gate susceptibility, as evinced from a good match between the simulated trends and the measured data.

Both the 0→1 and 1→0 simulations follow the expected trends when accounting for the $I_{RESTORE}$ and node capacitance as shown in the circuit schematics in Fig. 5. For instance, networks featuring stacks would typically require lower Q_{CRIT}, due to the lower $I_{RESTORE}$. Among unstacked versions, gates having extra node capacitance (viz. the off transistor in NAND PUN or NOR PDN) would require higher Q_{CRIT} than others (INV). The intensity of this trend also varies with supply voltage and the device flavor, sometimes resulting in deviations from expected norm e.g. at 0.45V for PUNs of the HVT variants, with the node capacitance becoming a dominant factor at lower supply especially for these weak flavors.

We also introduce another metric, the averaged Q_{CRIT} of the 0→1 and 1→0 transitions in Fig. 5(c), useful for estimating the overall SER susceptibility of a gate relative to others. With the high and low nodes uniformly distributed throughout the test

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structure for all the logic chains of the standard gate variants, the averaged Q_{CRIT} in fact provides a reasonable first-order estimate for the SER sensitivity of a gate type relative to others, not accounting for effects such as electrical masking or pulse quenching, exposed diffusion areas, process variations etc. The simulated Q_{CRIT} trends presented in this section will be analyzed in further detail alongside corresponding experimental data in the subsequent section.

V. SER Results And Dependences On Key Parameters

This section presents the measured SER cross section, defined as the number of errors for a given DUT type divided by the fluence, expressed in neutrons/cm^2, for the entire duration of exposure at the specific circuit setting. For the irradiation voltages presented in this work, the fluence values ranged between 1.134×10^{11} – 4.189×10^{11} neutrons/cm^2. Furthermore, to establish the uniformity of flux between individual boards, the SER data corresponding to each of the dependences presented in the subsequent sections was also analyzed board-wise. No regular trend indicating a possible loss in the flux uniformity due to stacking of multiple boards was observed.

A. Supply Voltage Dependence

Fig. 6 shows the measured cross-section for the different standard gate flavors considered together, along with SBUs in the embedded DFFs comprising the measurement circuit at multiple supply voltage levels. The failures go up exponentially as the supply voltage goes down [22-25], witnessing the highest increase (i.e. 7.1X) considering the case of INVs, with the errors sharply increasing as the supply voltage scales down to near-threshold voltages. This increase, compared to other gate types, is due primarily to the stronger node capacitance dependence as well as a heightened sensitivity to process variations, further pronouncing pulse quenching effects at low VDDs [10], both of which become deciding factors for soft error vulnerability in the low supply voltage regime, with the $I_{RESTORE}$ becoming a weaker factor. The pronounced impact of node capacitance on the SER vulnerability among the standard gate types is clearly reflected in the Q_{CRIT} simulation results in Fig. 5 at lower supply voltages, with the 0→1 results demonstrating a substantially higher Q_{CRIT} for all the NOR gate variants as compared to the INV types, despite both featuring logically equivalent pull down networks. The impact is also faintly seen in the 1→0 results, with the weaker $I_{RESTORE}$ flavors (1X HVT, 2X HVT) still exhibiting a higher Q_{CRIT} for the NOR gates compared to the INV types, contrary to what one would expect, given that the gate features the weakest pull-up network among all. For stronger variants (1X RVT, 2X RVT), the increase in $I_{RESTORE}$ offsets the node capacitance dominion, which is clearly demarcated by the higher Q_{CRIT} for the INV types. In addition to the node capacitance, digital gates become particularly sensitive to process variations in the low voltage regime, with the susceptibility dependent on the active transistor count directly influencing the propagation delays.

At higher voltages, $I_{RESTORE}$ becomes a dominant factor overcoming both node capacitance and process variation effects. This is evinced by the higher SER for NOR gates and the lowest SER for INV types in Fig. 6, even when considering all the gate types collectively. This is because the NOR gate features the weakest stack (PMOS) among all types, a result again evident from the Q_{CRIT} 1→0 results, demonstrating substantially lower values for all variants of the NOR type at higher supply levels. It should also be noted that the 0→1 Q_{CRIT} results at nominal indicate only marginally higher values for the NOR gates, indicating the much weaker contribution from the node capacitance as compared to lower supply values. These dependences will be broken down in further detail in the subsequent sections.

For SBUs in DFFs, a 2.6X increase is observed for a 695mV difference (1.185V to 0.49V) in the supply voltage, which is attributed not only to the non-minimum sized LVT transistors used for designing these circuits, but also the interconnect load (total 8um, horizontal + vertical) at the output node for routing to the D node of the subsequent DFF in the vertical arrangement. No MBUs were observed even at lower VDDs, for instance, 0.45V for the 65nm technology. This can be attributed to the relatively large center-to-center (1.72µm, vertical between rows; 8.1µm horizontal between the two adjacent columns) distance between the flops (see [22] for a comparison in a similar bulk process to SRAM bit cells, with MBU occurrences strongly correlated to the layout) in conjunction again, with the flop design itself.

One limitation of the circuit, however, is that it cannot distinguish between SETs and Single Event Multiple Transients (SEMTs). If multiple transients are induced in the logic chains that are both spatially and temporally adjacent, they might

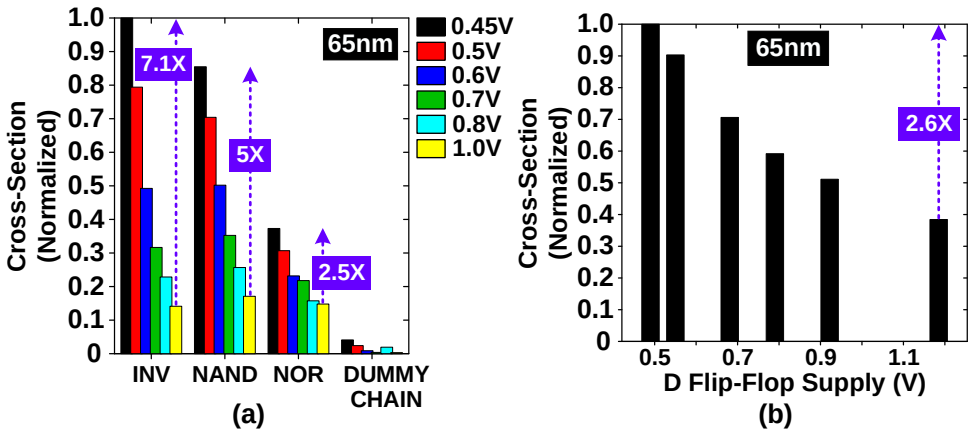

Fig. 6: Measured cross-section at multiple supply voltages for (a) the different standard gate variants considered together and (b) SBUs in D-Flipflops.

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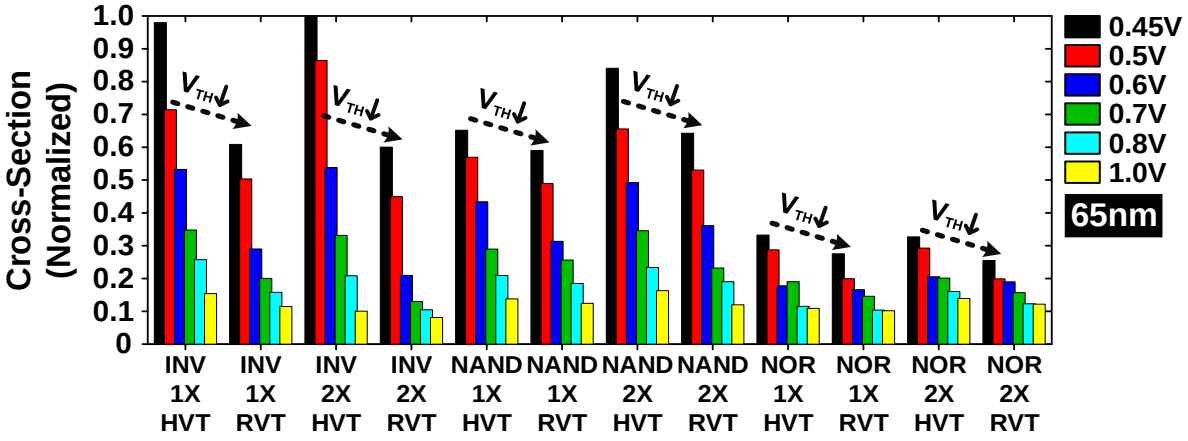

Fig. 7: Measured cross-section results for HVT DUT types vs. RVT DUT types, with the V_{TH} dependence highlighted.

overlap and be counted by the circuit as one single transient. However, the probability of this occurrence would be lower as compared to the SETs themselves, especially in the 65nm process node.

B. Threshold Voltage (V_{TH}) Dependence

Fig. 7 showcases the measured SER cross-section results for HVT and RVT flavors of the standard gate types placed side by side. With other parameters (such as node capacitance, gate topology, supply voltage and device size) being identical, the HVT variants demonstrate a heightened SER sensitivity, due primarily to the lower $I_{RESTORE}$ [26-27], with the trend being consistent for each gate type at all supply voltage levels. The impact of this dependence becomes more pronounced at low voltage levels (0.45V, 0.5V) due to the relative difference in the overdrive voltage ($V_{OV} = V_{GS} - V_{TH}$) between the two variants, which gradually builds up as the supply voltage is lowered. This trend is clearly reflected from the simulated results in Fig. 4. Simulation results in Fig. 5 also show a 1.3-1.5X higher Q_{CRIT} for the RVT variant, supporting the experimental observation.

While all gate types consistently demonstrate a heightened SER sensitivity for the HVT variants at all voltage levels, the relative change in the SER magnitude as a result of V_{TH} change among different gate types depends on the change in average $I_{RESTORE}$ (PUN and PDN combined) in going from a non-stacked gate type viz. INV to a stacked gate type (NAND featuring NMOS stack, NOR featuring the PMOS stack) when considering a device size (1X or 2X) for comparison at a particular supply voltage. The change in $I_{RESTORE}$ is not perfectly linear between unstacked and stacked versions (~2X resistance) for a change in variant type from HVT to RVT depending on supply voltage and is particularly difficult to analyze in the presented data, not only due to averaging effects resulting from a stacked PUN and an unstacked PDN (NOR) or vice versa (NAND) dictating the overall gate susceptibility, but also due to the contamination resulting from electrical masking effects (presented in the subsequent section).

C. Logic Chain Length Dependence

Fig. 8 illustrates the impact of logic chain length on the measured SER cross-section (normalized to gate count) for the standard gate variants considered collectively. With the increase in logic depth, electrical masking or pulse quenching effects [9-16] begin to dominate, causing the pulse to shrink and disappear within the chain. The trend becomes particularly noticeable at lower supply voltages [10], on account of (i) exponentially higher delays or delayed response time and (ii) increased sensitivity to process variations, which have a marked impact on the gate propagation delays. A transistor operating in the slow process corner for a gate in the logic chain results in further increase (and mismatch) in delays, causing significant pulse attenuation and impeding further propagation, the probability of which compounds with both the logic distance travelled as well as the active device count directly determining the delay for the gate topology. Especially evident at 0.45V for the three gate topologies, the effects gradually taper off with the increase in supply voltage. Among the standard gate topologies, INV DUTs show little to no logic depth dependence for higher supply voltages (0.8, 1.0V), whereas gates featuring stacked devices still show the dependence with the trend being especially noticeable for the NOR gates. Owing to lower mobility of p-channel devices in 65nm and identical transistor sizing (PMOS:NMOS=1:1) in all gate types, the NOR gate PMOS stack is the weakest of all PUNs / PDNs among the different gate types even at nominal supply voltages and is thus, still susceptible to electrical masking effects especially in longer chains.

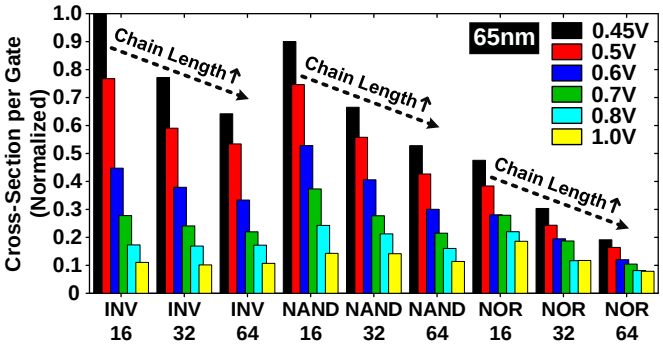

Fig. 8: Collective cross-section results for multiple logic chain lengths.

Fig. 9 presents the measured SER cross section results capturing the detailed impact of logic depth for the three gate topologies. Arranged in order of increasing drive strength at near-threshold voltages (NTV) (0.45V, 0.5V, see Fig. 4), measured data showcases the impact of $I_{RESTORE}$ on the

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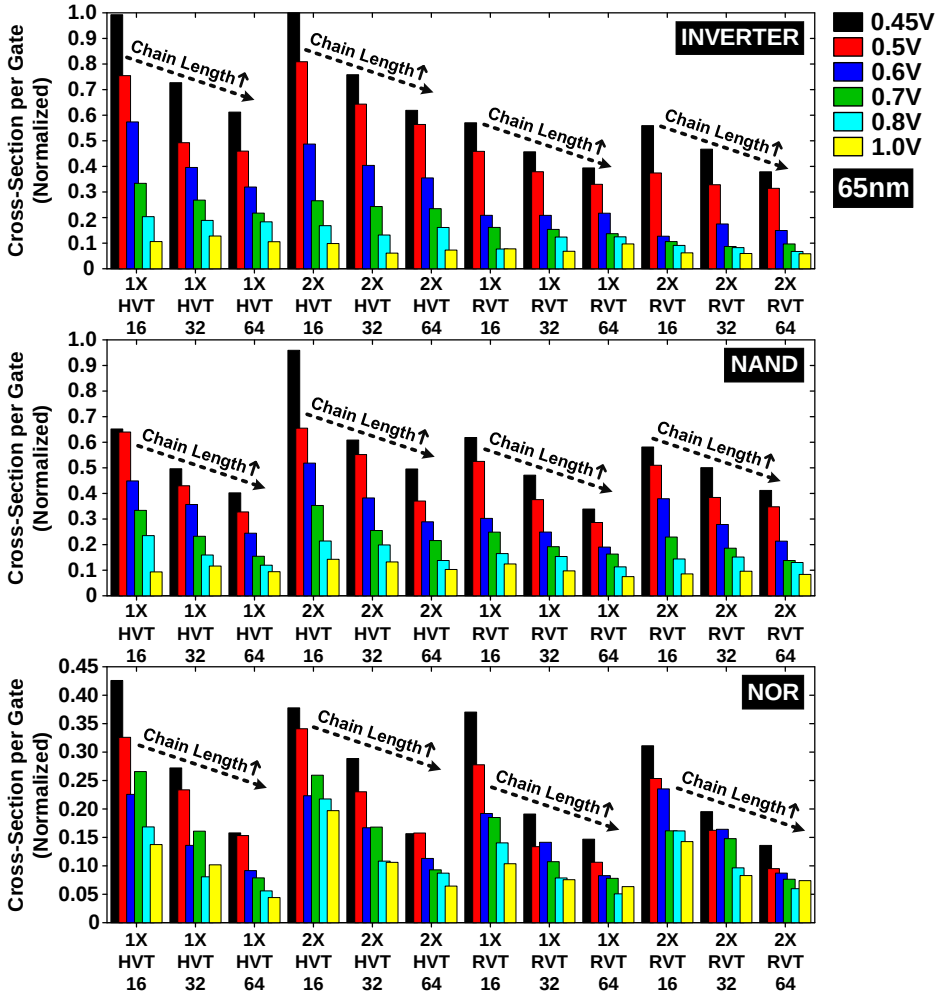

Fig. 9: Measured cross-section results showcasing the detailed impact of logic depth for variants corresponding to the standard gate topologies.

susceptibility of a gate variant to logic chain length induced electrical masking effects, with the stronger $I_{RESTORE}$ variants exhibiting little to no dependence even at lower voltages and weaker $I_{RESTORE}$ variants demonstrating the dependence all the way up to 1.0V. For instance, for INVs, the effect persists from 0.45V to 0.7V for the weakest $I_{RESTORE}$ variant (1X HVT), while stronger variants such as 1X RVT and 2X RVT demonstrate the dependence at only very low supply levels (0.45V, 0.5V). NAND and NOR gates are particularly prone to these effects on account of stacked devices which not only lead to larger delays, but also mismatch in the τ_{PHL} (high-to-low delay) and τ_{PLH} (low-to-high delay) values, resulting in pulse attenuation in both height and width [10-11] as the transient travels along the chain. This is clearly reflected in the measured data, with the stronger NAND gate variants (1X, 2X RVT) demonstrating the dependence upto 0.7V, whereas NOR gates featuring the weak PMOS stack exhibit this dependence even at nominal supply level (1.0V) for both stronger and weaker flavors alike.

D. Gate Type Dependence

Fig. 10 shows the measured cross section data for the different DUTs arranged gate-wise. The SER in the different gate types can be understood by analyzing the low voltage (0.45V, 0.5V) and nominal voltage (1.0V) behaviors for the weakest and the strongest $I_{RESTORE}$ sets (Fig. 10). As discussed in previous sections, among gates having the lowest $I_{RESTORE}$ (1X HVT), the dominant factors contributing to SER are the node capacitance and the susceptibility to process variations, with both dependences amplified at low voltages, where the contribution from $I_{RESTORE}$ is the weakest (Fig. 4, 5). Therefore, in the low voltage regime, the gate with the lowest capacitance (INV) and the one least susceptible to process variations (again, INV) should exhibit higher failures compared to other types, especially for the weaker $I_{RESTORE}$ flavors. This trend is clearly reflected in both the measured data, Fig. 10, as well as the mean Q_{CRIT} results, presented in Fig. 5(c) corresponding to the HVT variants (both 1X and 2X). NOR gates are especially robust at lower voltages, attributed in part to the strong pull down network featuring an extra capacitance (the tendency reflected in Fig. 5(a), as the substantially higher Q_{CRIT} needed for flipping the node state at 0.45V, 0.5V compared with other gates types) and in part to their higher susceptibility to electrical masking effects (Fig. 8, 9). The increase in $I_{RESTORE}$ for the stronger RVT variants at NTV offsets the impact of node capacitance, an effect evinced in both measured data (increased failure rate for NAND gates as compared to INV due to lower $I_{RESTORE}$ in the stacks) as well as simulation results (Fig. 5(b), where INVs exhibit a higher Q_{CRIT} relative to NOR gates for RVT flavors, indicating the dominance of $I_{RESTORE}$ over the node capacitance). At higher voltages (0.8V, 1.0V), INVs show

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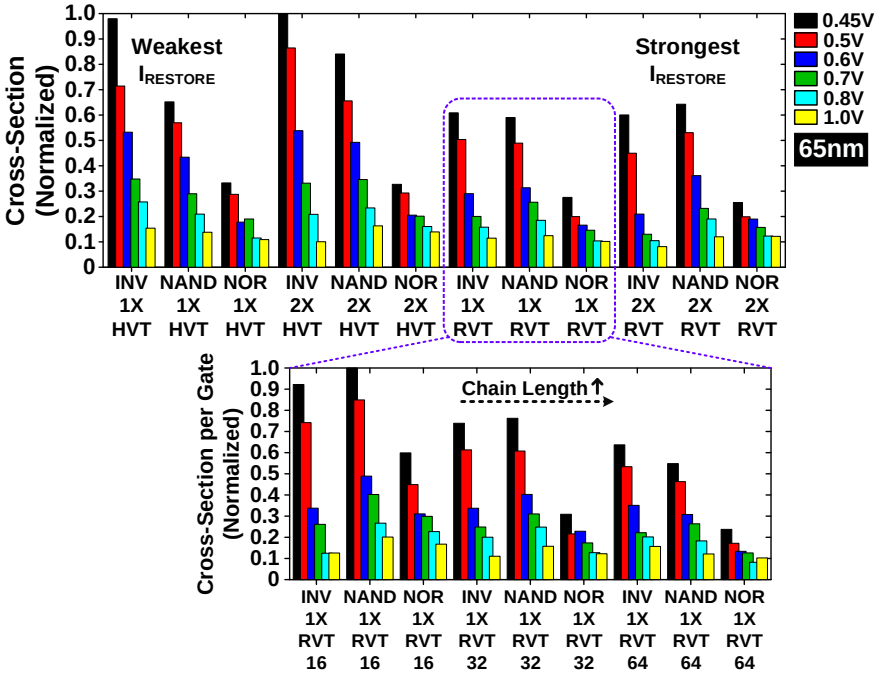

Fig. 10 Measured cross-section data indicating the logic gate type dependence.

lower SER cross-section, which can be especially seen for the case of stronger $I_{RESTORE}$ variants (2X HVT, 2X RVT, see Fig. 4 for the $I_{RESTORE}$ trends at these voltages). This is an expected result (confirmed also by the mean Q_{CRIT} trends in Fig. 5(c)), since $I_{RESTORE}$ now becomes the single most dominant factor determining the gate robustness at nominal levels, largely offsetting both process variations as well as capacitive loading effects and rendering the gates employing stacks more vulnerable to errors. Although the mean Q_{CRIT} data predicts this tendency for both weaker and stronger gate variants (with pronounced prediction for stronger types), it should be kept in mind that these simple post-layout simulations do not account for the other effects such as pulse quenching in longer chains, which prevent the generated SET pulses in weaker gate variants from reaching the measurement circuitry. To illustrate this point, we present the detailed breakdown for the 1X RVT variants, arranged gate-wise for the different chain lengths, clearly showing the expected trend obtained from Q_{CRIT} analysis for the shorter chain length (lowest SER for INVs), as well as the contamination at both NTV and nominal levels, progressively creeping in as the chain length increases to 4X. It should also be noted that the un-normalized counts from longer chain lengths would also be higher and hence, would contribute fairly in shaping the overall collective trend. This discussion also explains why the measured results from the weakest $I_{RESTORE}$ (1X HVT) variants show higher SER for INV DUTs even at nominal, contrary to the Q_{CRIT} predictions. In general, a complex interplay between supply voltage, node capacitance, $I_{RESTORE}$ (affected by device V_{TH}, width and stacking) as well as logic distance travelled to the sequential element determine the relative SER susceptibility among the standard logic gate types.

E. Width Type Dependence

Fig. 11 presents the measured SER for the different DUT types arranged width-wise. On account of having a lower $I_{RESTORE}$ (Fig. 4), a higher SER would typically be expected for the 1X variants. However, the comparatively small feature sizes used for implementing both 1X as well as 2X flavors render them susceptible to process variations, particularly at low supply voltages [10], leading to increased electrical masking, as seen for the 1X variants. As discussed, this effect is magnified for longer chains, for weaker $I_{RESTORE}$ (HVT) variants and low

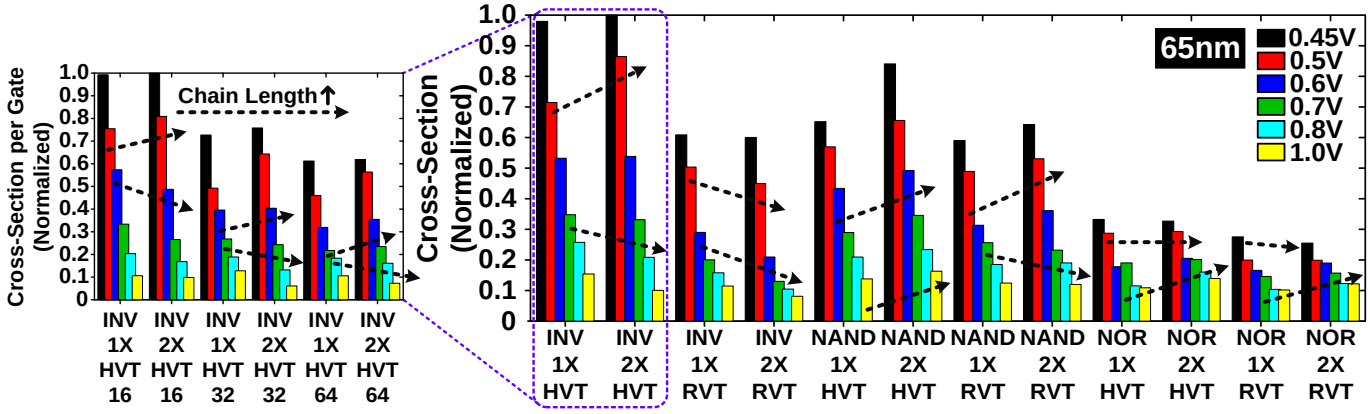

Fig. 11: Cross-section results highlighting the detailed device width dependence.

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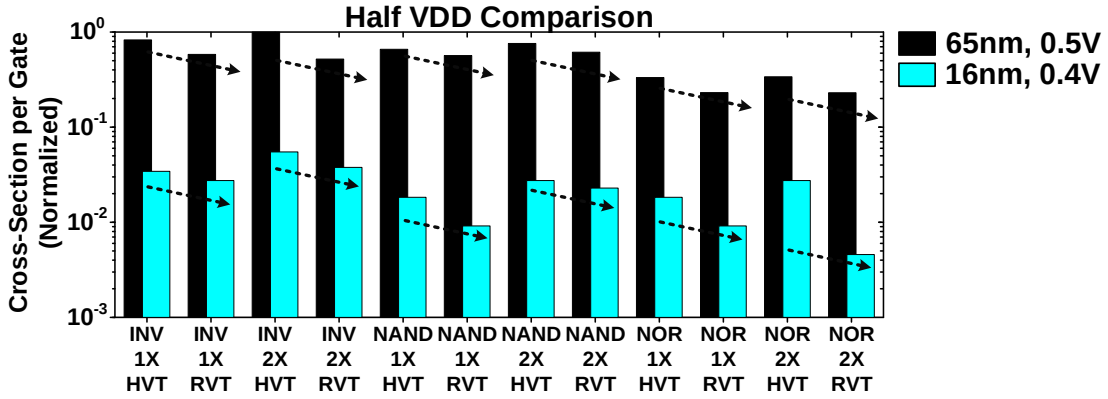

Fig. 12: Measured cross-section results for 65nm planar CMOS and 16nm FinFET DUTs at technologically similar bias points.

VDDs. The trend is clearly reflected in the test data for the INV DUTs, where slightly higher SER values are observed for the 2X HVT flavor at NTV levels, with detailed chain length breakdown showing the progressive increase in masking effects for longer chains, shaping the overall SER. With the increase in supply voltage, the increased gate overdrive offsets such effects, resulting in the expected trend beyond 0.6V. RVT flavors show the expected trend due to the stronger $I_{RESTORE}$. However, as discussed previously, on account of having stacked devices, the NAND/NOR gates are far more vulnerable to electrical masking effects. This can be seen for HVT variants of the NAND gate, with the 2X flavors exhibiting a higher SER all the way up to nominal. The RVT variants show the expected trend for the 2X DUTs, albeit for supply voltages of 0.7V and beyond, again attributed to increased drive current. NOR gate types being particularly susceptible due to the weak PMOS stack, show slightly higher error rate for even the 2X RVT variants at nominal voltages, with the NTV behavior exhibiting similar to slightly higher SER for the 1X flavors of both V_{TH} variants due to slight improvement in the weak $I_{RESTORE}$ for 2X devices coupled with similar susceptibility to masking effects at low voltages. In addition to these effects, the exposed diffusion area for larger widths might also play a role in their susceptibility to SER [28].

F. Technology Comparison: 65nm Planar Vs. 16nm FinFETs

Fig. 12 presents the measured SER cross-section (normalized to gate count), for the standard gate types implemented in 65nm planar bulk CMOS and 16nm FinFET processes, with supply voltages in both cases at half the nominal VDD. Previously reported in literature [1-3], the marked resiliency of FinFETs is clearly evident in our results with standard gate variants exhibiting nearly a 15-60X lower SER compared to their planar equivalents. Although an exact comparison is difficult due to second order effects caused by implementation differences such as logic chain lengths and input connections, measured data still clearly reflects some of dependences discussed in previous subsections.

VI. Conclusion

This work presents statistical data corresponding to neutron beam experiments conducted on standard combinational gates implemented in varying logic chain lengths. A high density, logic oriented test-vehicle with SER and SET pulse width measurement capabilities is introduced and demonstrated in 65nm planar CMOS and 16nm FinFET processes. Using measured data, a wide range of circuit dependences and their intricate interaction dictating the SER for a standard logic gate are explored in detail. The discussion is supplemented with simple first-order technology characterization simulations, which provide further insights supporting the test results.

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