A Counter based ADC Non-linearity Measurement Circuit and Its Application to Reliability Testing

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***Abstract*—In this paper, we present a counter based measurement circuit for in-situ characterization of analog-to-digital converter (ADC) differential non-linearity (DNL) and integral non-linearity (INL). An array of counters collects the histogram of the ADC output code for a triangular input voltage. Since the ADC operation and data transfer operation are separated in time, the DNL and INL results are immune to noise in the measurement setup. Using the proposed characterization method, we studied short-term bias temperature instability (BTI) effects in a successive-approximate-register ADC under different operating conditions.**

Keywords—In-situ; Counter; DNL; INL; SAR-ADC; reliability; device aging; bias temperature instability

I. Introduction

Characterizing analog-to-digital converters (ADCs) is a challenging task as their performance is sensitive to the noise in the measurement setup. There is a plethora of performance metrics that matter to ADC designers; differential non-linearity (DNL), integral non-linearity (INL), signal to noise and distortion ratio (SNDR), effective number of bits (ENOB), spurious free dynamic range (SFDR), and dynamic range (DR). Among these metrics, DNL and INL are the standard linearity parameters which are obtained from the histogram of the ADC codes for a slow triangular input voltage. The frequency of the triangular signal should be low enough to avoid any settling time issues. In the ideal case, all ADC codes appear the same number of times. In reality, however, some codes may have a higher (or lower) count than the ideal count due to non-linearity in the circuit and noise effects. Plotting the deviation of the actual count from the ideal count for each ADC code gives the DNL distribution. Integrating the DNL up to a certain code gives the INL distribution. While measuring DNL or INL is not enough to fully characterize an ADC for high speed applications, they are highly relevant metrics for a wide range of ADCs.

Fig. 1 shows two conventional test setups for characterizing DNL and INL [1-3]. The setup in Fig. 1(a) simply retrieves the raw digital code from the ADC chip while applying a slow ramp voltage as the input. This setup does not require any special circuits; however, the high-speed digital interface can generate significant noise in the measurement setup. This is because the input-output (IO) signals are switching at a high frequency while the ADC is performing the sensitive analog to digital conversion. Consequently, this setup is not suitable for characterizing high resolution ADCs or studying subtle shifts in ADC performance. The test setup in Fig. 1 (b) addresses these concerns. Here, the raw ADC data is stored in an on-chip memory array and later transferred to the host computer. This

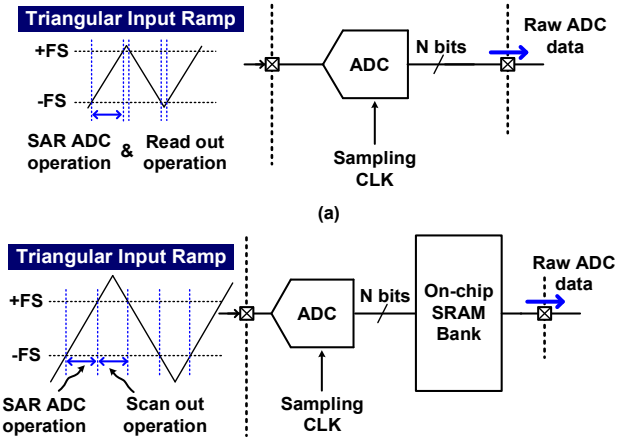


Fig. 1. Conventional DNL/INL characterization methods. (a) ADC samples are continuously retrieved by a test computer. Noise caused by the high speed IO signals can corrupt the conversion results. (b) ADC output is stored in an on-chip memory and transferred to the test computer later. ADC operation is not corrupted by IO switching noise.

setup separates the ADC operation from the data transfer operation, making the ADC characterization immune to measurement noise. The main drawback of this setup however is that it requires a significant amount of on-chip memory, as large as 1 megabits [1], to fully characterize an ADC. Furthermore, the amount of data that needs to be transferred to the host computer is very large.

In this paper, we demonstrate a novel light-weight measurement circuit employing a bank of counters for precise DNL and INL characterization. The proposed method is immune to measurement noise as the ADC operation and data transfer operation are separated in time. Compared to the setup in Fig. 1(b), our design is simpler and more compact as only the count values are stored on-chip. The test time overhead is negligible compared to prior art. Using the proposed approach, we successfully measured short-term reliability effects in a 10-bit successive approximation register (SAR) ADC, which would otherwise have been difficult using conventional test setups.

II. Proposed In-situ DNL/INL Measurement Circuit

Fig. 2(a) shows the proposed in-situ DNL/INL measurement circuit which consists of a decoder block and an array of counters. Each ADC output code is decoded, which enables the corresponding counter and increments its value. A 5-bit counter was chosen in our design considering the area overhead, ADC ramp time, and the target number of samples. For example, a larger counter would require a larger area, but allows a slower ramp signal and can collect more samples before having to

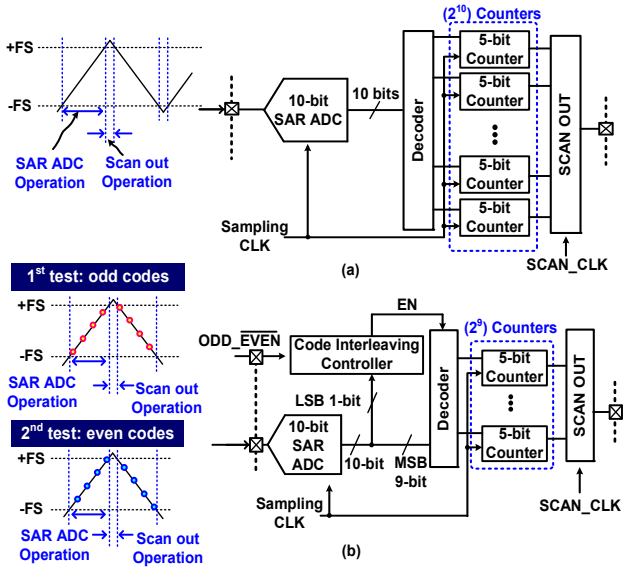


Fig. 2. Block diagram of the proposed DNL/INL measurement circuit; (a) standard design; (b) interleaved design with reduced number of counters. Here, odd and even codes measured from two separate tests must be combined together.

transfer the counter values to the host computer. To prevent the counter from overflowing, the ramp signal should have a period shorter than 2^N * *max count* * *sampling period*. Here, N is the ADC resolution. Storing counts rather than raw ADC codes, reduces the amount of data that needs to be transferred off-chip. This allows the data transfer to occur briefly between the signal ramp up and ramp down. Since the ADC operation and the data transfer operation are separated in time, the ADC can be tested in an extremely low noise environment.

One drawback of the implementation in Fig. 2(a) is the large number of counters needed to measure the full histogram. That is, for an N-bit ADC, we need 2^N counters. This results in a significant area overhead for the test circuit. To make the circuit area more tractable, we opted for the 2-way interleaved design in Fig. 2(b) where only half the number of counters are implemented. To measure the full DNL and INL histograms with half the number of counters, we have to measure the odd and even codes in two separate tests and combine the results later. As shown in Fig. 2(b), the decoder is enabled only when the LSB of the ADC code matches the ODD_EVEN control bit. Using the 2-way interleaved design, we can reduce the circuit area by 50% at the expense of two ramp tests. 4-way or 8-way interleaved designs can be considered for testing ADCs with higher number of bits.

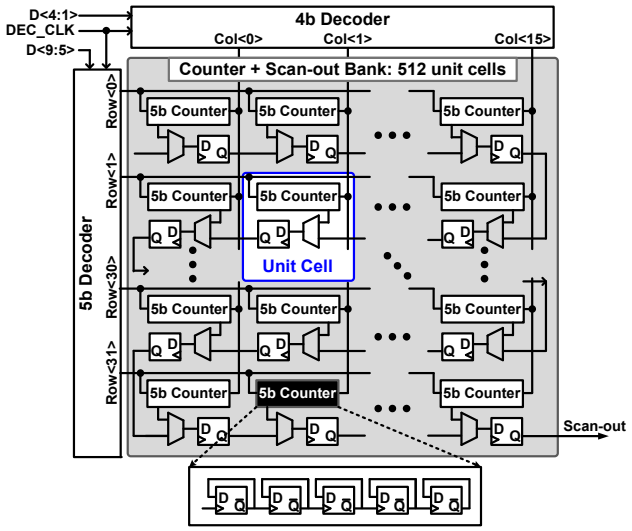


Fig. 3. Implementation of DNL/INL measurement circuit including row and column decoders, 5 bit counters, and scan-out. The counter corresponding to the ADC's output code is incremented.

A total of 512 5-bit counters were laid out as shown in Fig. 3. The 10-bit code from the ADC, less the 1 LSB for even/odd code selection, is decoded by the column and row decoders. That is, a 4-bit column decoder and a 5-bit row decoder selects and increments the 5-bit counter corresponding to ADC code D<9:1>. The 5-bit counters can store count values up to 32, which are read out between signal ramps.

III. Measured DNL/INL Data from 65nm Test Chip

A 10-bit SAR-ADC employing the proposed counter based measurement circuit was fabricated in a 65nm CMOS technology. Fig. 4 shows the measured DNL histogram for the proposed in-situ method and the conventional method in Fig. 1(a). Results are shown for three different clock frequencies; i.e. 0.1MHz, 1.0MHz, and 10MHz. For the experiment, we used a core VDD of 1.2V, an IO VDD of 2.0V (which is slightly lower than the nominal level to further reduce IO switching noise), and an input ramp range of 0.8V. As the frequency increases, DNL measured using the traditional method gets progressively worse while the DNL measured using the in-situ method is not affected. The DNL for the in-situ method ranges from -0.88LSB to +0.34LSB while for the conventional method, it ranges from -1.00LSB to +2.11LSB. The higher immunity to noise means that ADC performance can be measured precisely without an elaborate board design or test setup.

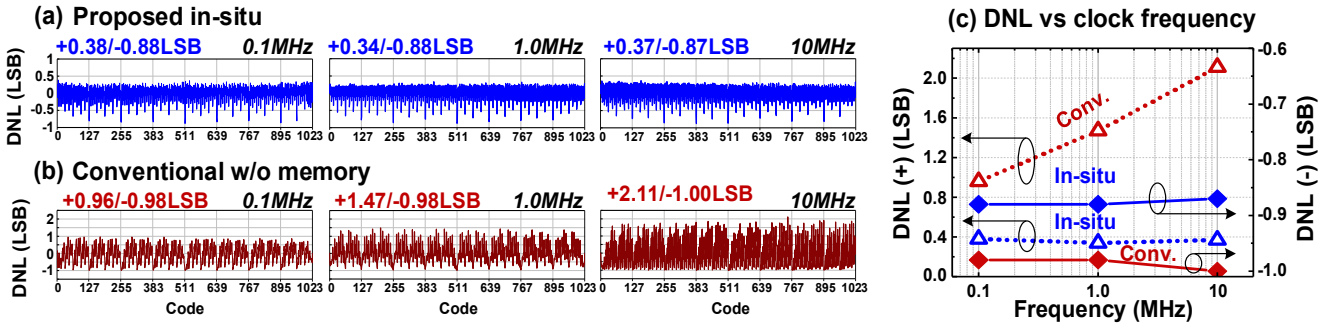


Fig. 4. DNL comparison between the proposed method and the conventional method in Fig. 1(a) for 0.1MHz, 1.0MHz, and 10MHz clock frequencies.

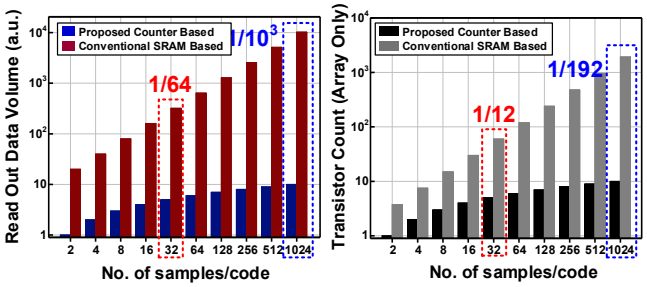


Fig. 5. Comparison between the proposed method and conventional SRAM based test method. (a) Read out data volume; (b) Transistor count (array part only).

Fig. 5 (left) compares the read out data volume of our in-situ method and the conventional method. For an N-bit ADC, the data volume of the two methods can be expressed as $2^N \cdot log_2(\#\ of\ samples/code)$ and $2^N \cdot N \cdot (\#\ of\ samples/code)$, respectively. Our design employing a 5-bit counter reduces the data volume by 64 times. Fig. 5 (right) shows the transistor count comparison (array part only) between the proposed method and conventional SRAM array. An asynchronous counter based on a chain of D-flip-flop (DFF) circuits was used in our chip. Each DFF has a transistor count of 32. A single SRAM cell has a transistor count of 6. Based on these assumptions, we achieved a 12x reduction in transistor count.

IV. Application to ADC Reliability Studies

A. Codes Vulnerable to Short-term BTI Effects

Bias temperature instability (BTI) has become a critical reliability concern in advanced technologies. BTI degradation occurs when carriers get trapped in the interface or the gate dielectric while the device is in a strong inversion mode. This causes the threshold voltage (Vth) to increase. The magnitude of the Vth shift is a function of temperature, voltage, and stress time. When the stress voltage is removed, the device immediately enters a "recovery" phase. BTI degradation and recovery can occur even at microsecond time scales [4] affecting noise-sensitive circuits such as comparators. For instance, when two input transistors of a comparator circuit are exposed to two very different input voltages, asymmetric short-term BTI aging can lead to a time-dependent offset voltage as illustrated in Fig. 6. More specifically, a large asymmetric voltage stress in the input transistors in early conversion steps can induce an error in the later steps where a small voltage difference must be resolved by the comparator (Fig. 7). This issue can be detrimental to the performance of SAR-ADCs even for a fresh chip [5].

Prior work has shown that certain codes are more vulnerable to short-term instability effects (Fig. 7). One of the vulnerable codes is D = 767_{10} which ends with a binary pattern of 0111… In the absence of short-term instability, the correct output code is produced. However, when short-term instability is present, an incorrect code of D = 768_{10} can be generated. Notice the pattern of the incorrect code which ends with 1000… The error in this example is caused in the third conversion step. Other vulnerable codes listed in Fig. 7 have similar patterns; i.e. 0 followed by 1's or 1 followed by 0's.

In this work, we characterized short-term BTI effects in a 10-bit SAR-ADC by measuring the DNL of vulnerable codes using

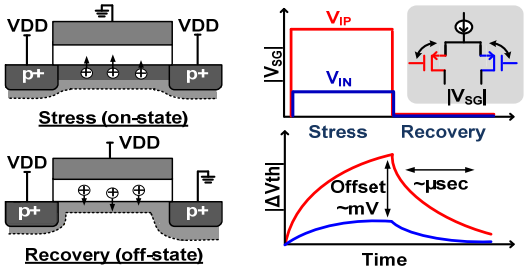
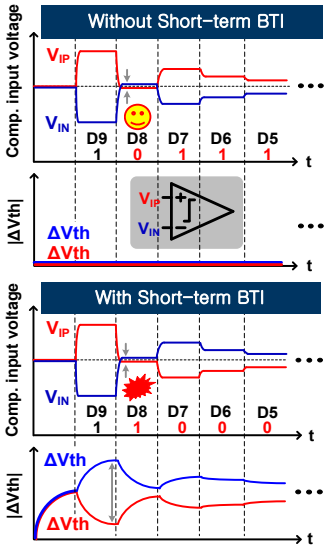


Fig. 6. (Left) Vth degradation and recovery due to short-term BTI effects. (Right) Input offset voltage of comparator circuit can vary dynamically when the difference between the two input voltages V_{IP} and V_{IN} is large.



Vulnerable codes		Conv. step w/ error
Decimal value	Binary D9 D8 D7 D6 D5 D4	
127 =	0 0 0 1 1 1	D7
128 =	0 0 1 0 0 0	
255 =	0 0 1 1 1 1	D8
256 =	0 1 0 0 0 0	
383 =	0 1 0 1 1 1	D7
384 =	0 1 1 0 0 0	
639 =	1 0 0 1 1 1	D7
640 =	1 0 1 0 0 0	
767 =	1 0 1 1 1 1	D8
768 =	1 1 0 0 0 0	
895 =	1 1 0 1 1 1	D7
896 =	1 1 1 0 0 0	

Fig. 7. Illustration of codes that are most vulnerable to short term BTI effects in a 10 bit SAR-ADC. Codes ending with a pattern of 0111… can get misinterpreted as the neighboring code which ends with a pattern of 1000….

the proposed in-situ measurement circuit. It's important to note that the typical value of voltage offset caused by short-term BTI can be less than a millivolt which is difficult to measure using conventional methods.

B. Test Methodology

To study the detailed behavior of short-term instability, we varied the ratio between the stress and recovery times by switching on and off the header PMOS device of the comparator as shown in Fig. 8. The comparator includes a pre-amp stage to reduce kickback noise and input-referred noise. IO devices were used to implement the comparator circuit to suppress gate leakage and sub-threshold leakage. Both PMOS input and NMOS input comparators have been implemented and tested. A multi-phase voltage controlled oscillator (VCO) and a phase selection MUX were used to generate the variable duty cycle clock. For the PMOS input comparator shown in Fig. 8, switching off the header causes the common source node of the input PMOS transistors to collapse, forcing the two input devices into a recovery state. |Vsg| of the two input transistors equalize and consequently, the asymmetric Vth degradation is recovered prior to the next conversion step. A shorter duty cycle clock can reduce the BTI induced Vth shift further by virtue of

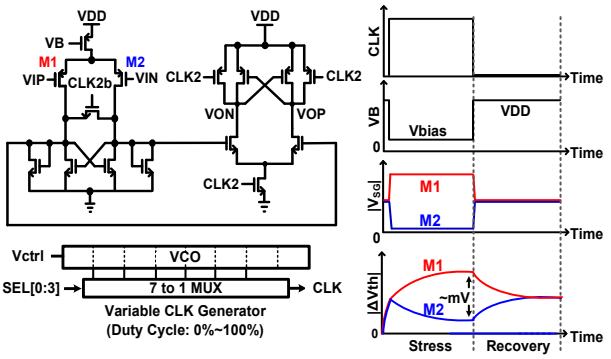


Fig. 8. Variable duty cycle clock generator and clocked bias current for studying fast BTI degradation and recovery effects in comparator circuits. PMOS input comparator is shown in this figure.

a short stress time and a long recovery time. We also characterize the impact of clock frequency on short-term BTI effect in a SAR-ADC.

C. *Measured Results and Analysis*

Fig. 9 shows the DNL of the vulnerable odd codes (i.e. D = 127, 255, 383, 639, 767, 895) and vulnerable even codes (i.e. D = 128, 256, 384, 640, 768, 896) for different duty cycles. A relatively slow clock frequency of 0.125MHz was used in this test to cause more BTI degradation. Results show that for shorter duty cycles, DNL tends to increase for the odd codes and decrease for the even codes. In other words, the number of occurrences of vulnerable odd codes increases while that of vulnerable even codes decreases. This trend suggests that some of the incorrect codes are rectified by the longer recovery time. We also measured the DNL versus duty cycle for different clock frequencies; 0.125MHz, 0.5MHz, and 2MHz. As shown in Fig. 10, the DNL trend lines are generally flat. That is, short-term instability is less obvious at higher frequencies due to the shorter stress time. Fig. 11 shows DNL results for an NMOS input comparator. We found no apparent shift in the DNL value indicating that short-term instability is less pronounced for NMOS devices in this technology. So one remedy to short-term instability issues in this technology is to use comparators with NMOS input devices. Fig. 12 shows the 65nm test chip die photo and the chip feature summary.

V. Conclution

In this work, we demonstrated a counter based measurement circuit for precise characterization of ADC DNL and INL. Using the proposed method, we studied short-term device instability issues in a 10-bit SAR-ADC fabricated in 65nm CMOS. Results confirm that subtle DNL shifts can be accurately measured using the proposed method.

Acknowledgement

The authors would like to thank Dr. Vijay Reddy and Dr. Srikanth Krishnan at Texas Instruments for their technical feedback. This work was supported in part by the Semiconductor Research Corporation and the Texas Analog Center of Excellence (TxACE).

References

[1] L. Kull, et al., "A 90GS/s 8b 667mW 64× int erleaved SAR ADC in 32nm digital SOI CMOS," in *ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 378–379

[2] L. Kull, and D. Luu, " Measurement of high-speed ADCs", *IEEE Custom Integrated Circuits Conference (CICC)*, 2018.

[3] Staller, Len (February 24, 2005). "Understanding analog to digital converter specifications". *Embedded Systems Design*.

[4] C. Yilmaz, et al., "Modeling of NBTI-recovery effects in analog CMOS circuits," *IEEE Int. Reliability Physics Symp. (IRPS),* 2013.

[5] W. Choi, H. Kim, and C.H. Kim, "Circuit Techniques for Mitigating Short-Term Vth Instability Issues in Successive Approximation Register (SAR) ADCs", *Custom Inte grated Circuits Conference (CICC)*, 2015.

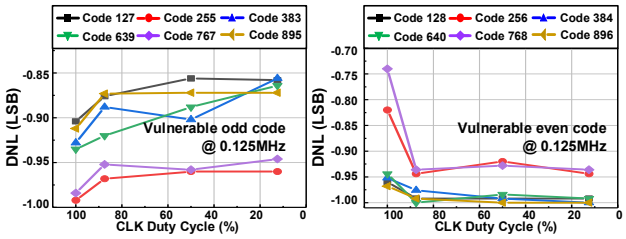


Fig. 9. DNL measured under different duty cycles for the most vulnerable codes; (left) codes ending with 0111…; (right) codes ending with 1000…. Results shown are for comparators with IO PMOS input transistors.

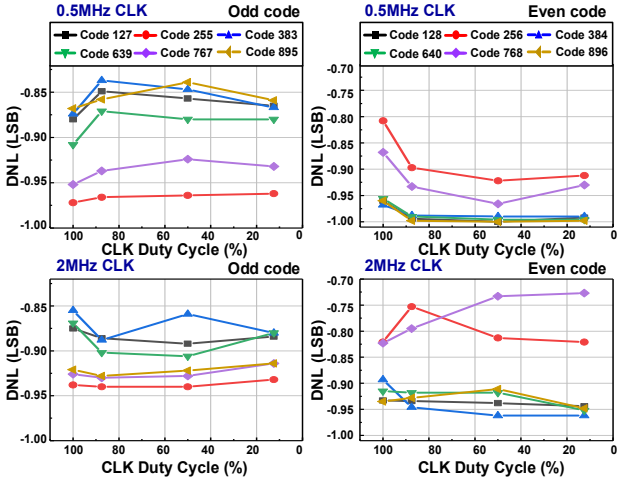


Fig. 10. DNL measured at 0.5MHz and 2MHz clock frequencies for the most vulnerable odd and even codes.

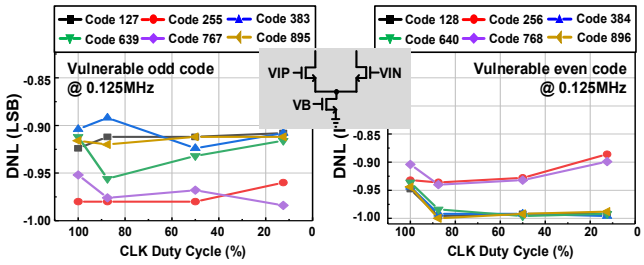
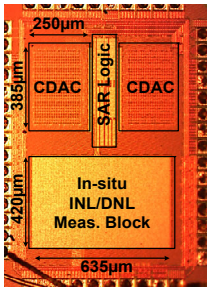


Fig. 11. Measured DNL for SAR-ADC with IO NMOS input comparators suggesting negligible short term instability effects.



Process		65nm GP CMOS
Core / IO supply		1.2V / 2.5V
ADC resolution		10-bit
DNL (max)	vs Con. (w/o SRAM)	0.88 LSB (1.23 LSB improv.)
Read Out Data Volume	vs Con.	1/64 (for 32 samples/code)
Tr. count of on-chip measurement block		94,208 (Counters only)
DNL		+0.34 / -0.88 LSB @ 1MHz
INL		+1.67 / -1.41 LSB @ 1MHz
Total chip area		0.57mm^2

Fig. 12. 65nm die photo and chip feature summary.