Electromigration Effects in Power Grids Characterized Using an On-Chip Test Structure with Poly Heaters and Voltage Tapping Points

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Abstract

A 65nm test chip to study electromigration (EM) effects in power grids was taped-out and tested. A 9x9 grid was implemented using M3 and M4 metal layers which was stressed under constant current and constant voltage modes. On-chip poly heaters were employed to raise the die temperature to 350ºC without damaging the chip package. A bank of transmission gates based on IO transistors were used to tap out the M3 and M4 voltages at each intersection point of the power grid. Using the test structure, we could observe for the first time, subtle behaviors of EM such as mechanical stress dependent failure locations and self-healing due to redundant current paths.

Introduction

Electromigration (EM) effects in a single wire or a chain of wires have been studied for decades [1,2]. However, EM effects in a power grid have not been reported due to the measurement complexity. Redundant current paths in power grids make failure induced resistance jumps less obvious, and thus hard to track. In this paper, we present an on-chip test structure with poly heaters and voltage tapping points which allows efficient monitoring of subtle failures in a power grid.

Test Structure Design

The test structure is a 9x9 grid implemented in M3 and M4 metal layers, as shown in Figs. 1 and 2. Pad connection points A, B, and C are located at the two corners and the center of the grid with multiple dense vias to prevent failure. Each metal segment is 20µm in length and 0.1µm in width. 81 intersections are formed on the entire 9x9 grid. To collect EM data within an attainable stress time, single minimum size via were used to connect M4 and M3 layers at each intersection. 162 (=9x9x2) nodes are uniformly distributed on the entire grid, with half of the nodes on M4 and the other half on M3. As shown in Fig. 1, we use a M5-M4 via to tap the node voltage of M4, and a M3-M2 via to tap the node voltage of M3. This design allows us to directly measure the voltages on grid structure, without introducing any appreciable electrical or mechanical disturbance to the power grid. M5 and M2 wires were routed to the transmission gate array located at the other side of the chip to protect from the extremely high stress temperatures. The voltage drop across each 20µm M4 and M3 segment and M4-M3 via can be calculated from the measured tapping voltages.

As shown in Fig. 2, each power grid voltage is multiplexed out through individual transmission gates connected to a shared analog pad. A scan chain enables one tapping voltage at a time, and IO devices are used to suppress leakage current. The active circuits are placed more than 400µm away from the heating area to further reduce the leakage current. Three on-chip heaters [2] were used for efficient local temperature control. The heating area is 260µm x 260µm, with the power grid DUT placed in the middle. The die photo is shown in Fig. 10. The stress temperature was controlled by a software program shown in Fig. 3. The direction of the stress current was periodically reversed to prevent EM in the heaters themselves which resulted in a momentary temperature overshoot.

Power Grid Failure Locations

Fig. 4 shows all 162 tapping voltages measured from a fresh grid. The voltage drop across each segment was calculated and plotted as shown in Fig. 5. Here, the arrow indicates the magnitude and polarity of the voltage across each wire, while the circle and square markers at each intersection indicate the voltage across each via. Fig. 6 shows the first EM failure point under three different stress current configurations: A+B → C; C → A+B; and A → B. In all three cases, the first EM event happened close to the negative voltage terminal denoted V(-). This result verifies that EM failure is affected not only by current density but also by mechanical stress [3]. Fig. 7 shows how the voltages in each branch change after an EM event. The change of the voltage can be attributed to two reasons: resistance increase in the via or wire due to EM, or current increase due to EM at a nearby location.

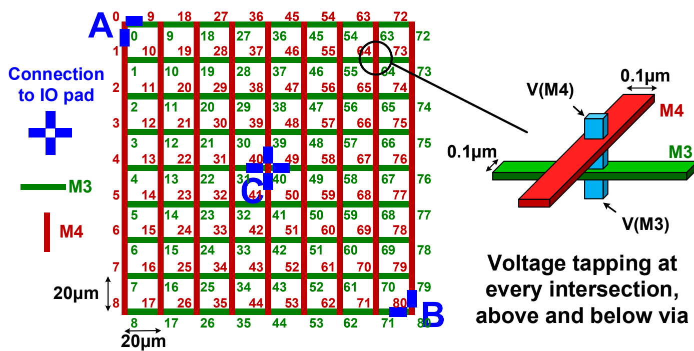
EM Healing Effect

Fig. 8 shows the power grid resistance between A+B and C, along with the voltage drop across each adjacent node. We observed not only abrupt and progressive failures but also self-healing behavior. This is consistent with [4] where supporting data shows that wire connections can be temporarily restored. As shown in Fig. 8 (right), several voltage traces show toggling behavior for stress times from 15 to 20 hours. Based on their fluctuation magnitudes, we can find the location of the via that is undergoing self-healing. The voltage across via #39 under constant voltage stress elucidates the stress and healing cycles (Fig. 9). The time it takes for the connection to break again increases with a longer stress time.

Significance of EM Healing

To our knowledge, this is the first report of EM healing in a power grid under continuous current stress. Unlike previous works where the temperature was lowered during measurement, this work does not involve any temperature cycling, and thus thermal shrinking and expansion cannot be the reason behind the healing phenomenon. We believe EM healing is a natural process occurring in power grids due to mechanical back stress. Healing was rarely discussed in previous works because single wire test structures do not have any redundant current paths, so stress current is forced even after an EM failure, resulting in permanent damage that cannot be reversed. However, a power grid structure is different in that it has numerous redundant paths allowing the current to bypass the failure location immediately upon an EM event, providing the opportunity for healing. Since EM healing effect was overlooked in previous studies, the actual lifetime of a power grid might be significantly longer than previously thought.

References [1] S. Lee and A. S. Oates, IRPS, 2006. [2] C. Zhou, X. Wang, R. Fung, S. J. Wen, R. Wong and C.H. Kim, VLSI Technology Symposium, 2015. [3] M. H. Lin and A. S. Oates, IRPS, 2016. [4] C. Zhou, X. Wang, R. Fung, S. J. Wen, R. Wong and C. H. Kim, TDMR, 2017.



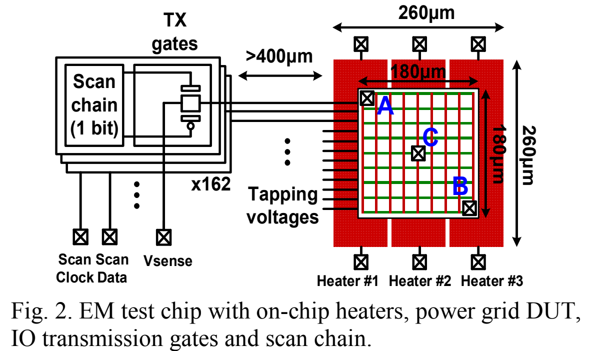


Fig. 2. EM test chip with on-chip heaters, power grid DUT, IO transmission gates and scan chain.

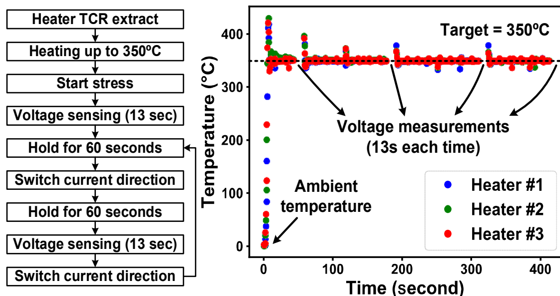


Fig. 3. (Left) Temperature control loop. Heater current direction reversed periodically to prevent EM in heaters. (Right) Temperature measured from 3 heaters.

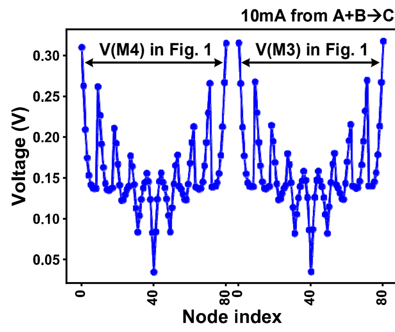


Fig. 4. Measured tapping voltages for all M3 and M4 nodes.

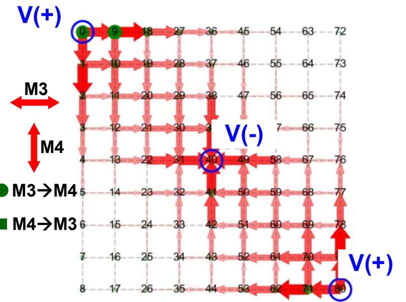


Fig. 5. Measured voltage drop. Arrow indicates the magnitude and polarity of voltage drop between adjacent nodes.

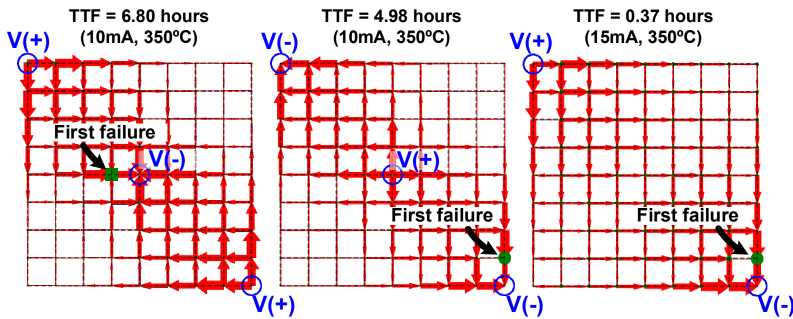


Fig. 6. First EM failure locations for different stress current configurations. Due to mechanical stress effects, the first failure occurs near the negative voltage terminal.

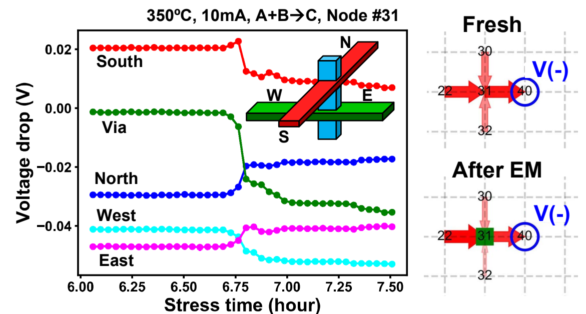


Fig. 7. Example of voltage drop traces after an EM event. The increased voltage across the via suggests a change in the via resistance or EM in nearby structures.

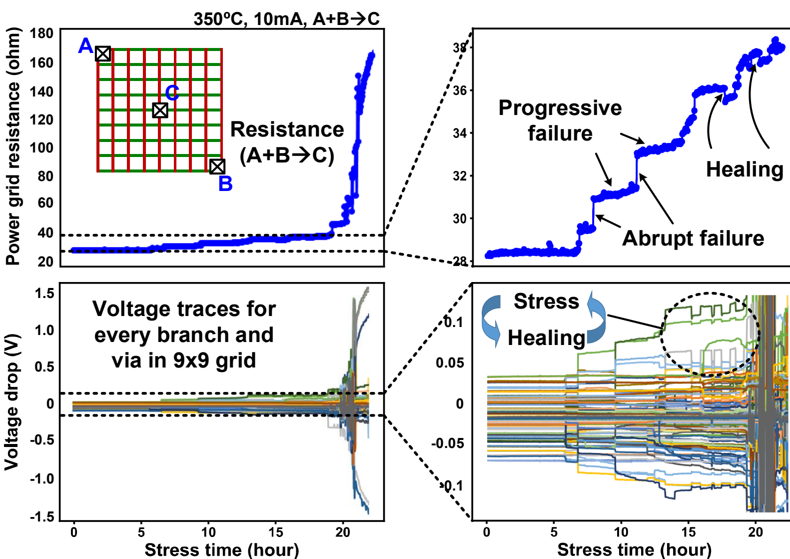


Fig. 8. (Left) Power grid resistance and voltage drop traces of all wires and vias. (Right) Zoomed in plots showing self-healing behavior.

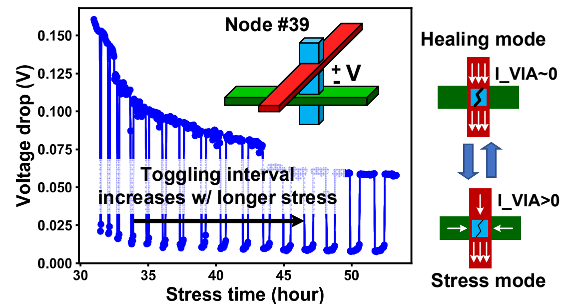


Fig. 9. Voltage across via toggles between stress mode and healing mode under constant voltage stress. Time spent in stress mode gradually increases.

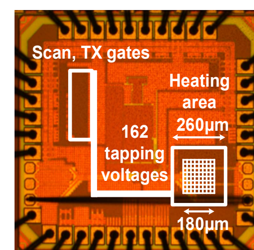


Fig. 10. Die photo of 65nm test chip.