A 2.1 pJ/bit, 8 Gb/s Ultra-Low Power In-Package Serial Link Featuring a Time-based Front-end and a Digital Equalizer

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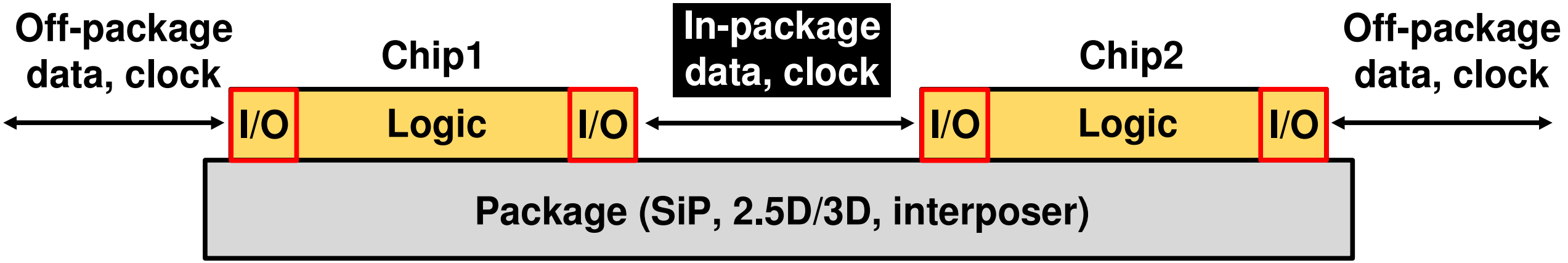
Outline

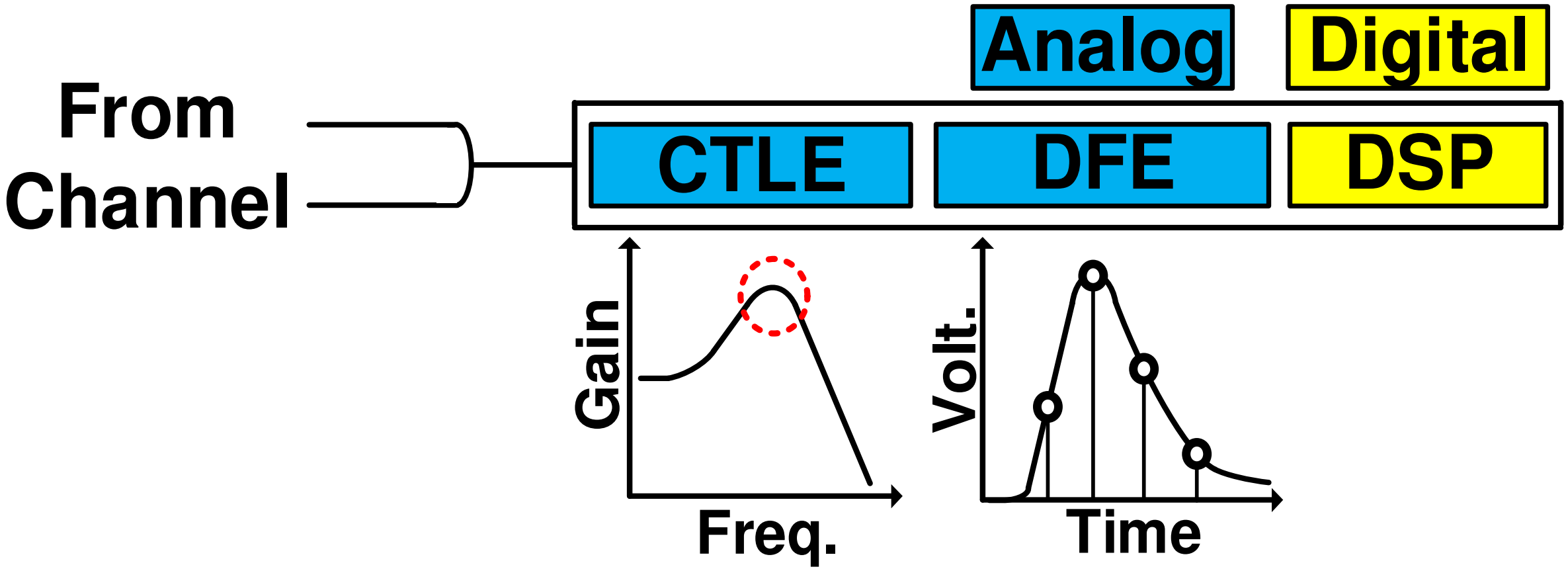
- Motivation
- Proposed Time-Based Receiver
- Proposed Delay Line Based Time Amplifier
- 65 nm Test Chip Measurement results
- Conclusion

Motivation



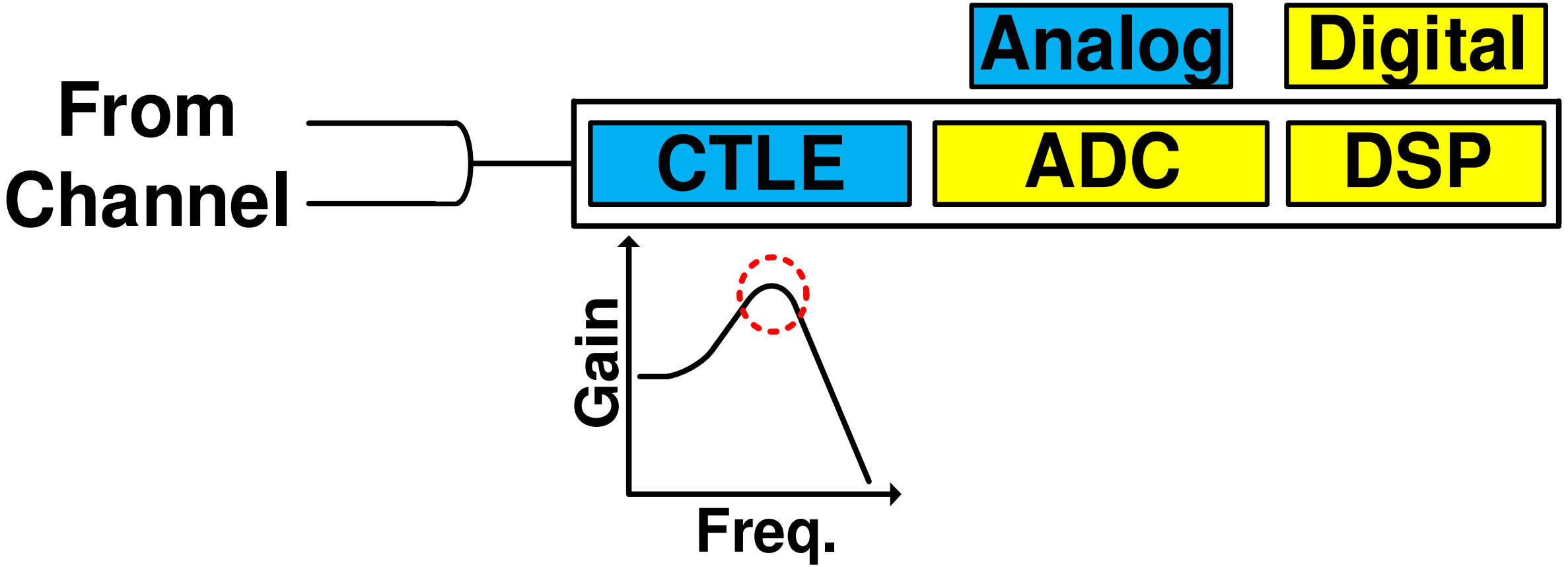
- **System-in-Package**
  - Multi-chip integrated in a single package
  - Enables small form factor

RX Equalization Technique



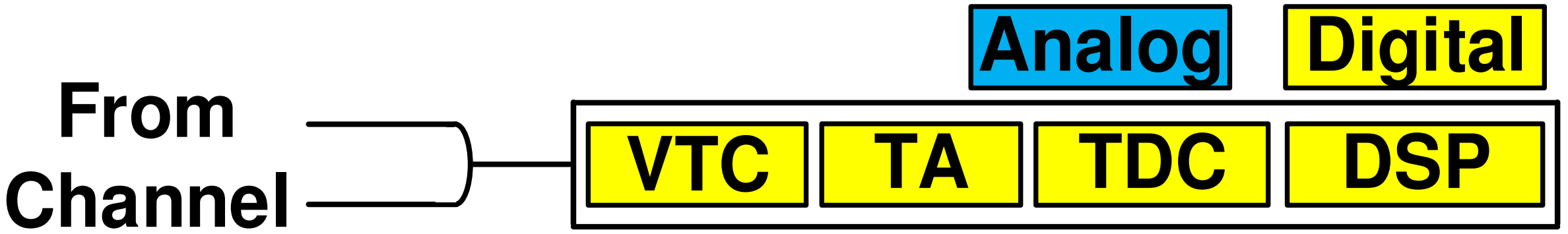
- Continuous Time Linear Equalizer (CTLE)
- Decision Feedback Equalizer (DFE)

RX Equalization Technique



- ADC-based receiver enables digital equalization
- Take advantage of CMOS scaling

RX Equalization Technique

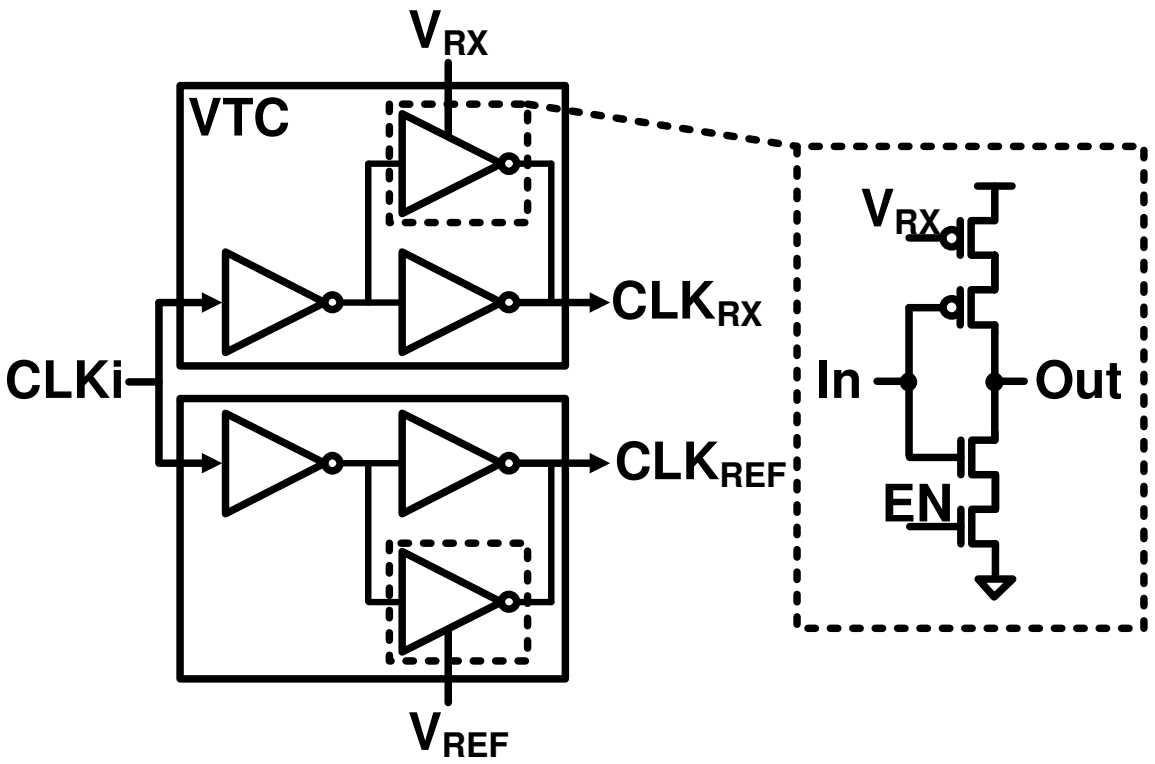


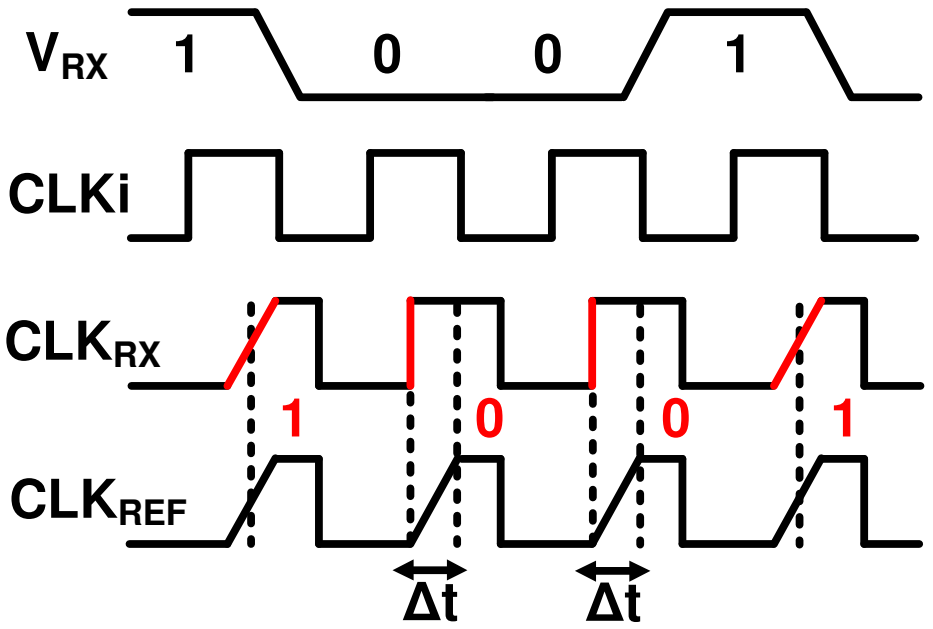
- Voltage-to-Time Converter (VTC)
- Time Amplifier (TA)
- Time-to-Digital Converter (TDC)
- Digital-intensive time-based front-end
- Signal amplifier is performed in the time domain while equalization is performed by DSP circuits

Time-Based Receiver

Receiver Type (Digital / Analog)	Features	
Analog Frontend: CTLE → VGA → Analog DFE	Fully-Analog	Voltage based
Analog Frontend: CTLE → VGA → S/H → ADC → DSP	Analog FE, Digital Equalizer	Voltage based
Proposed Time-based Frontend: VTC → TA → TDC → DSP	Digital FE, Digital Equalizer	Time based

Voltage-to-Time Converter

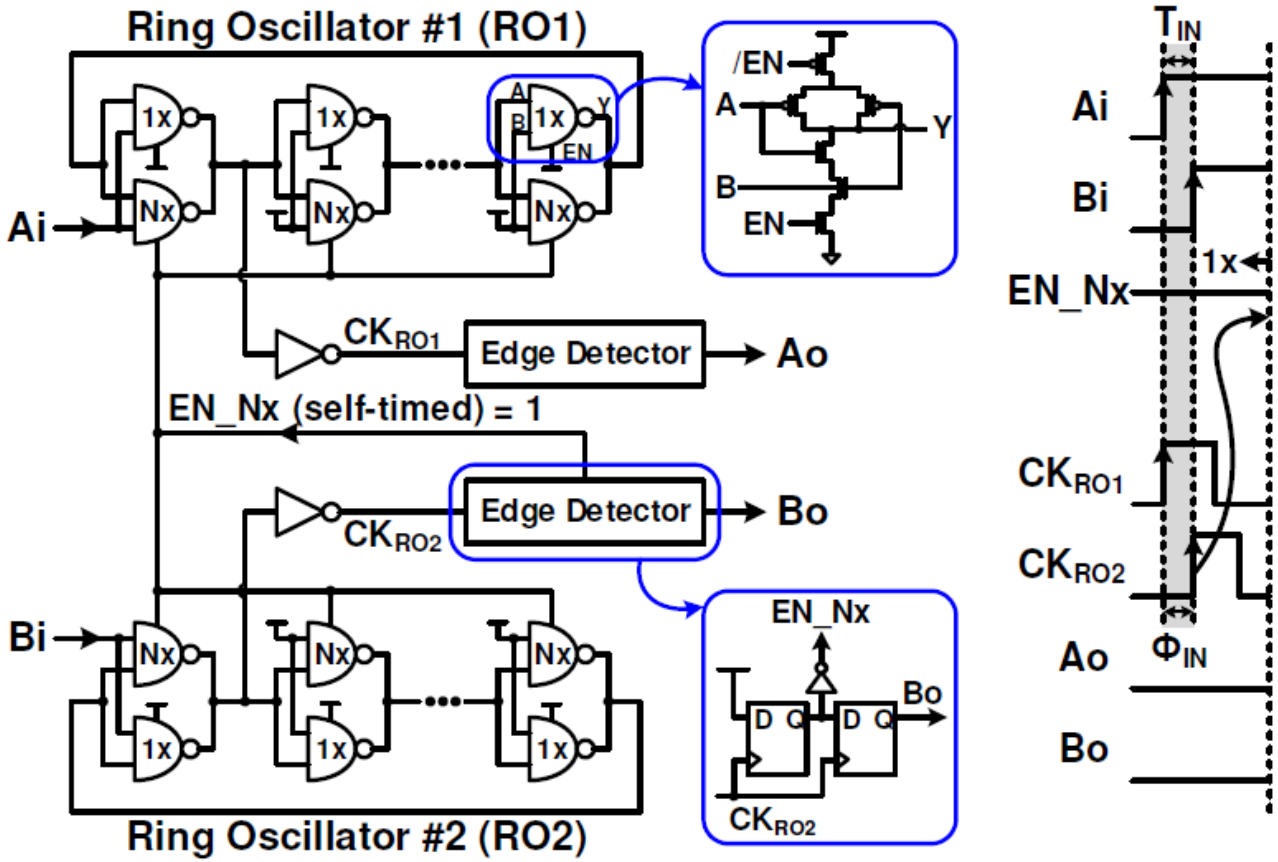




[1] P. Chiu, et al., JSSC, 2018.

- Time delay is determined by input signal
- Voltage signal is converted to time delay

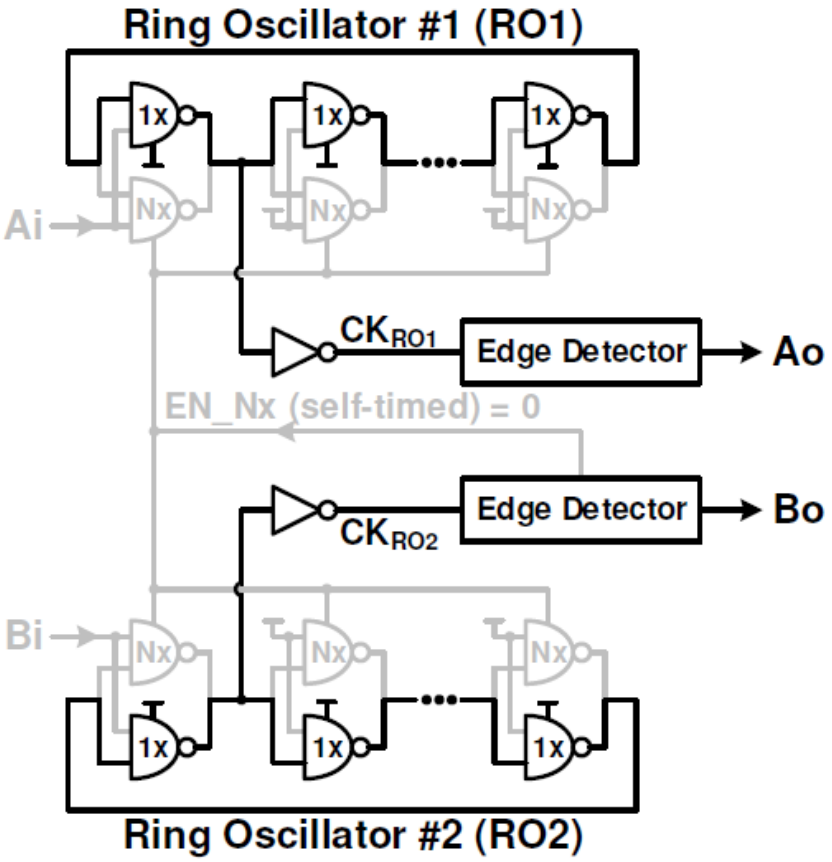
Related Time Amplifier

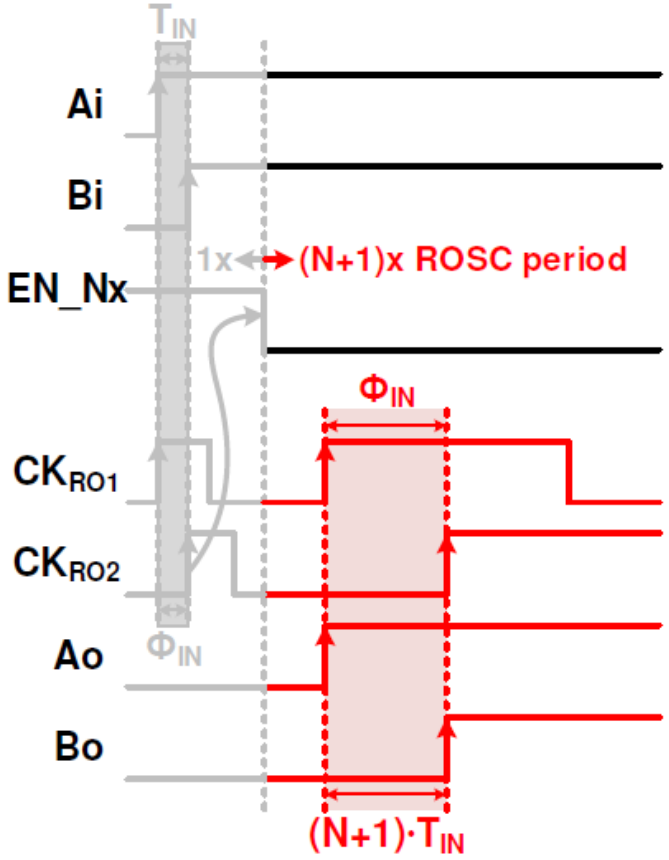


[2] B. Kim, et al., CICC, 2015.

- NAND gate based Ring-oscillator design
- Speed is limited by oscillator frequency

Related Time Amplifier





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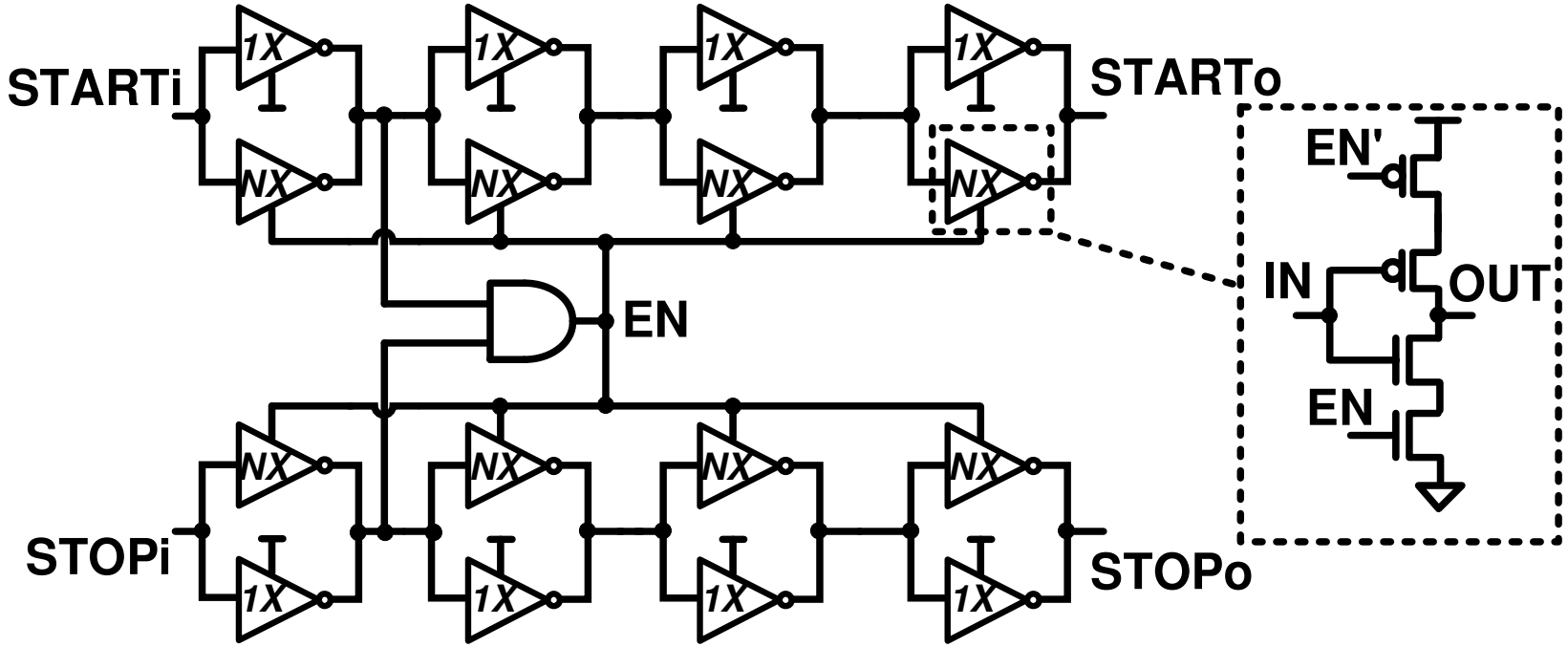
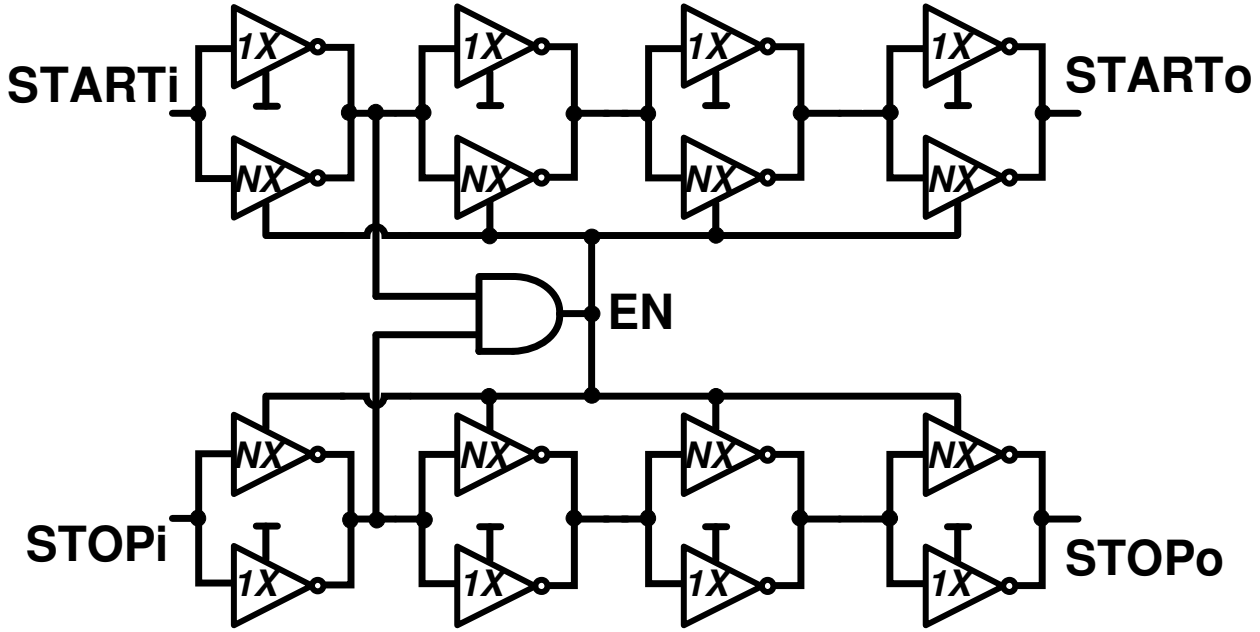
Proposed Time Amplifier



- Open loop delay line for short range application
- Inverter based design

Proposed Time Amplifier



STARTi

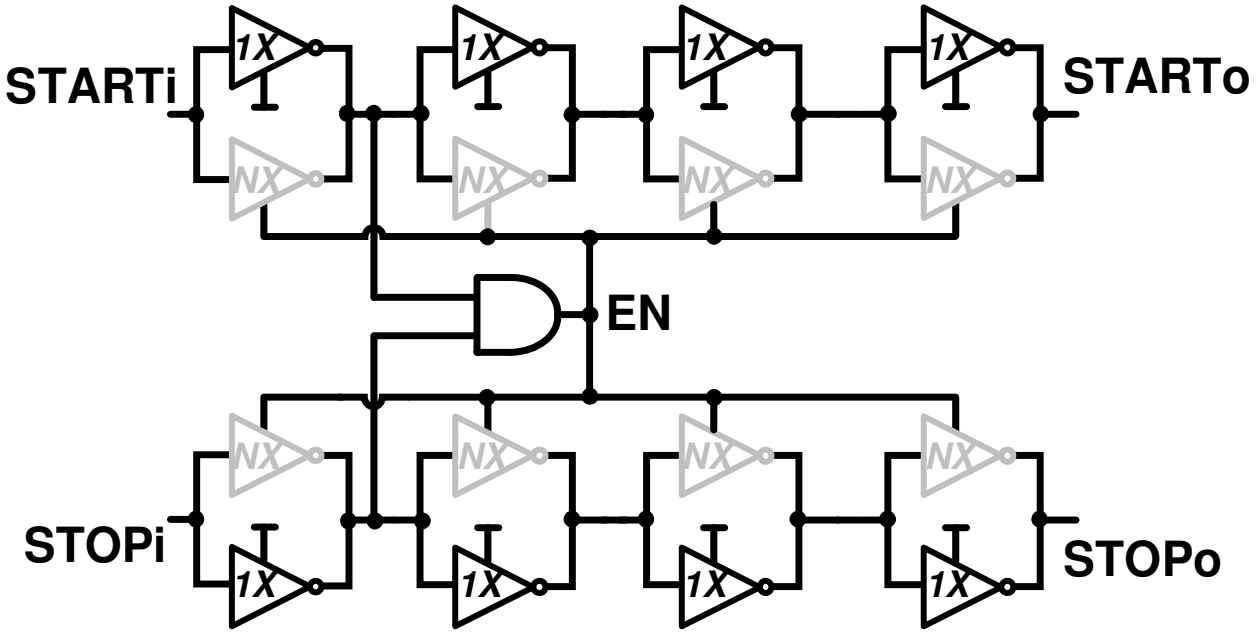
STOPi

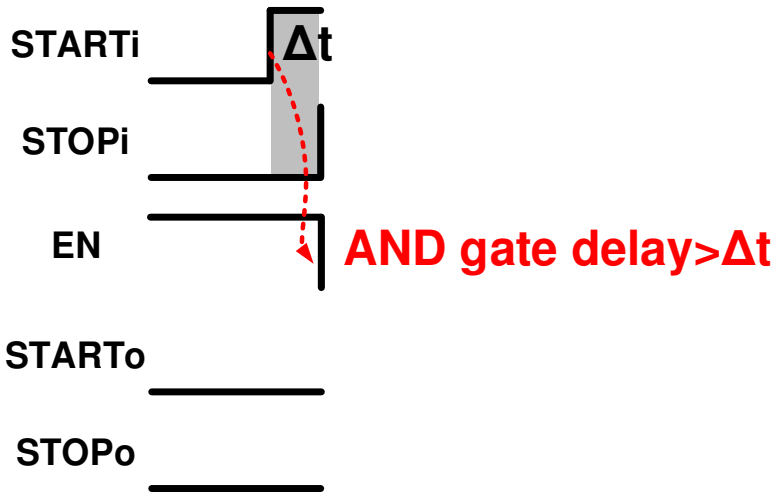
EN

STARTo

STOPo

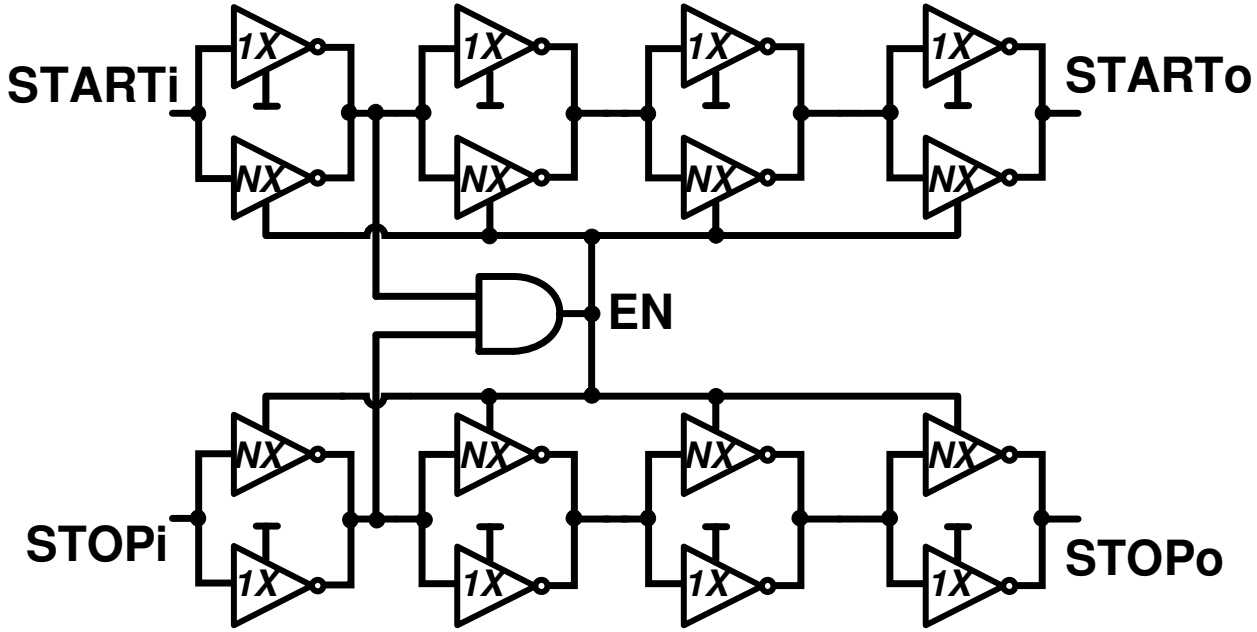
Proposed Time Amplifier

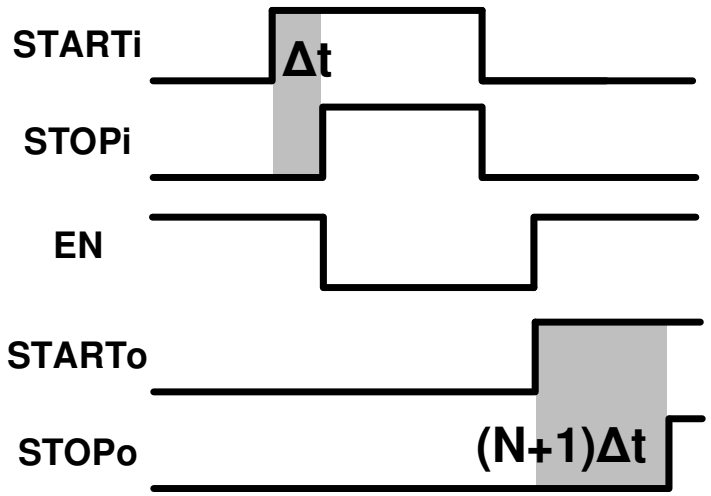




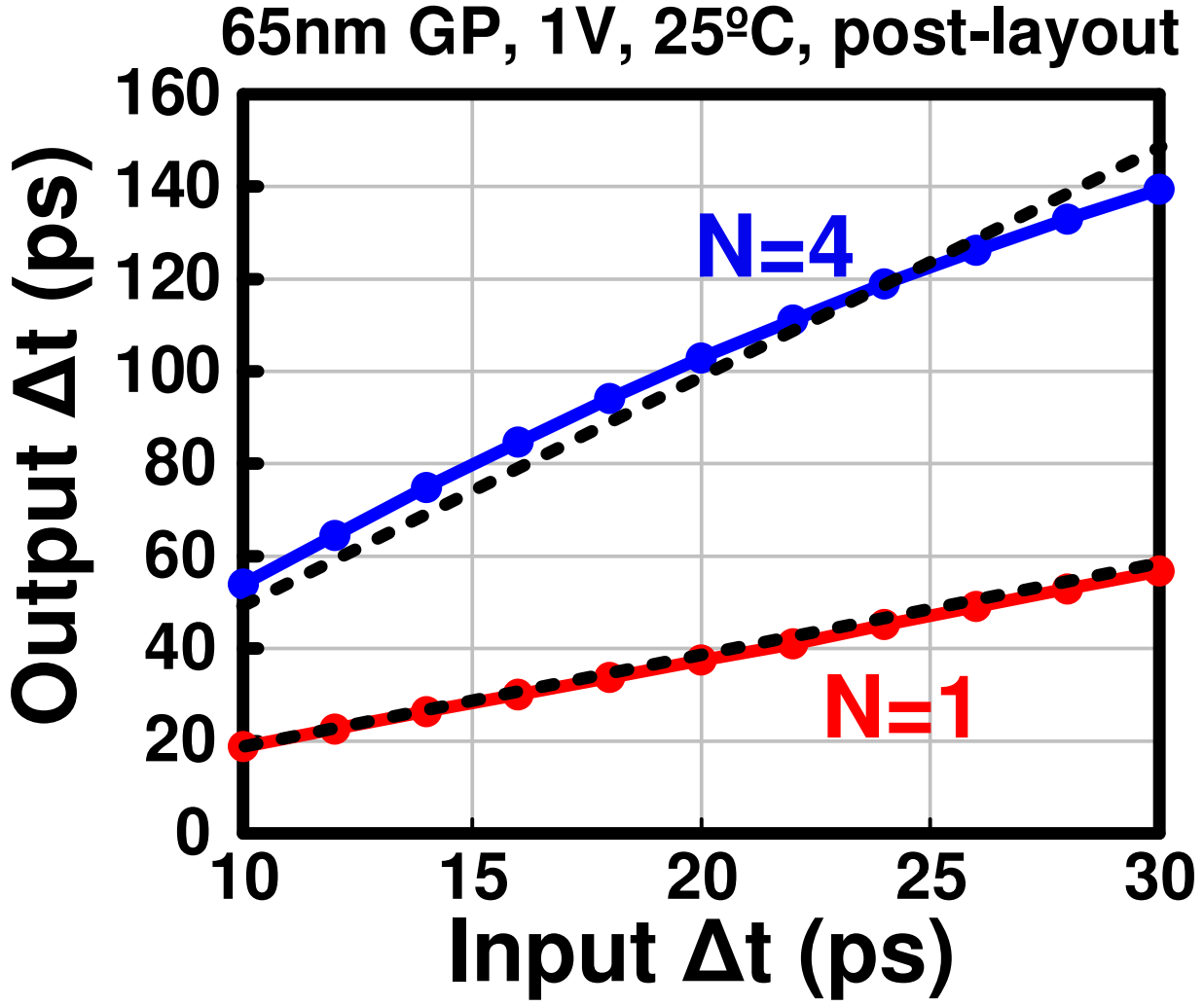
- STARTi driving by N+1 inverter Δt longer than STOPi

Proposed Time Amplifier



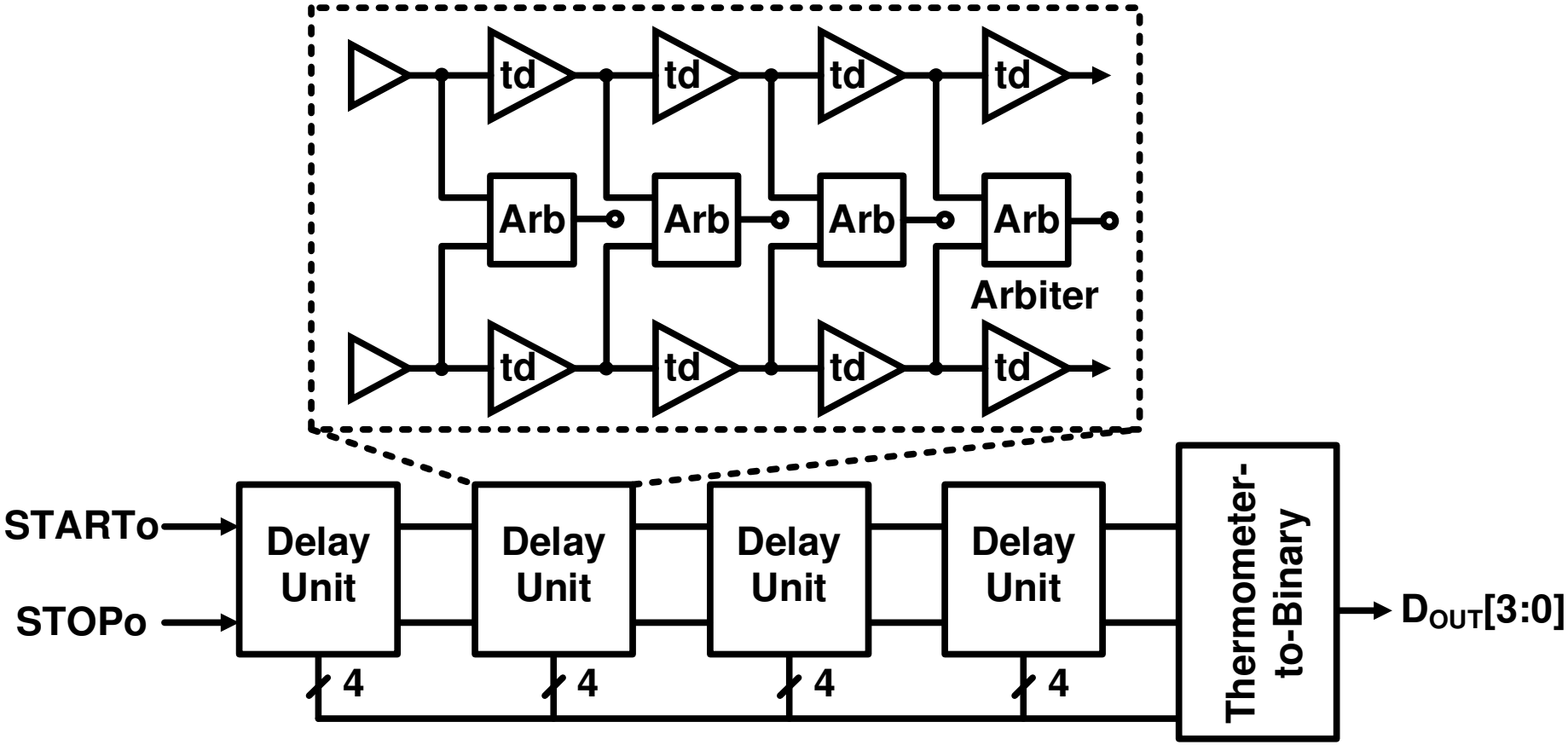


Time Amplifier Simulation Results



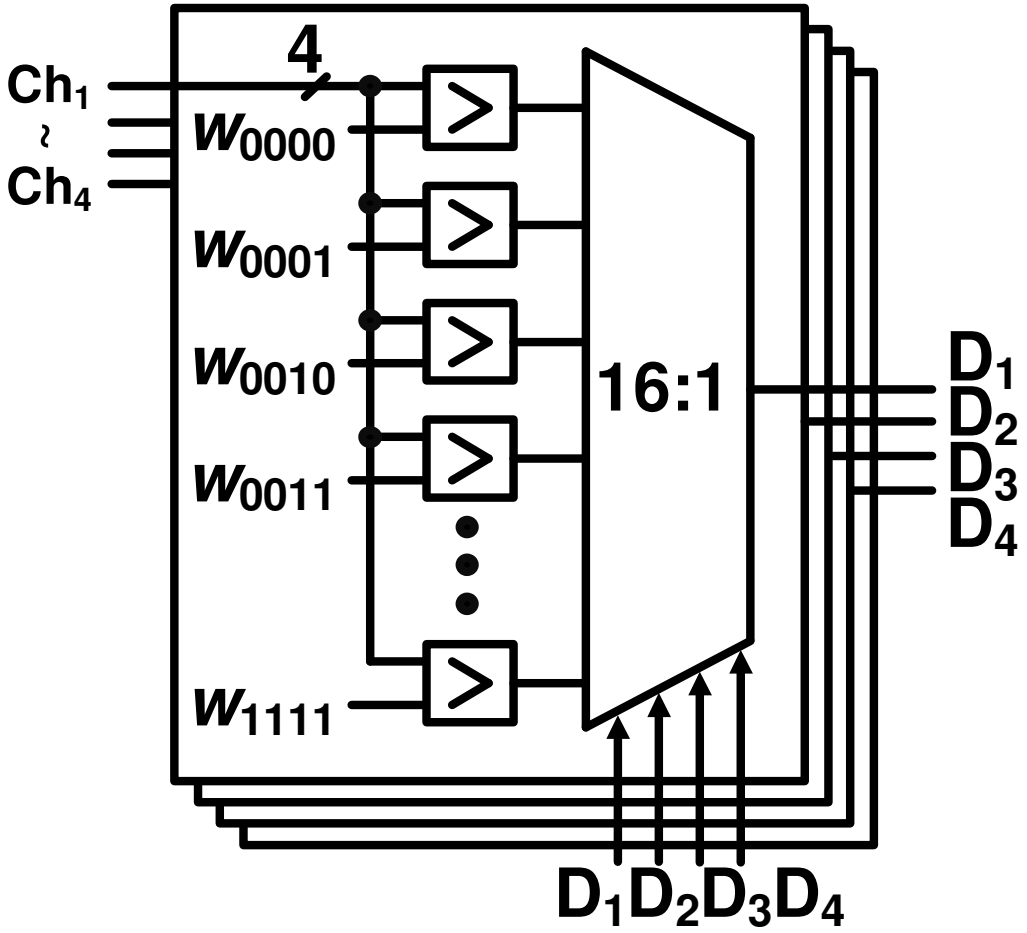
- High linearity between input and output delay @ 2GHz operation

4-bit TDC



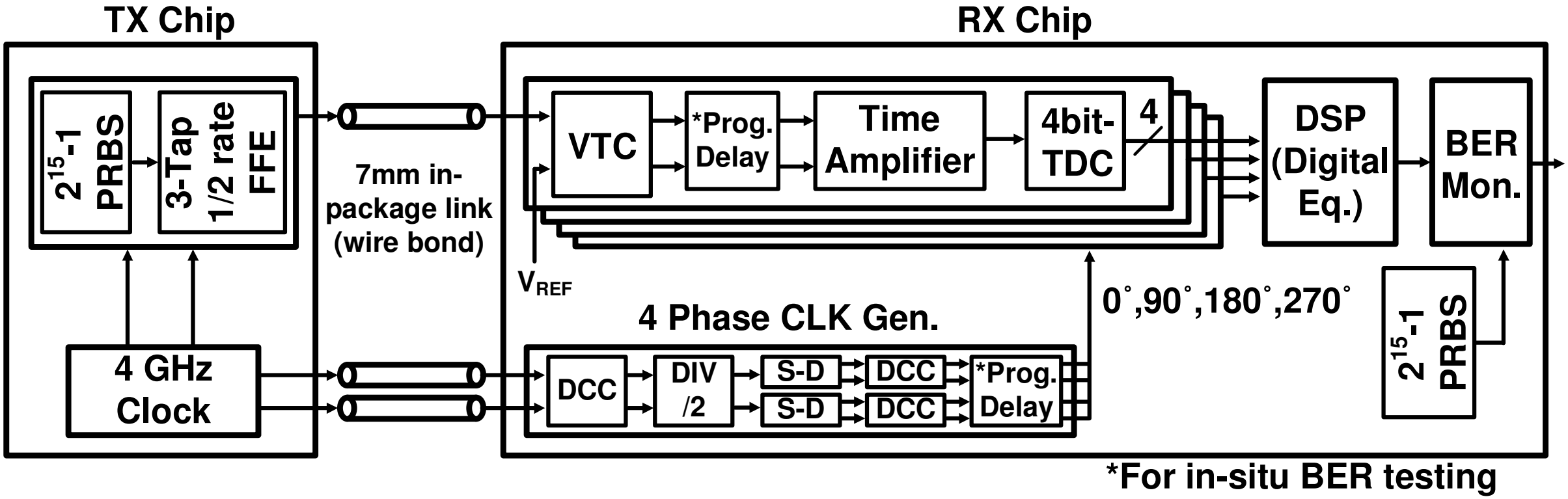
- Conventional 4-bit Vernier line TDC
- Total TDC delay should smaller than 1 UI

Digital DFE



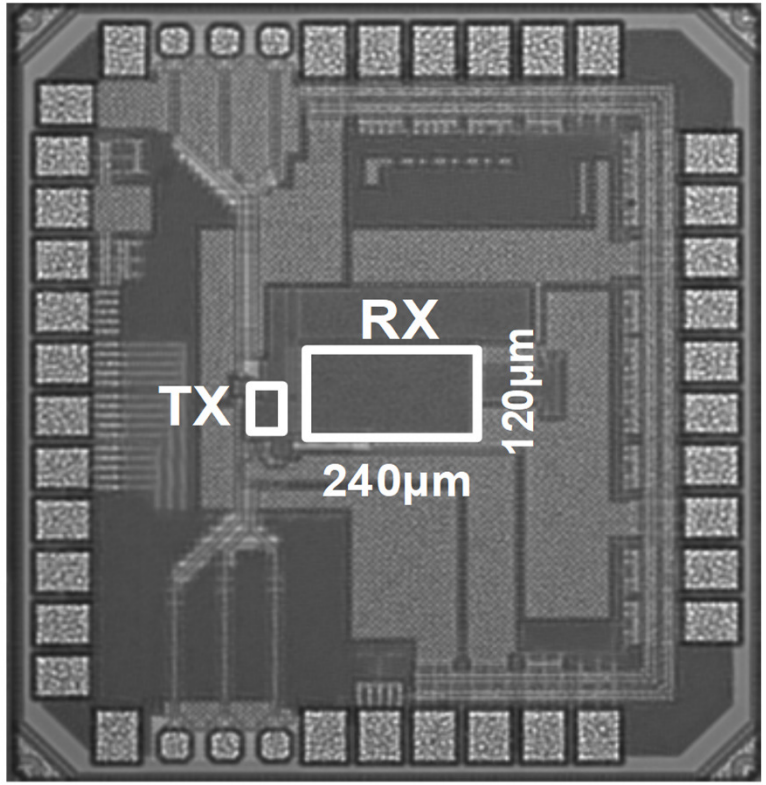
- 4-bit digital comparator
- TDC output compared with predetermined weights

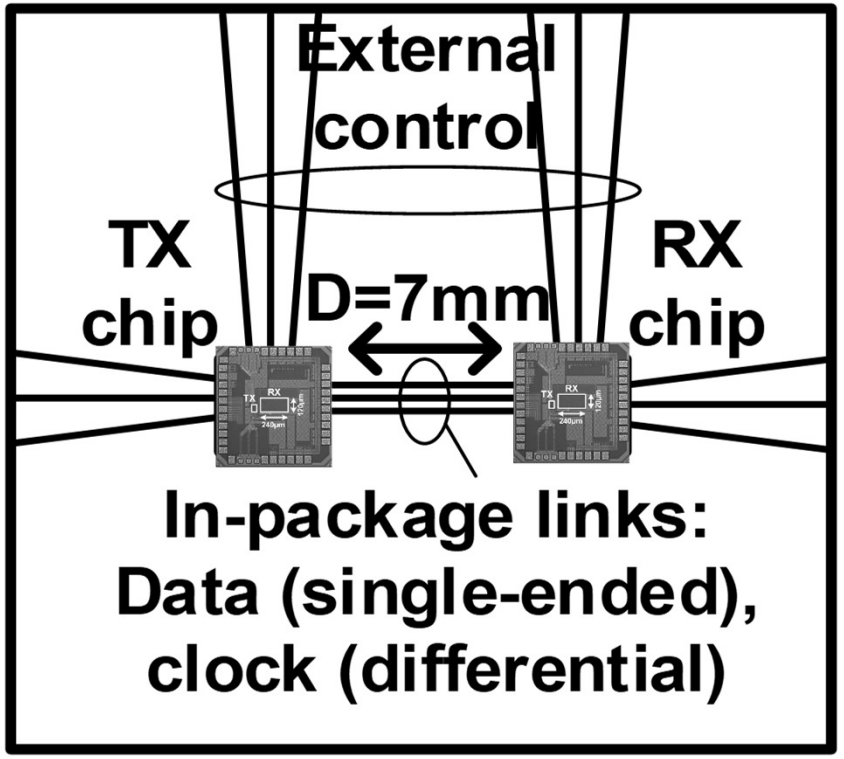
Proposed Transceiver for SiP



- Transmitter: PRBS, FFE and clock
- Receiver: 4-lane time-based receiver, digital equalization and BER monitor

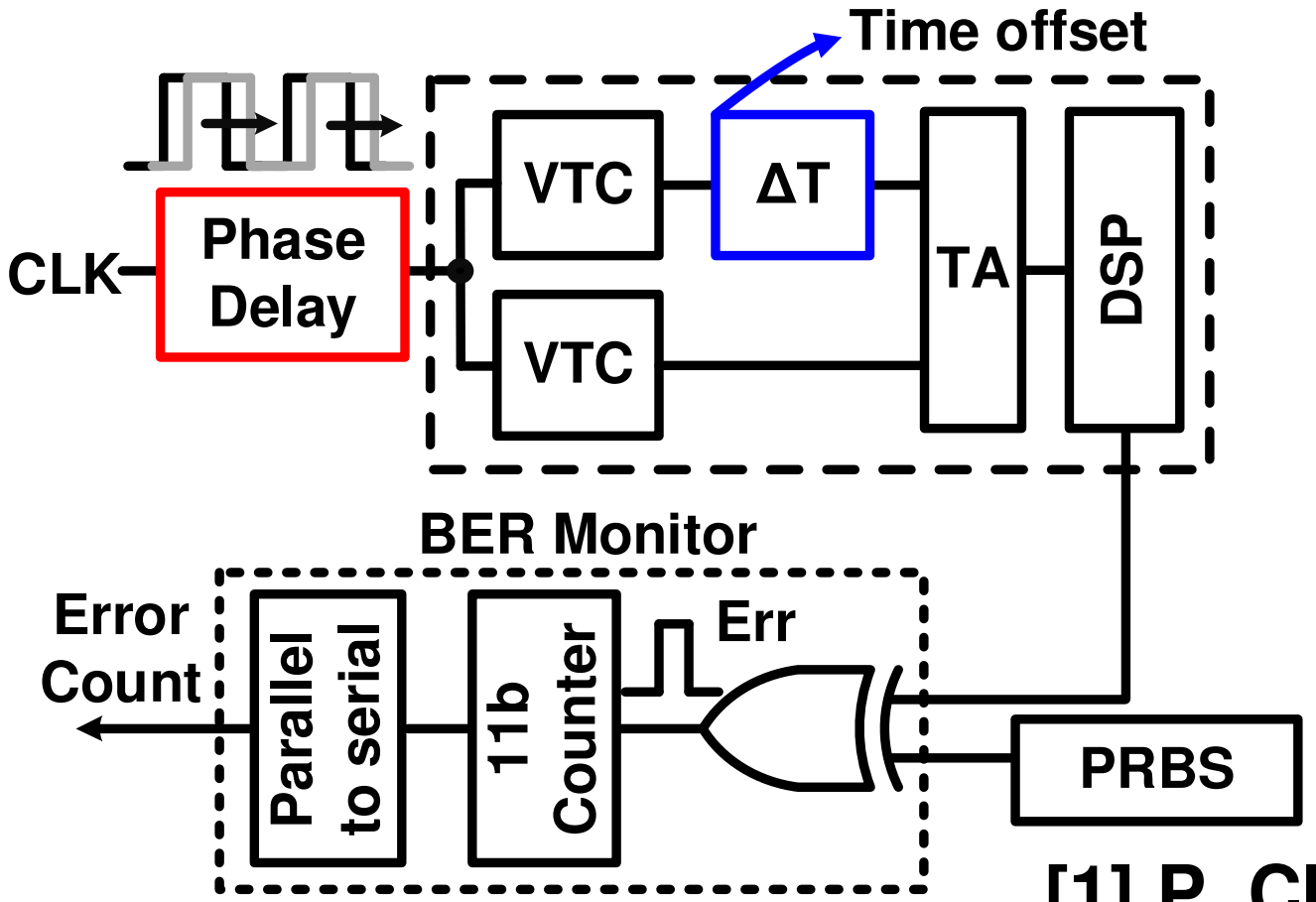
65nm Test-Chip and Photo

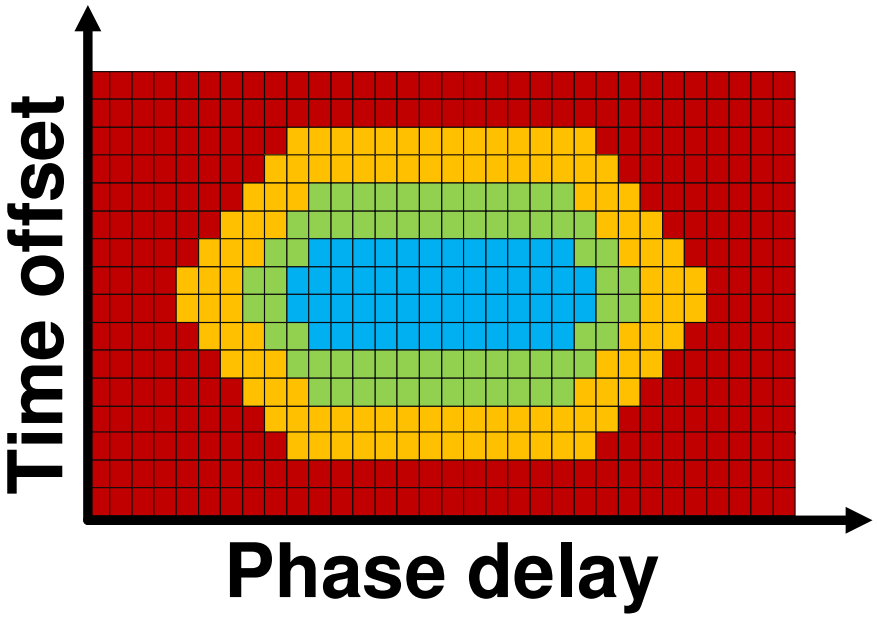




- **TX and RX chip are integrated in same package**

In-situ BER Eye-Diagram Monitor

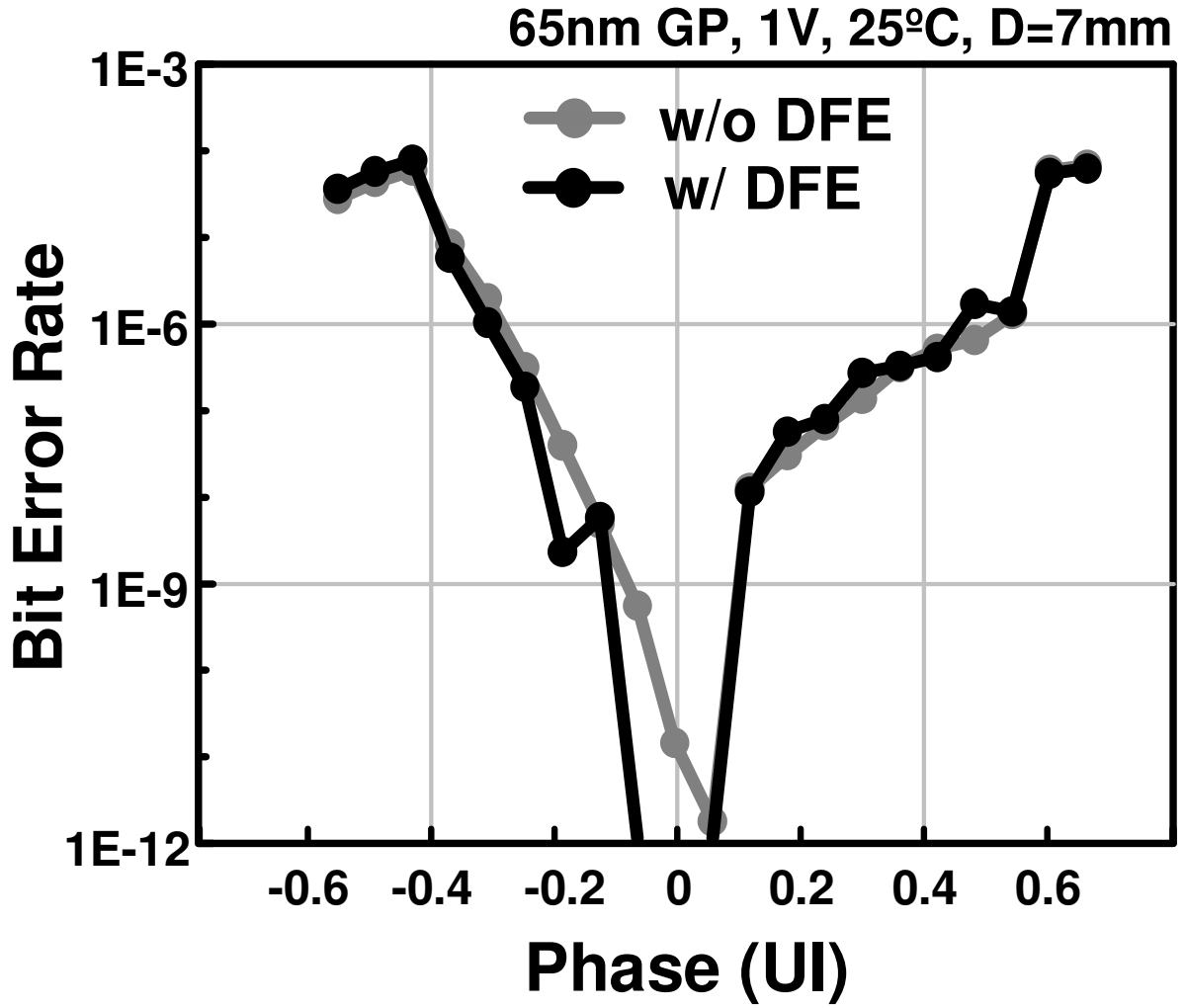




[1] P. Chiu, et al., JSSC, 2018.

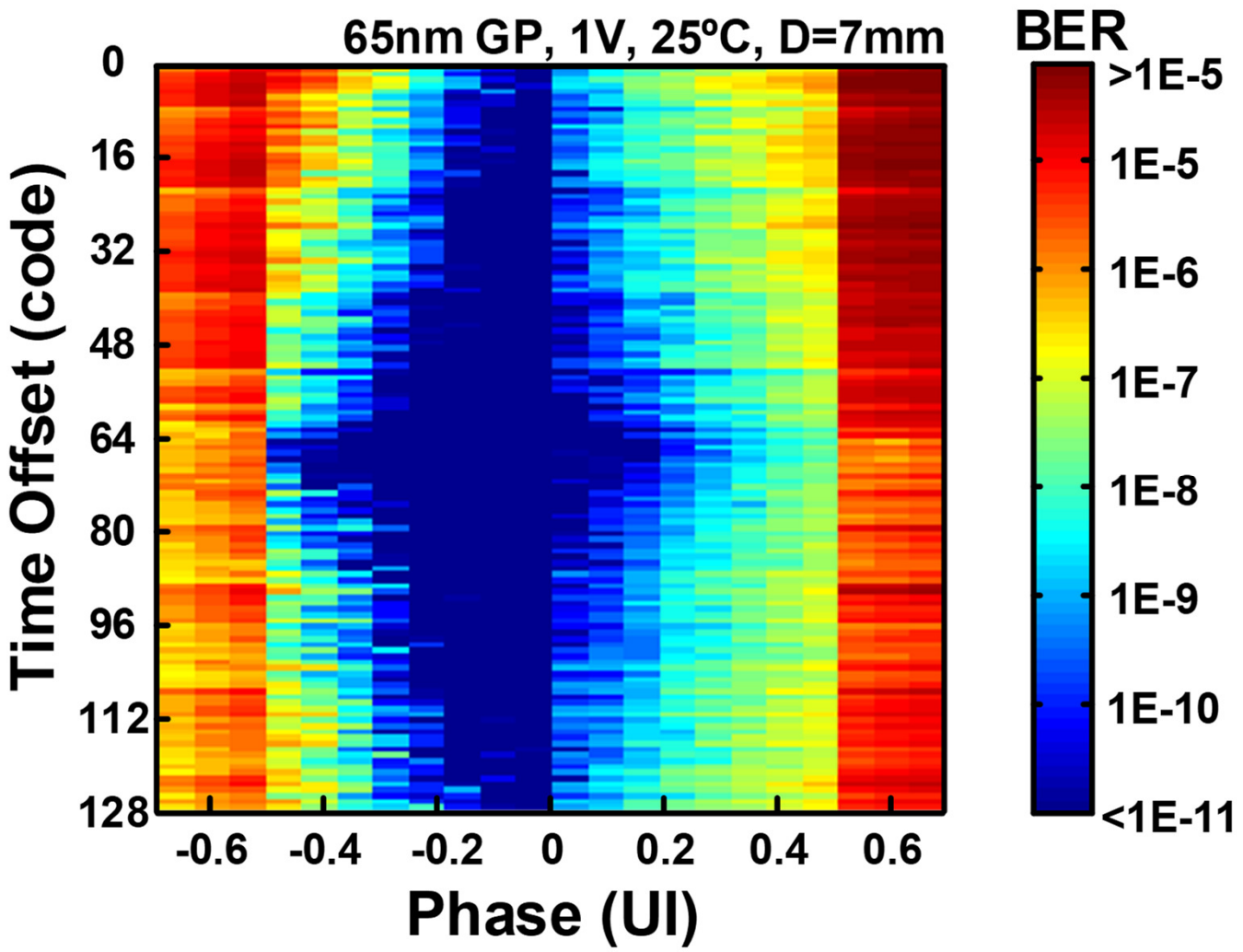
- X-axis: Phase delay in red box
- Y-axis: Time offset in blue box

Measured BER Bathtub



- Eye width = 0.12UI @BER < 10^{-12}

Measured BER Eye Diagram



- Y-axis: time offset code corresponds to voltage offset

Performance Summary

	JSSC'12 [3]	JSSC'13 [4]	JSSC'15 [5]	JSSC'16 [6]	This work
Application	Off Chip	Off Chip	Off Chip	Off Chip	SiP
RX Architecture	4x Flash ADC	4x Flash ADC	4x Flash ADC	32x SAR ADC	4x TDC
Front-end Type	Voltage-Based (CTLE +VGA)	Voltage-Based (VGA)	Voltage-Based (VGA)	Voltage-Based (Analog FFE)	Time-Based (VTC+TA)
Data Rate	10 Gb/s	10.3125 Gb/s	8.5-11.5 Gb/s	10 Gb/s	8 Gb/s
Technology	65nm	40nm	40nm	65nm	65nm
Voltage	1.1V	0.9V	1V	1V	1V
Resolution	4 bit	6 bit	6 bit	6 bit	4 bit
BER	<1E-9	<1E-12	<1E-12	<1E-10	<1E-12
RX Area (w/o DSP)	0.288 mm^2	0.27 mm^2	0.82 mm^2	0.38 mm^2	0.0192 mm^2
Power Efficiency (pJ/b)	8.1 (RX only)	15.1 (RX only)	18.9 (RX, includes Clock)	7.9 (RX only)	2.1 (TX+RX, includes DSP power)

Conclusion

- Digital-intensive time-based front-end receiver is proposed for SiP application
- The proposed time-based receiver achieves an energy-efficiency of 2.1 pJ/b while the area is 0.0192mm^2
- The proposed VTC and TA based implementation significantly reduces circuit complexity and has favorable scaling properties