A 10Gb/s 10mm On-Chip Serial Link in 65nm CMOS Featuring a Half-Rate Time-Based Decision Feedback Equalizer

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Abstract

An all-digital 2-tap half-rate time-based decision feedback equalizer (TB-DFE) was demonstrated on a 10mm on-chip serial link. Implemented in a 65nm GP technology, the transmitter and receiver achieve an energy-efficiency of 31.9 and 45.3 fJ/b/mm, respectively, at a data rate of 10Gb/s. A Bit Error Rate (BER) less than 10^{-12} was verified for an eye width of 0.43 Unit Interval (UI) using an in-situ BER monitor.

Introduction

On-chip serial links are attractive for high-speed point-to-point applications as they can achieve 10Gb/s or higher data rates without using power-hungry and floorplan-disrupting repeaters. Several circuit techniques have been proposed to improve the communication speed and energy-efficiency of on-chip serial links. Some recent examples include charge-injection based feedforward equalization [1], capacitive based de-emphasis [2], and current mode transceiver with active inductor [3]. However, these analog-intensive approaches are susceptible to PVT variation and suffer from headroom issues at low operating voltages. Moreover, they do not take full advantage of the technology scaling benefits and require considerable design effort to implement in a new technology.

Decision feedback equalization (DFE) has now become indispensable for improving the performance of off-chip links, however they have not been adopted widely in on-chip links due to the large power consumed by the current mode logic (CML) circuits required for high-speed operation. In an effort to make DFE more digital-friendly and amenable to technology scaling, we propose a time-based DFE technique where the weighted sum filter operation is performed entirely in the time domain. Our digital intensive approach utilizes inverters and digitally-controlled delay elements that can be readily designed in advanced technologies. Another advantage of the proposed TB-DFE is that a higher number of taps can be incorporated by simply adding more delay stages.

Time-Based DFE

A comparison between conventional and proposed TB-DFE is shown in Fig. 1. The output voltage of a conventional CML based DFE can be expressed as $V_{DFE} = V_{RX}(t) + \sum_i x[n-i] \cdot w_i$ where x[n-i] is the preceding binary data and w_i is the weight of each tap. This voltage is determined by the current through the multiple pull-up and pull-down paths in the CML circuit, and is converted to a binary value by a slicer. The proposed time-based scheme converts the voltage signal into a time delay, and the basic operation can be described as $T_{DFE} = T_{RX}(t) + \sum_i x[n-i] \cdot w_i$. Delay $T_{RX}(t)$ is a function of the incoming channel voltage $V_{RX}(t)$ which is equalized using the previous binary outputs x[n-i] and weights w_i. The phase detector (PD) compares the phase difference between the DFE path and the reference path to generate a binary output. This is equivalent to the slicer operation in a conventional DFE, but in the time domain.

Fig. 2 shows the operation example of the proposed TB-DFE for a bit sequence of '0100'. Due to channel inter-symbol-interference (ISI), the received voltage signal $V_{RX}(t)$ will be distorted, which results in a smaller sensing margin between data '1' and data '0' in the time domain. The reduced phase difference between the DFE path signal N_{DFE} and reference path signal N_{REF} may lead to an incorrect decision. The TB-DFE feedback loop can enhance the phase difference by utilizing the previous decision data and DFE weights w_i.

65nm Transceiver Design

Fig. 3 shows the 10mm on-chip transceiver system we implemented in a 65nm GP test chip. It consists of a half-rate feed forward equalizer (FFE) on the transmitter side, and an inverter based TIA followed by a TB-DFE on the receiver side. TX data is generated by a 2^{15}-1 pseudo random bit generator (PRBS). A high-swing voltage-mode output driver with a 3-tap half-rate FFE de-emphasizes the output signal and transmits data over a 10 mm channel. The output driver is implemented using a bank of inverters with resistors connected between the driving transistors and channel for TX impedance matching. An inverter based TIA containing a bank of programmable transmission gates enables RX impedance matching. An in-situ BER monitor was implemented for BER bathtub and eye diagram measurements.

Details of the 2-tap half-rate TB-DFE are shown in Fig. 4. Each delay stage is composed of three parallel tri-state inverters, an always-enabled inverter, and three MOS capacitors to support high speed operation and fine-grain programmable delays. The first delay stage is controlled directly by the analog voltage $V_{RX}(t)$ while the second delay stage is controlled by the binary feedback data. The third stage serves as the offset delay ΔT for eye diagram measurements, which is equivalent to the offset voltage in conventional DFEs. The inverter based implementation significantly reduces the circuit complexity and makes it easier to re-design the DFE circuit in a new technology. To further optimize the circuit, one of the two taps was folded into the reference path with a complementary weight configuration. With the modification, the number of inverters and capacitors is cut down by half which also reduces power consumption and chip area. A zero-offset aperture PD was adopted in our design [4].

In-situ BER Monitor and Measurement Results

Fig. 5 shows the proposed circuit for in-situ BER bathtub and eye diagram measurements. The programmable phase delay allows the clock to sample data over a 2 UI range. Since the proposed TB-DFE converts voltage into time, instead of sweeping the voltage offset, we sweep the time offset ΔT to create the BER eye diagram. This was implemented by adding a third delay stage in the TB-DFE delay lines which allows the delay offset to be swept up to one tap delay. The BER monitor compares the TX data from the 2^{15}-1 PRBS with the DFE output. Finally, the error count is tallies and serially read out. Fig. 6 shows the bathtub curves with and without TB-DFE for two consecutive bits. The TB-DFE lowers the BER floor from 10^{-10} to 10^{-12} while ensuring an eye width of 0.43 UI. Fig. 7 shows the BER eye diagram. The delay offset was swept from 0ps to 18ps using a 6-bit control code. Fig. 8 shows the energy-efficiency and data rate measured at different supply voltages. To save test time, only the data point at 1.2V is based on a BER criteria of 10^{-12} while the other data points are for a BER of 10^{-9}. The die photo and summary table are shown in Figs. 9 and 10, respectively. The transmitter and receiver blocks (not including the BER monitor) achieve an energy-efficiency of 30.9 and 45.3 fJ/b/mm, respectively, at a data rate of 10 Gb/s.

References [1] B. Kim et al., ISSCC, 2009. [2] D. Walter et al., ISSCC, 2012. [3] S. Lee et al., ISSCC, 2013. [4] S. Kundu et al., ISSCC, 2016. [5] M. Chen et al., VLSI, 2015.

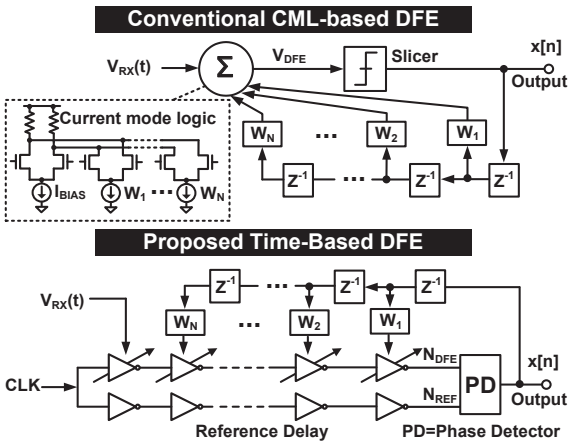

Fig. 1. Conventional DFE and time-based DFE.

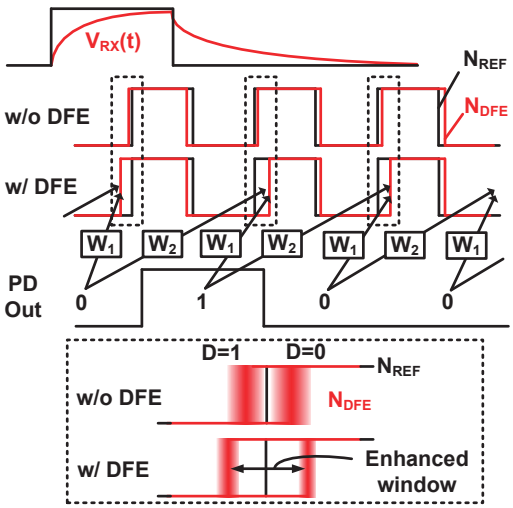

Fig. 2. Illustration of time-based DFE compensation for data stream '0100'. The time difference window expands with DFE.

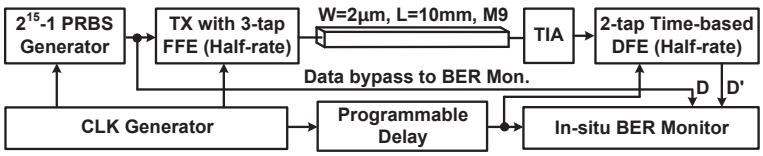

Fig. 3. Block diagram of 10mm on-chip serial link test chip.

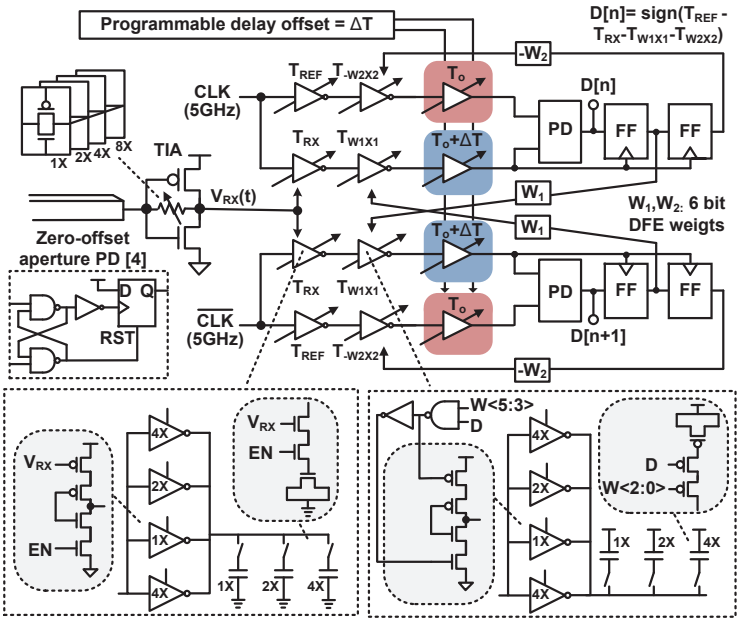

Fig. 4. Half rate 2-tap time-based DFE circuit implementation.

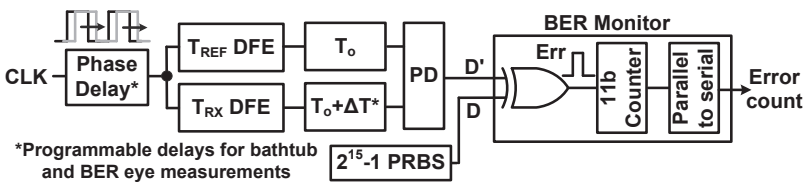

Fig. 5. Circuit blocks used for bathtub and BER eye diagram measurement.

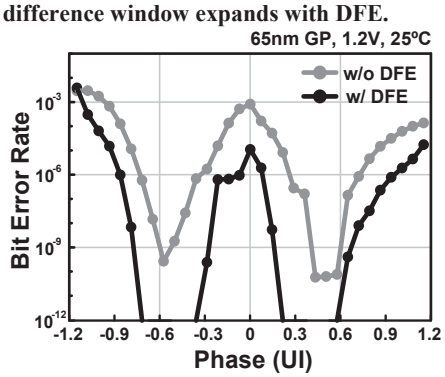

Fig. 6. Measured BER bathtub curves (<10^{-12}) for two consecutive bits.

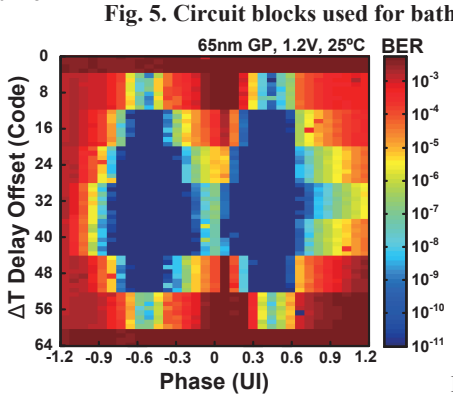

Fig. 7. Measured BER eye diagram for two consecutive bits.

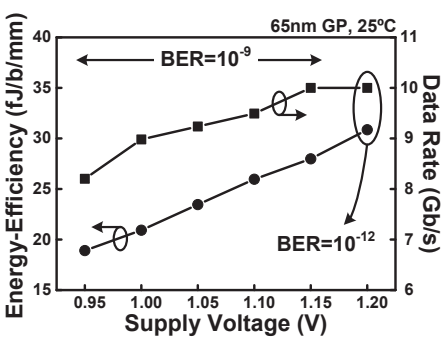

Fig. 8. Supply voltage versus data rate and energy-efficiency.

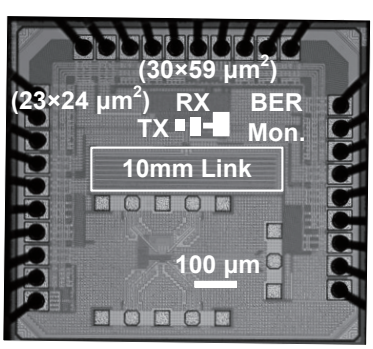

Fig. 9. 65nm chip micrograph

	ISSCC'09 [1]	ISSCC'12 [2]	ISSCC'13 [3]	VLSI'15 [5]	This work	
Technology	90nm	65nm	65nm	65nm	65nm	
TX and RX	Current mode driver+TIA	Voltage mode driver+sense amp.	Current mode driver+sense amp.	CTLE-based repeater	Voltage mode driver+TIA	
Features	No DFE	No DFE	No DFE	No DFE	2-tap TB-DFE	
Data Rate	4Gb/s	10Gb/s	3Gb/s	4Gb/s	10Gb/s	
Throughput (Gb/s/µm)	2	2.56	0.75	4	2	
Link Length	10mm	6mm	10mm	2.5mm+2.5mm	10mm	
BER Bathtub	< 10E-6	< 10E-12	< 10E-12	< 10E-12	< 10E-12	
BER Eye	Yes (< 10E-6)	No	Yes (< 10E-12)	No	Yes (< 10E-11)	
Energy Efficiency (fJ/b/mm)	35.6	174	9.5	48.4	TIA	14.4
					DFE	30.9
					FFE	31.9

Fig. 10. Comparison with state-of-the-art on-chip serial links.