An 8-bit Analog-to-Digital Converter based on the Voltage-Dependent Switching Probability of a Magnetic Tunnel Junction

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***equal contribution**

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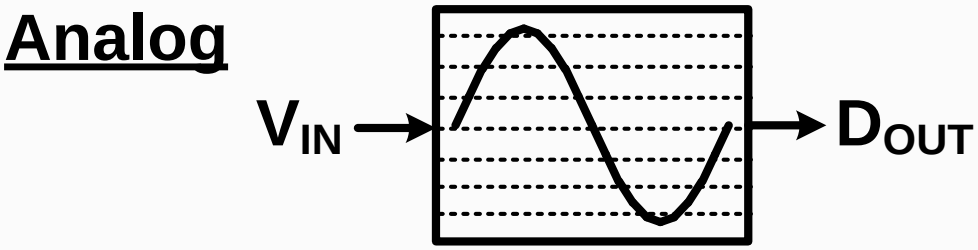
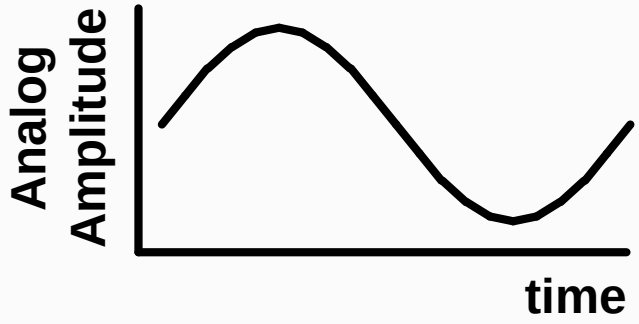
Outline

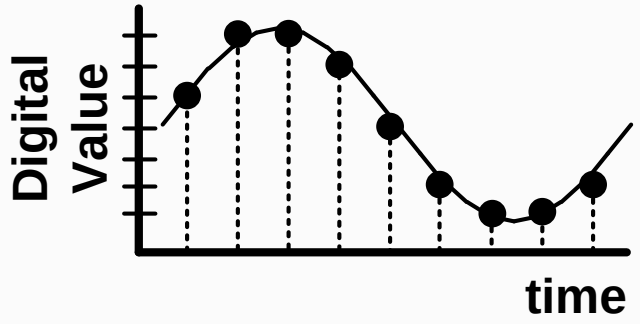
- **Background**
  - **Analog-to-Digital Converter (ADC)**
  - **Magnetic Tunnel Junction (MTJ)**
- **Proposed MTJ-based “Probabilistic” ADC**
- **Techniques for Improving Linearity and Input Voltage Range**
- **Summary**

Analog-to-Digital Converter (ADC)



Resolution: N bits
(=2^N quantization steps)

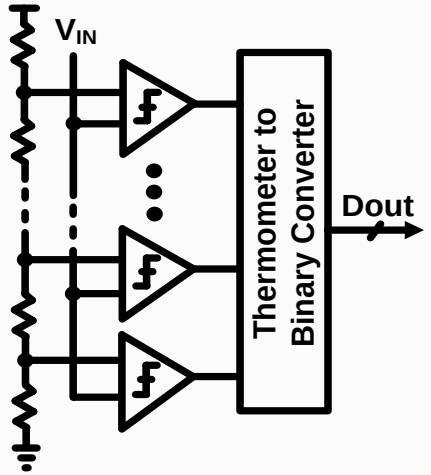




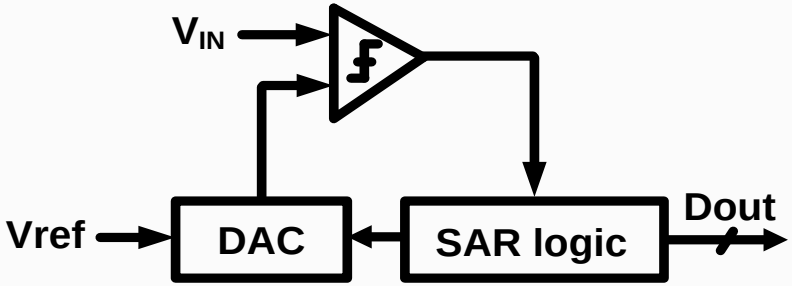
- **ADC converts an analog input voltage to a digital code**
- **An N-bit ADC quantizes an analog voltage into 2^N discrete levels**

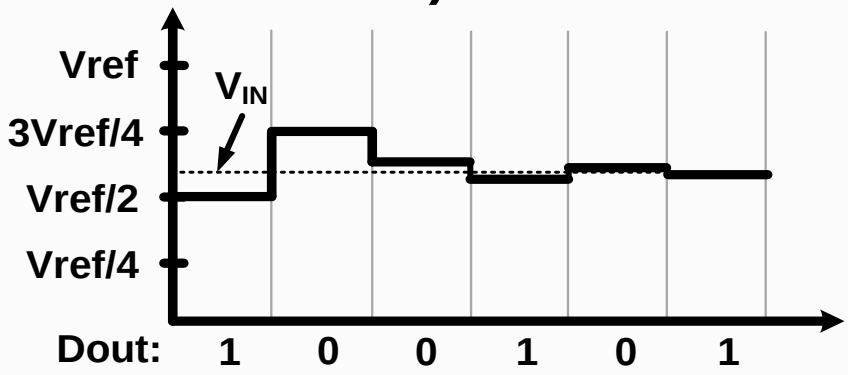
Traditional ADC Architectures

- **Flash ADC**
  - Fast conversion rate (up to several Gs/s)
  - High power consumption
  - Low resolution (2 ~ 8 bit)

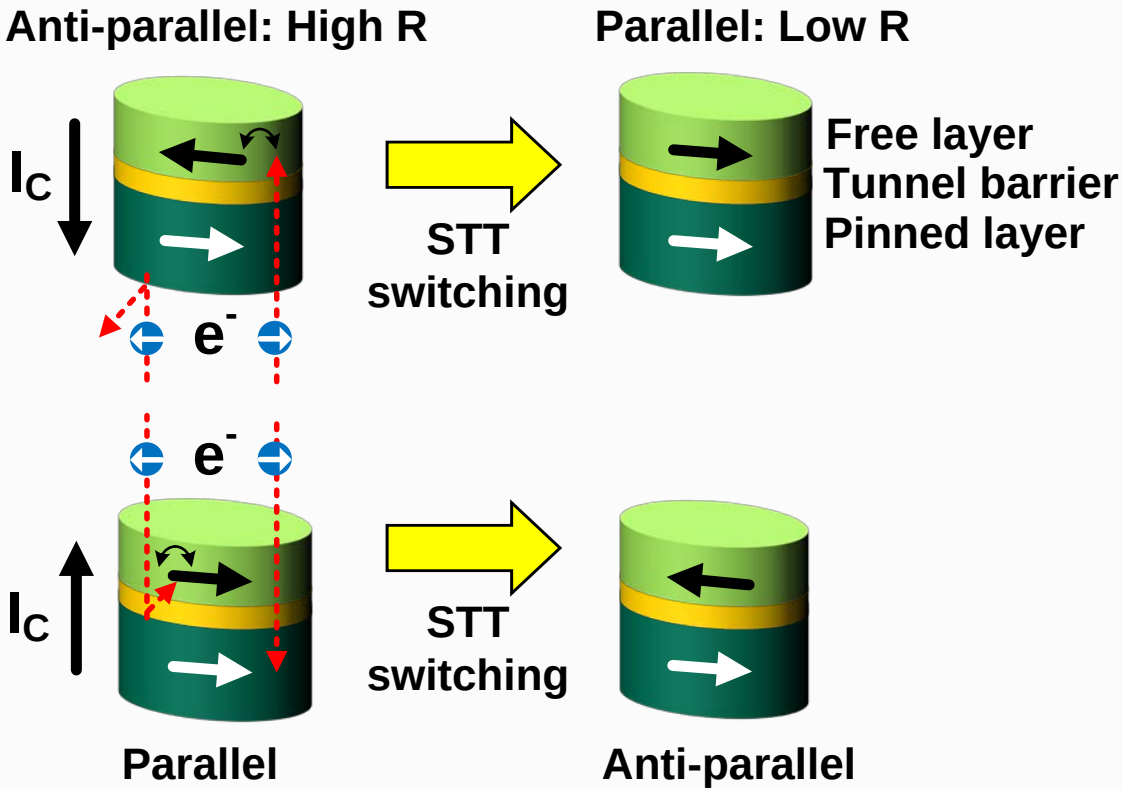


- **Successive Approximation Register (SAR) ADC**
  - High resolution (10 ~ 16 bit)
  - Low power consumption
  - Slow conversion rate (1Ks/s ~ several 100Ms/s)





Magnetic Tunnel Junction (MTJ)



- Basic storage element of STT-MRAM memory
- Spin polarized electrons rotate the magnetization of free layer using spin transfer torque

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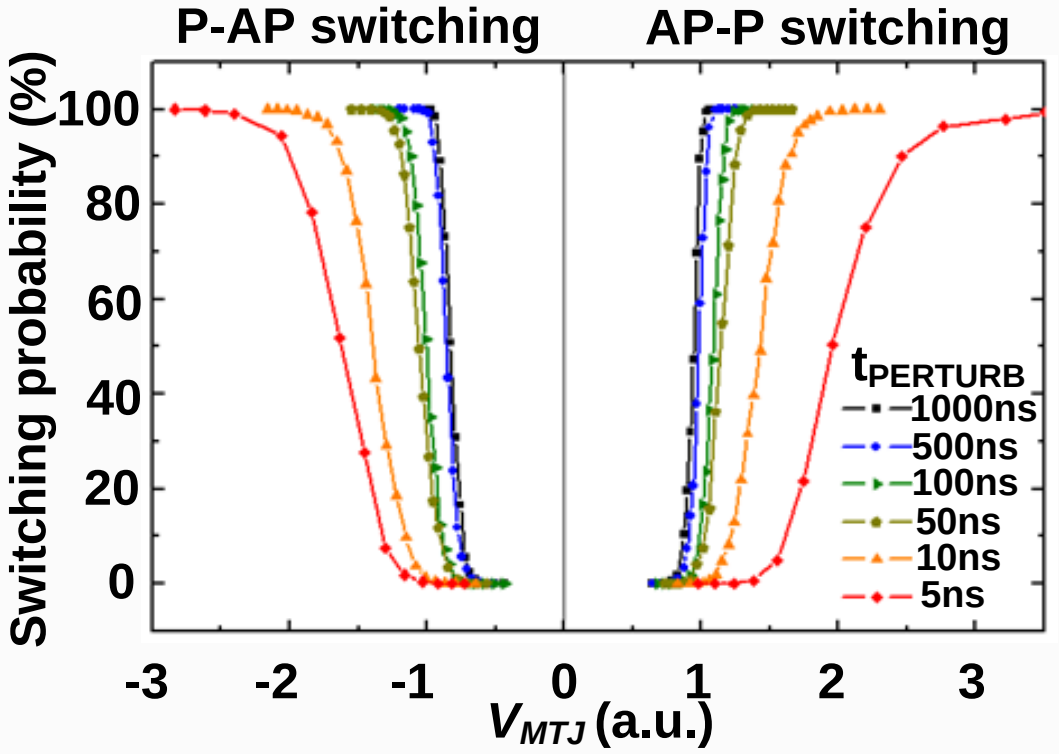
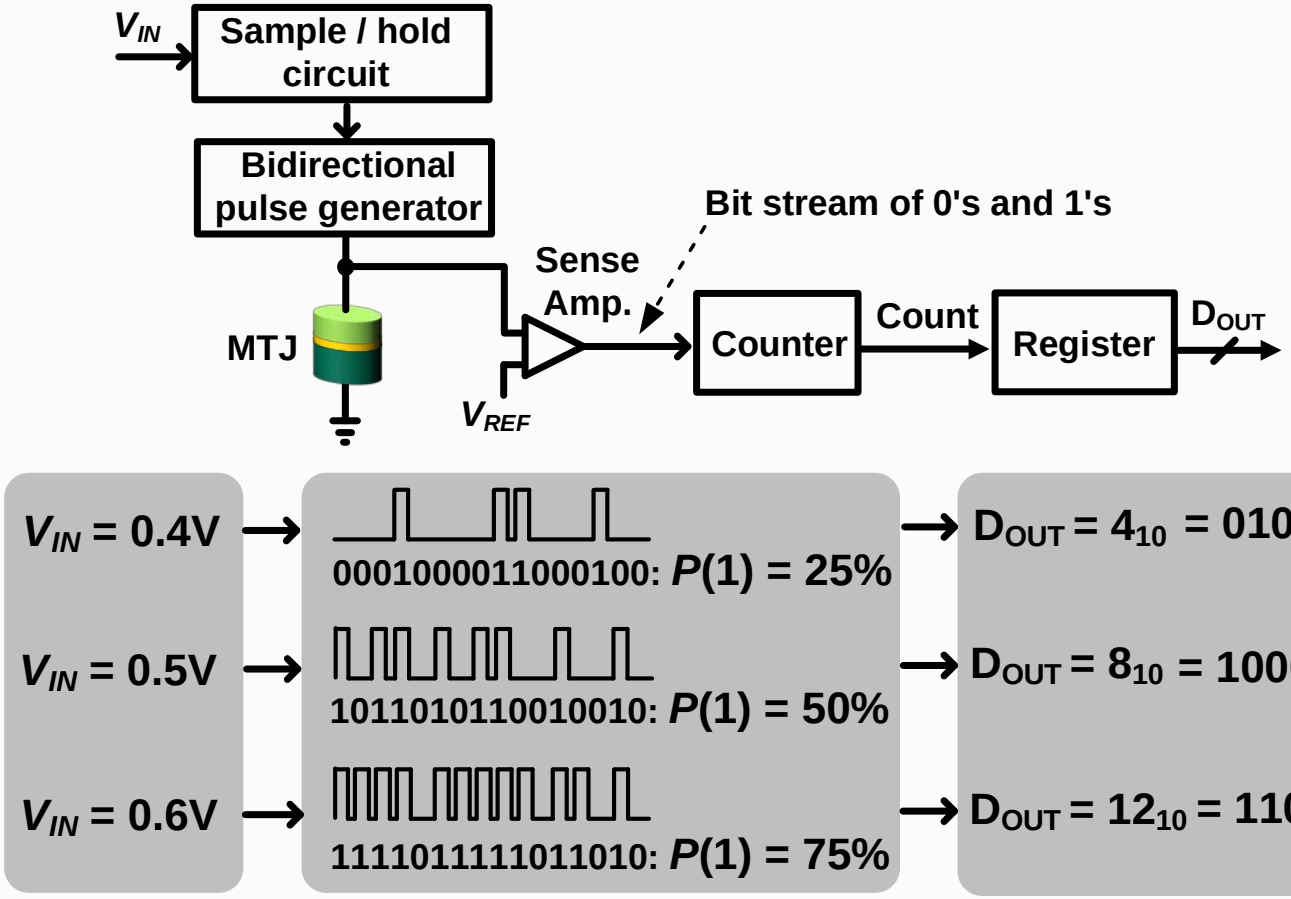
Switching Probability of an MTJ



H. Zhao, et al., TMAG, 2012.

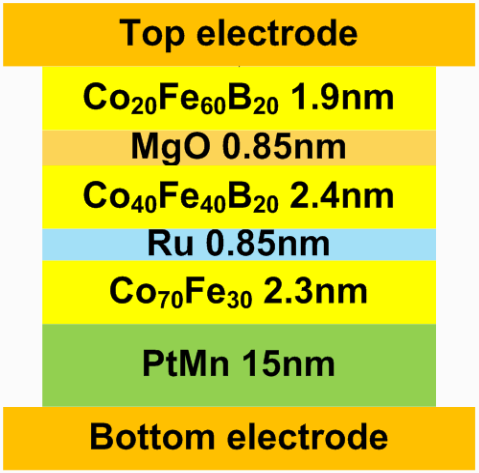
- **Switching probability depends on the applied analog voltage (V_{MTJ})**

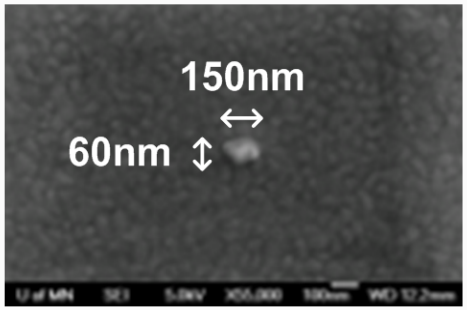
Proposed MTJ-Based "Probabilistic" ADC



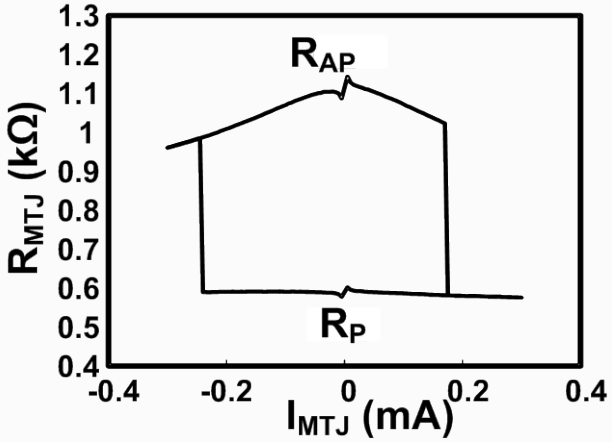
- **Analog voltage → random bit stream → compute probability of '1's → digital code**

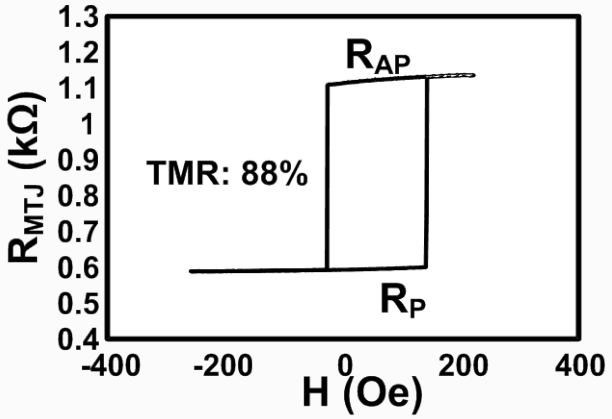
MTJ Device Used for Experiments





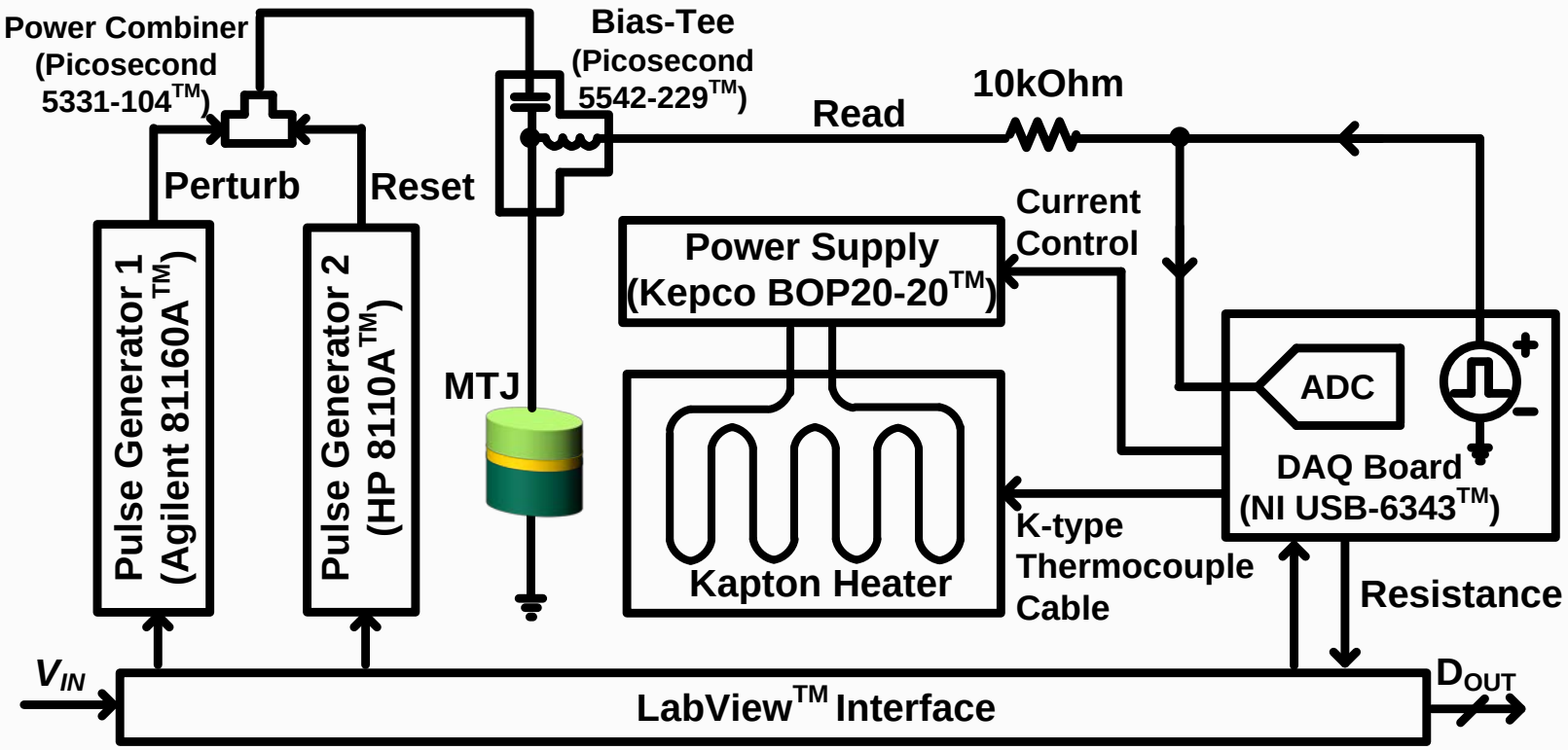
Dimension	150x60nm^2
RA	5.31 Ω·μm^2
TMR	88%
Thermal stability	64





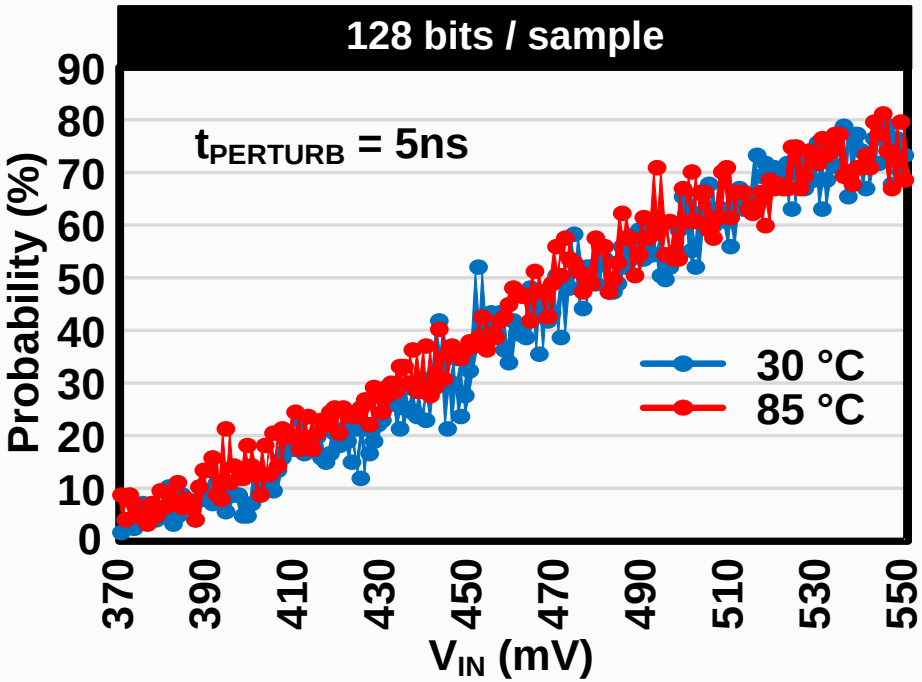
- **CoFeB based in-plane MTJ device with a TMR of 88% and a thermal stability of 64**

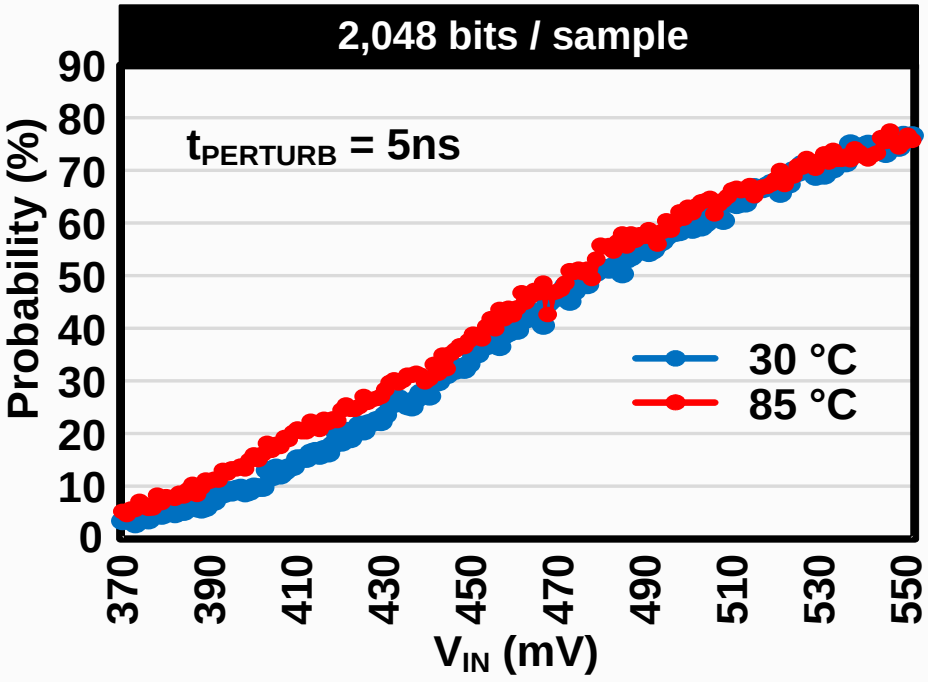
Experimental Setup



- **MTJ measurement setup with 1mV voltage resolution and <1℃ temperature accuracy**

Measured Switching Probability Curve



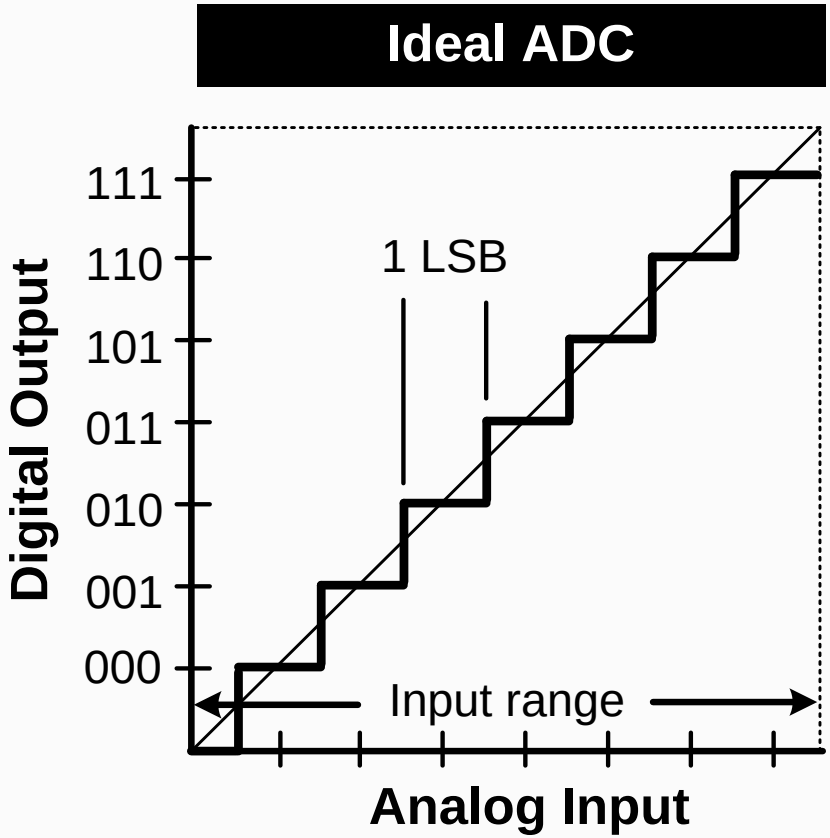


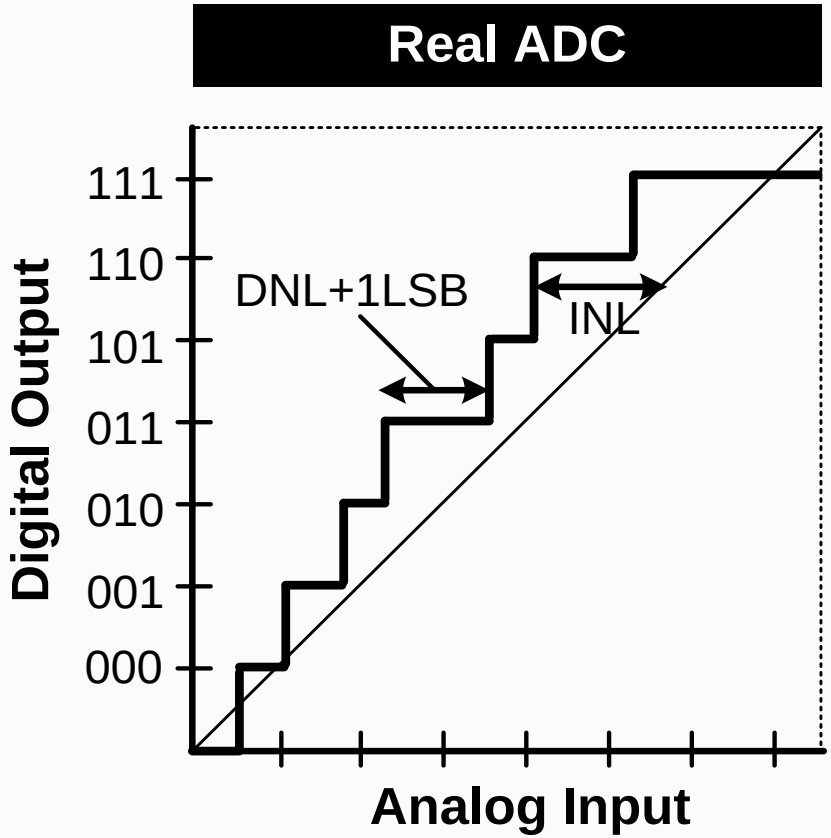
- A short 5ns $t_{PERTURB}$ used for suppressing thermal activation switching
- Averaging more bits gives a smoother and more accurate probability curve (128 bits vs. 2,048 bits)
- Temperature sensitivity is acceptably low

ADC Non-Linearity Metrics:

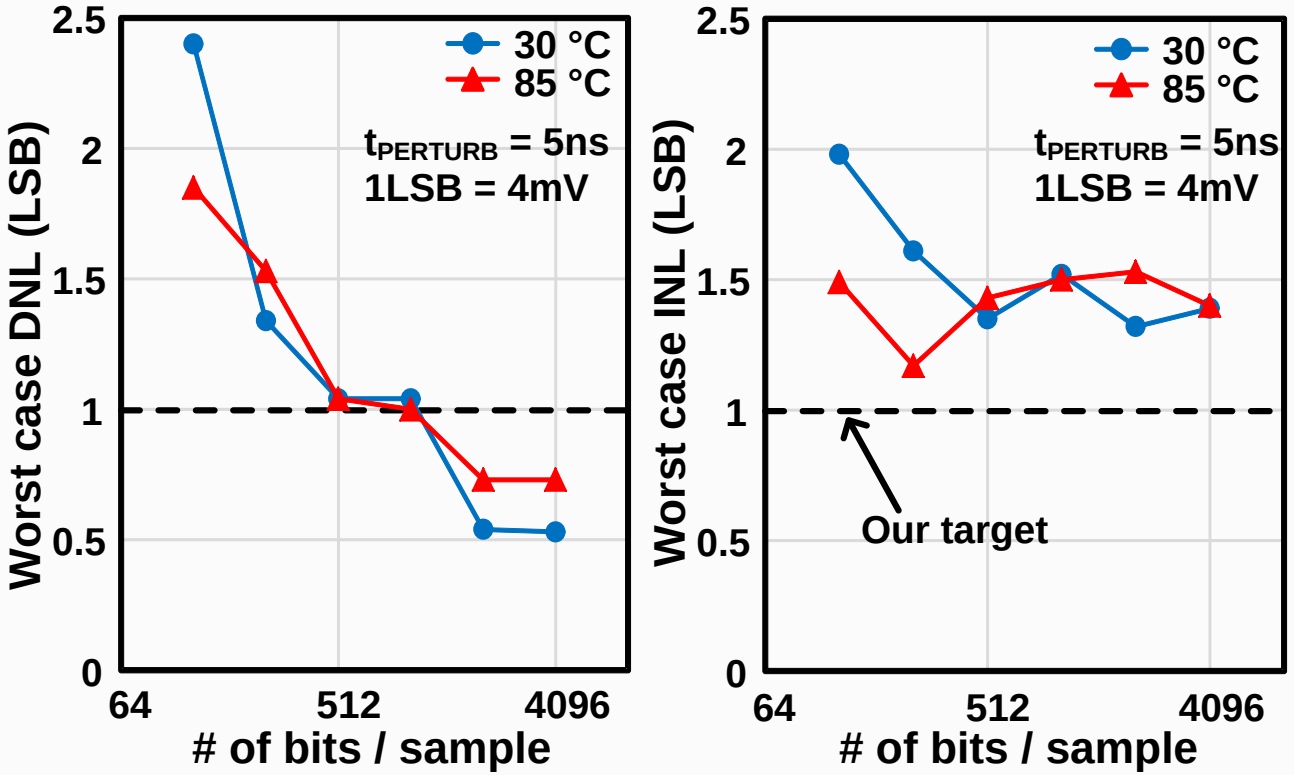
Differential Non-Linearity (DNL)

Integral Non-Linearity (INL)





Measured Worst Case DNL and INL



- A 5-bit ADC resolution is assumed (i.e. 1LSB = 4mV)
- DNL of 1 LSB can be achieved by averaging more random bits (e.g. 2,048 bits)
- INL cannot be improved by simply averaging more bits

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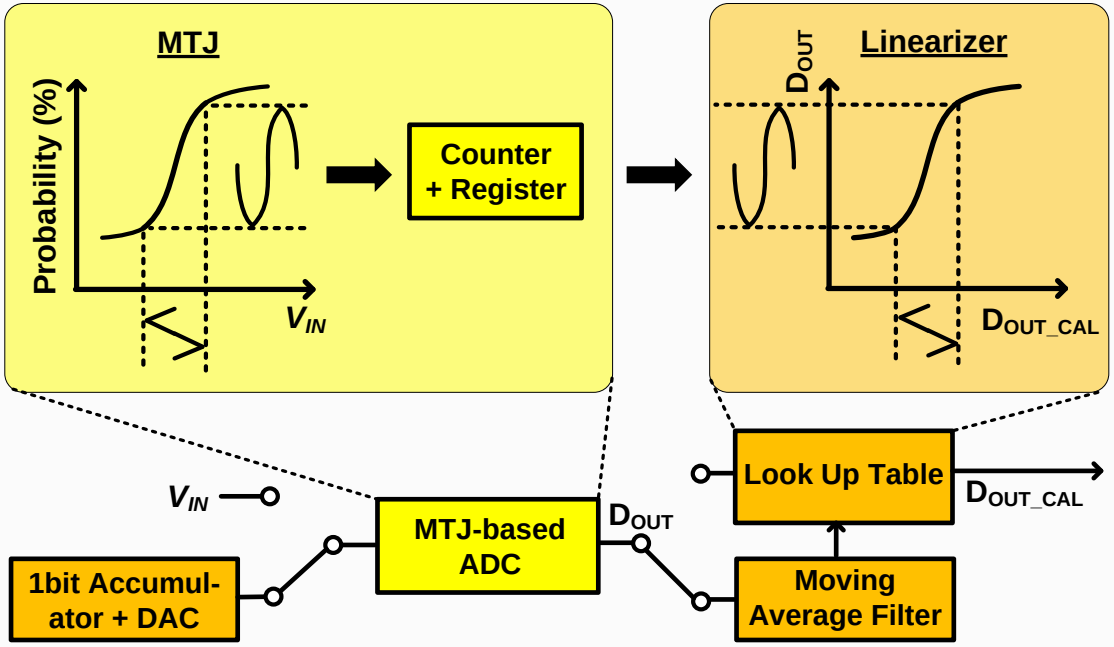
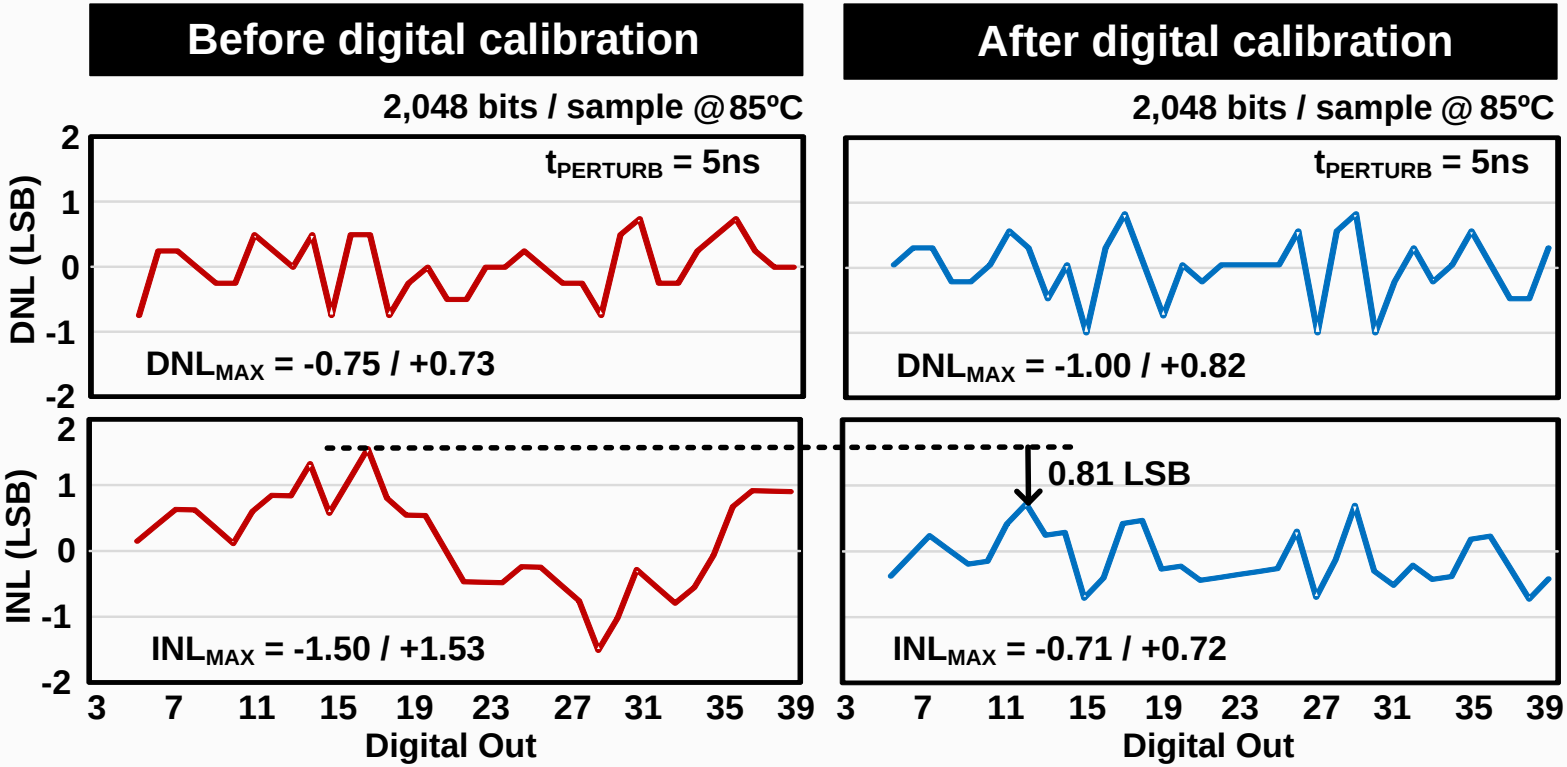
One-time Digital Calibration for Improving INL



J. Kim, et al., TCAS-I, 2010, J. Daniels, et al., VLSI Circuits Symposium, 2010.

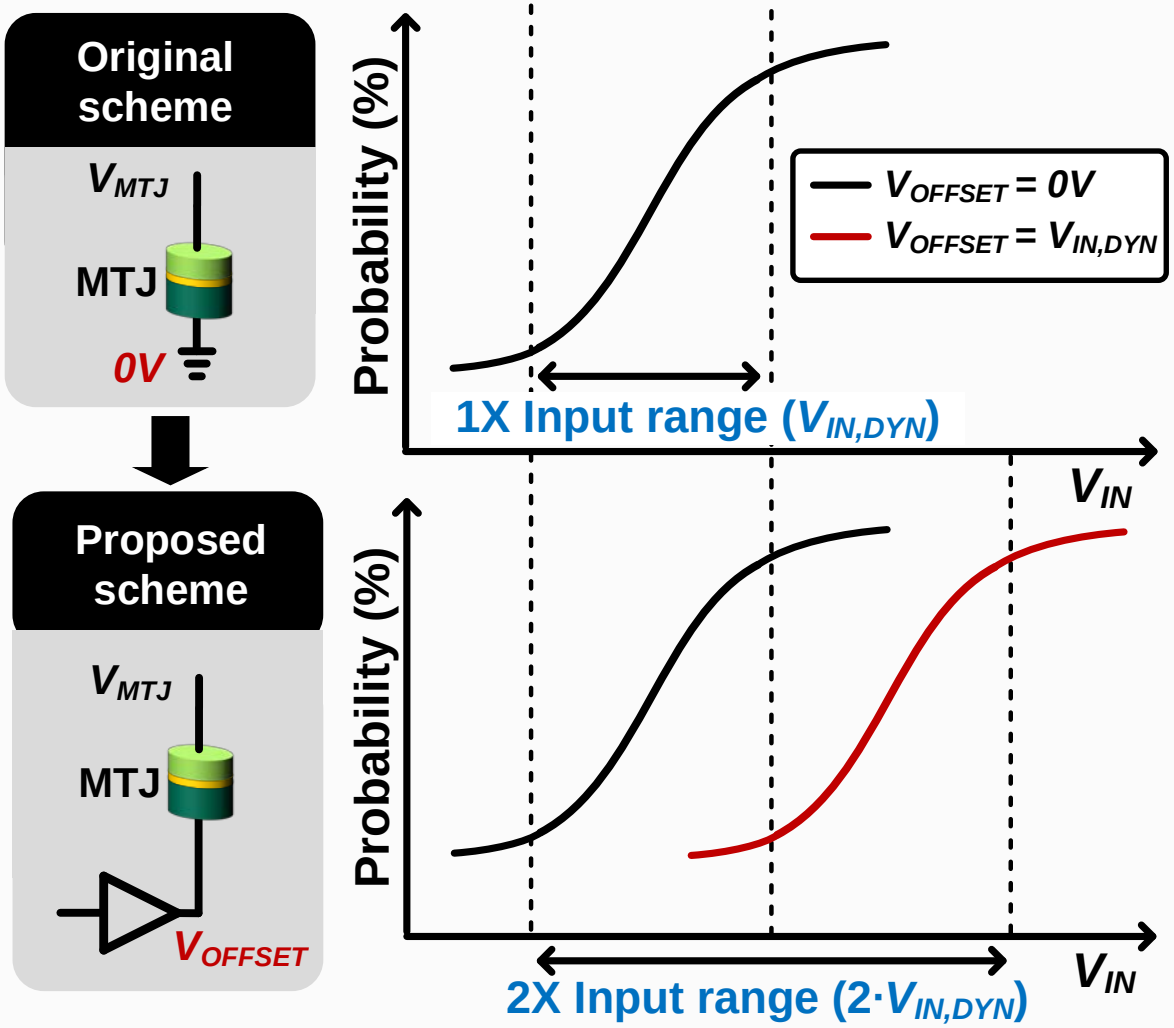
- **Basic idea: Pre-calibrate MTJ transfer curve and store the inverse function in a look-up table to compensate for inherent non-linearity**

Measured DNL and INL @ 85℃

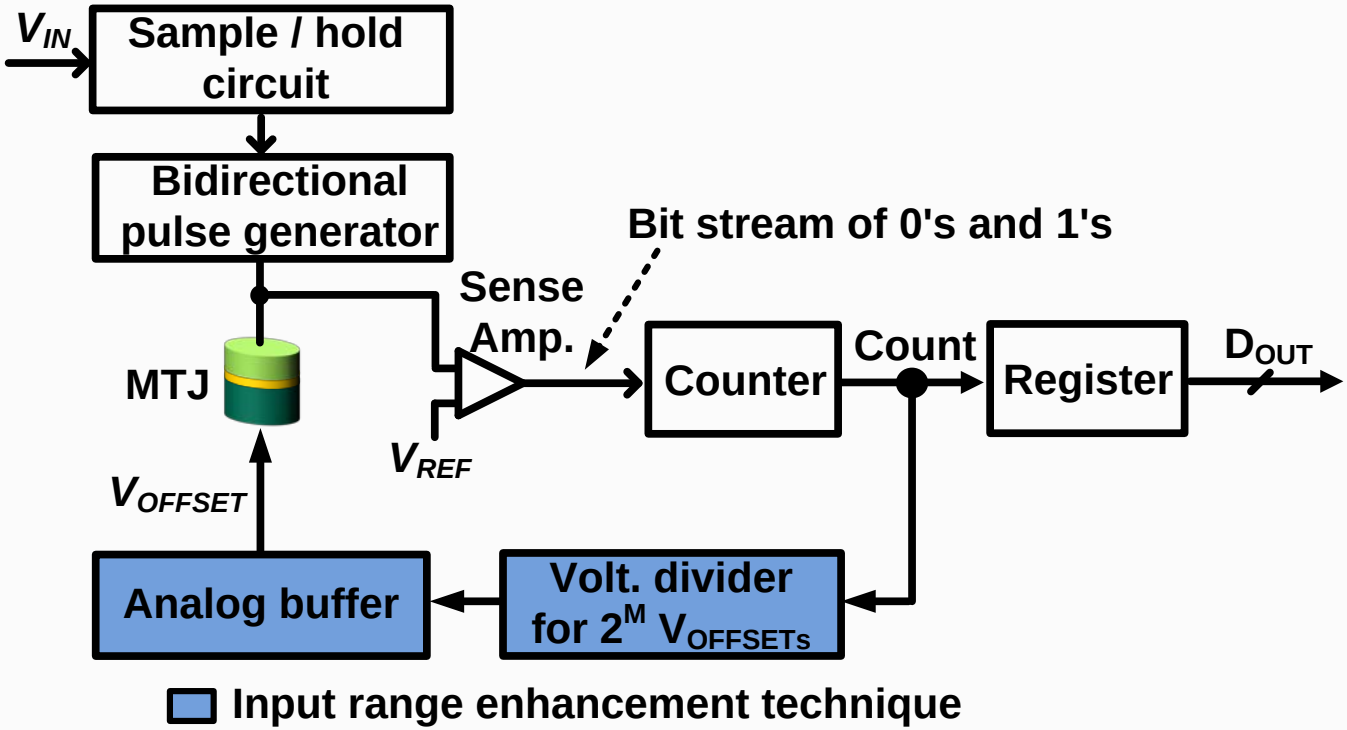


- **Target DNL / INL of 1 LSB can be met after one-time calibration**
- **ADC resolution limited to 5-bit due to narrow input voltage range**

Proposed Input Range Enhancement Technique

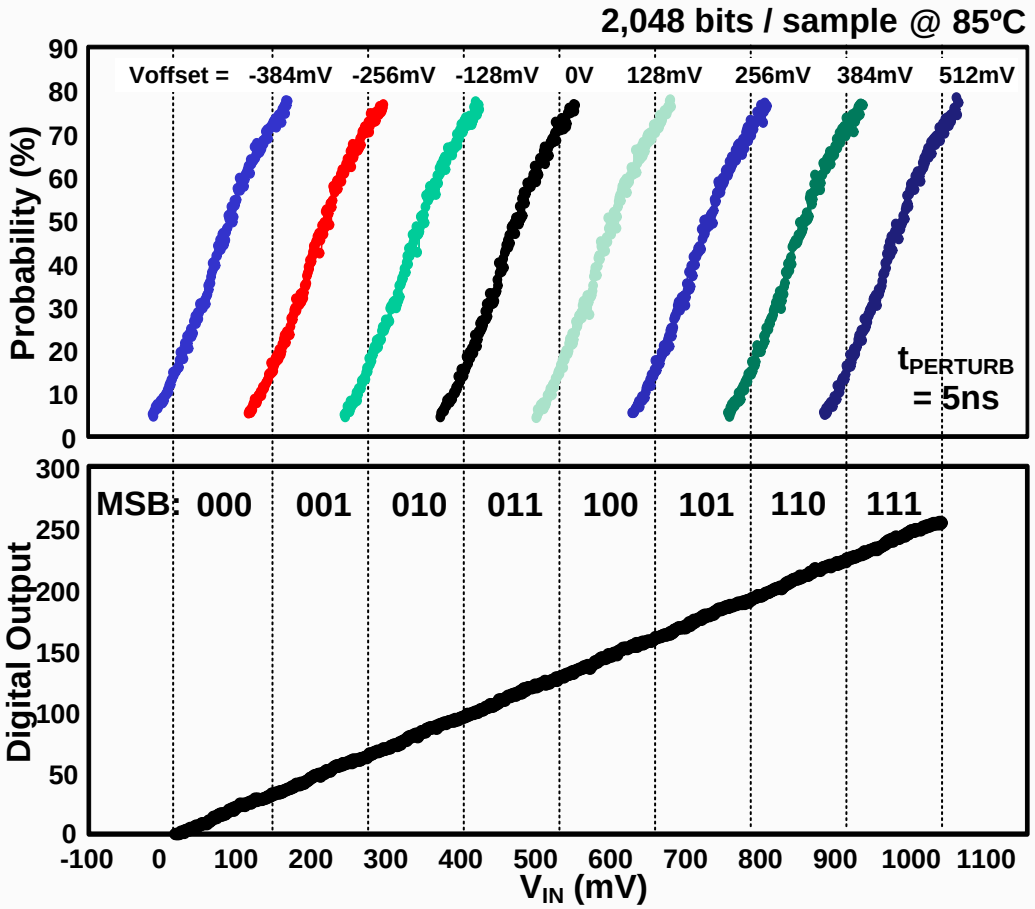


Implementation of Input Range Enhancement Technique



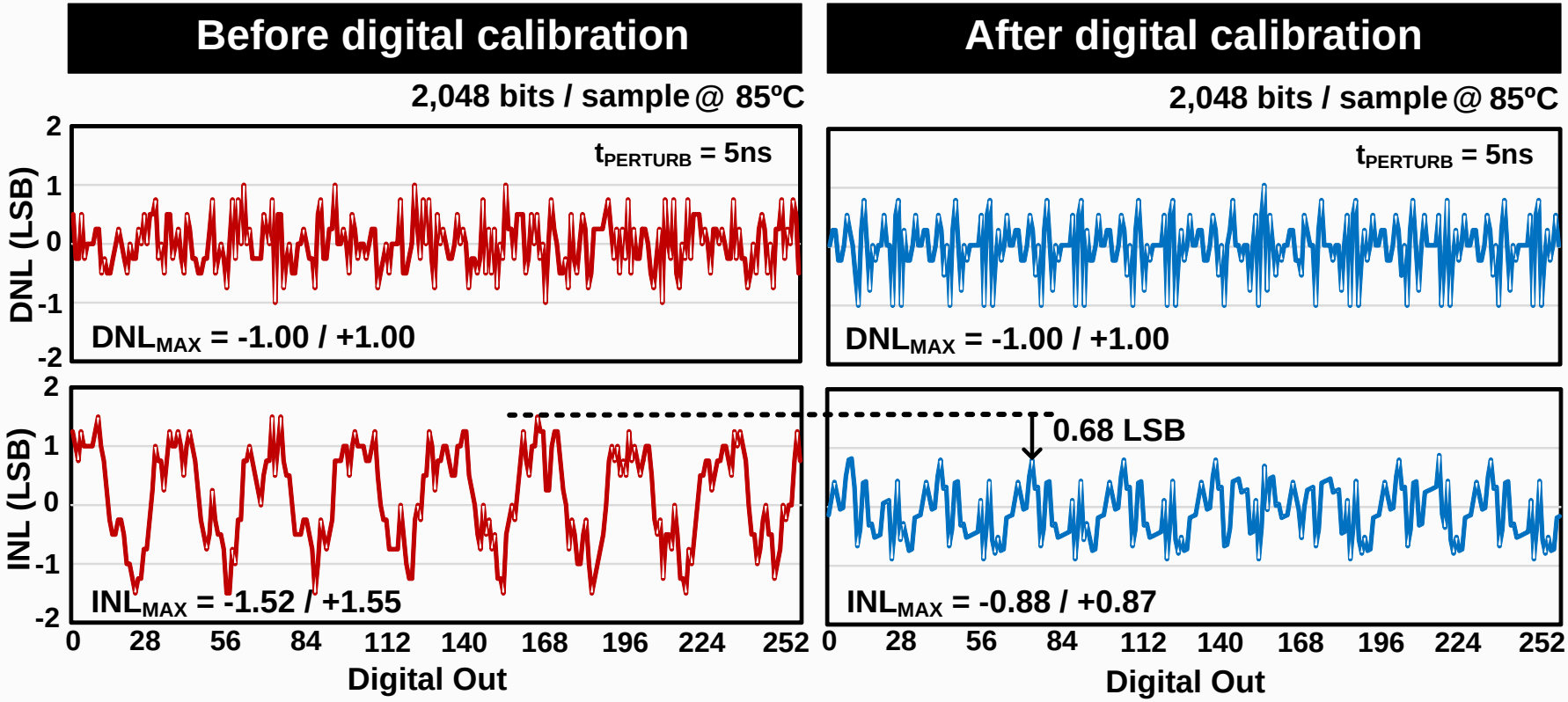
- A voltage divider and an analog buffer control the MTJ bottom node voltage

Measured Probability and Corresponding Digital Output



- 8x wider input voltage range → 3 additional bits

Measured DNL and INL @ 85℃



- Target DNL / INL of 1 LSB can be met after calibration
- 8-bit ADC resolution with good linearity is achieved

ADC Performance Summary

2,048 bits / sample

		30 ºC			85 ºC		
	Input range	DNL_{MAX} (LSB)	INL_{MAX} (LSB)	Bits	DNL_{MAX} (LSB)	INL_{MAX} (LSB)	Bits
Original MTJ-based ADC	128mV (X1)	0.74	1.32	5	0.75	1.53	5
+ Digital calibration	128mV (X1)	1.00	0.76	5	1.00	0.72	5
+ Digital calibration + Input range enhancement	1024mV (X8)	1.00	0.84	8	1.00	0.88	8

- **ADC resolution (=8 bit) was limited by the minimum voltage step (=1mV) of pulse generator. Actual resolution could be as high as 14 bits.**

Summary

- **An 8-bit resolution MTJ-based ADC with excellent linearity demonstrated for the first time**
  - **2,048 bits averaged to generate one ADC sample**
  - **Insensitive to temperature using a 5ns pulse width**
  - **Digital calibration and input range enhancement techniques**

Acknowledgement

- **This work was supported in part by C-SPIN, one of six centers of STARnet, a Semiconductor Research Corporation program, sponsored by MARCO and DARPA**