An 8bit, 2.6ps Two-Step TDC in 65nm CMOS Employing a Switched Ring-Oscillator Based Time Amplifier

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***Abstract*- An 8bit two-step time-to-digital converter (TDC) with a novel digital switched ring-oscillator based time amplifier (TA) is demonstrated in 65nm CMOS. The proposed TA achieves a predictable and programmable gain without requiring any calibration. The implemented 8bit two-step TDC with a 16x TA gain achieves a time resolution of 2.6ps at 80MS/s conversion rate while consuming 2mW. The measured DNL and INL are 1.84LSB and 2.36LSB, respectively. The TDC area is 0.07mm^2.**

I. Introduction

Time-to-digital converters (TDCs) based on delay lines or Vernier delay lines have been used in a wide variety of applications including digital phase-locked loops (PLL), time-of-flight imagers, on-chip skew and jitter measurements, and nuclear experiments. Standard delay line TDCs have a wide input range but suffer from a poor time resolution since they cannot resolve a time difference shorter than a single inverter delay. Vernier delay line TDCs, on the other hand, can achieve a better time resolution by decreasing the delay difference between two delay lines and comparing the output samples from each delay stage. However, it also has limitations such as narrow input range, long conversion time and tight device-matching requirement. Time amplifier (TA) based TDCs (e.g. two-step and pipeline TDC) have been recently gaining traction as a promising approach for achieving both a wide input range and a high resolution by amplifying time residue from the coarse TDC stage and converting the amplified time residue to fine digital code at the subsequent fine TDC stages. However, previous TA techniques [1-3] have several limitations such as limited input ranges, unpredictable and unreliable gains that are susceptible to PVT variations. In this paper, we present a novel all-digital TA circuit with a precise gain control for wide input range based-on a ring oscillator (ROSC) that can switch between high and low frequency modes.

II. Switched Ring-Oscillator Based Time Amplifier

Fig. 1 shows the proposed TA circuit with its timing diagram before and after the ROSC switching operation. As shown in Fig.1, left, the TA consists of two identical switched ROSCs with NAND-based ROSC stages. Each ROSC stage has N+1 unit NAND gate cells connected in parallel and they are divided into two groups, ND1 and ND2. 1 out of N+1 unit NAND gate cells is assigned to group ND1 which is always turned on throughout the TA operation while the other N unit gate cells are assigned to group ND2 and can be either enabled (Fig. 1, left) or disabled (Fig. 1, right). The incoming early (Ai) and late (Bi) input signals are directly connected to the left-most ND2 gates of both ROSC circuits. Activation of RO1 and RO2 are staggered based on the rising edges of Ai and Bi. Since both ND1 and ND2 groups are enabled initially, both ROSCs are operating at their maximum oscillation frequency. The time input TIN (i.e. the time difference between the rising edges of two input signals) is converted to the corresponding phase difference (i.e. Φ_{IN}) between the two ROSC clocks, CK_{RO1} and CK_{RO2}. Then, a self-timed signal EN_{ND2} generated after a CK_{RO2}-to-Q and an inverter delay by the edge detector circuit disables all the ND2 gates. This causes the clock period of both ROSCs to be stretched out by a factor of N+1 as shown in Fig. 1, right. Finally, the edge detectors capture rising edges of the two ROSC clocks once

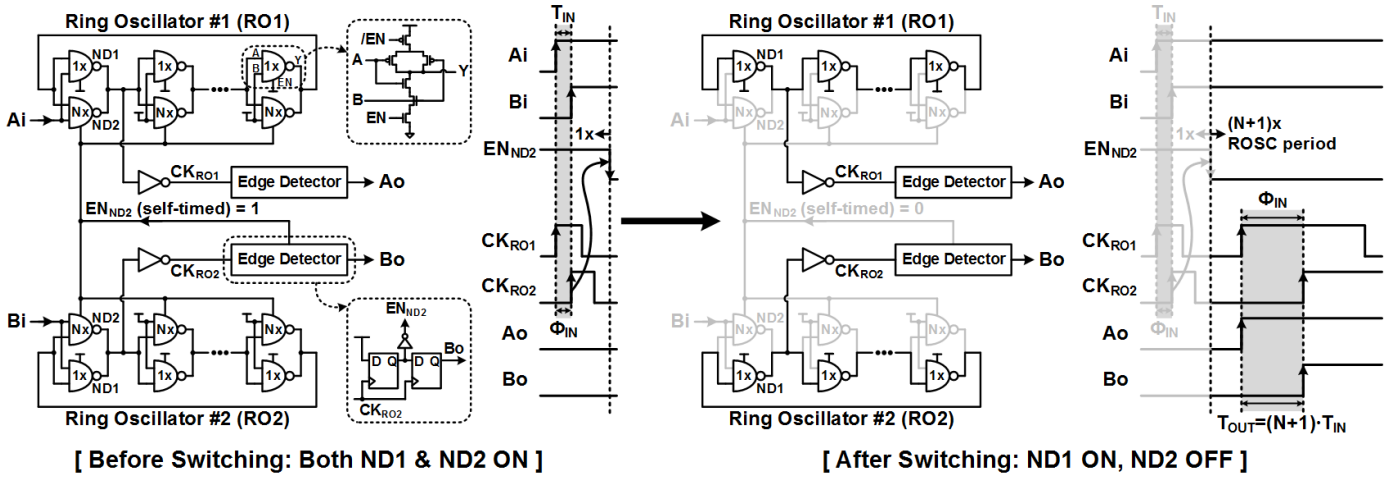


Fig.1. Proposed switched ring-oscillator based time amplifier circuit and its timing diagram before/after the switching operation.

the ROSC frequencies are settled. Since the ROSC phase difference is preserved when the ROSCs are switched to a low frequency mode, the equivalent time difference between the rising edges of the two ROSC clocks is now N+1 times longer (i.e. amplified by N+1 times) than the initial time difference due to the lowered ROSC frequencies. Note that the two ROSCs are switching to the lower frequency simultaneously and therefore intermediate ROSC frequencies from each ROSC during the switching operation are cancelled each other and does not affect the TA gain accuracy.

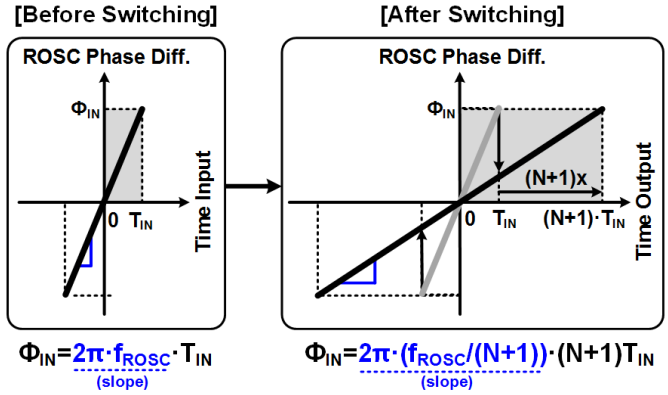


Fig.2. Switched ring-oscillator based time amplifier mechanism.

Fig. 2 describes the TA transfer characteristics. Before the ROSC clock periods are stretched out, time input (T_{IN}) is first converted to ROSC phase difference (Φ_{IN}) with respect to the ROSC frequency (f_{ROSC}) in high frequency mode. As shown in the equations in Fig. 2, the slope of the transfer curve is proportional to the ROSC frequency. Therefore, the slope is reduced by a factor of N+1 when the ROSC is switched to N+1 times lower frequency mode. Since the ROSC phase difference is unchanged after the switching, the corresponding time output becomes N+1 times longer than the time input as the slope has been reduced by N+1 times. The proposed TA technique can be implemented for an arbitrary integer gain by simply sizing the NAND gates accordingly.

III. Comparison with Existing Time Amplifiers

Fig. 3 shows three different existing TAs presented in the recent literature. Firstly, the SR-latch metastability based TA [1] in Fig. 3(a) utilizes the intrinsic dependency between the input time difference and latch resolving time for high gain. This architecture has a relatively narrow input range which may be acceptable for certain applications, but the gain is sensitive to various process parameters and thus this type of TA requires frequent calibration. The TA gain of the second existing TA based on discharging time control method [2] shown in Fig. 3(b) right quickly degrades for the larger time inputs and therefore a dynamic calibration is required to have a constant gain throughout the entire input range. Note that both metastability and discharging time control based TAs inherently work with nearly overlapping input edges due to

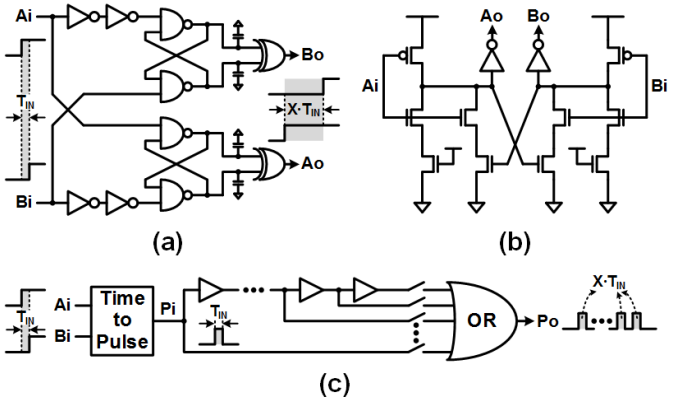


Fig.3. Existing time amplifier circuits based on (a) SR-latch meta-stability [1], (b) discharging time control [2] and (c) pulse-train [3]

their high gain and narrow range properties. Recently, a digital pulse train based TA [3] in Fig. 3(c) has been proposed to cope with the shortcomings of the prior techniques. However, this design is a pseudo time amplifier in the sense that it does not amplify the time, but integrates repetitive time pulses utilizing a specialized gated delay line based TDC to mimic time amplification. In addition, non-idealities in the requisite time-to-pulse conversion and gated delay line based TDC may even result in worse TDC performance.

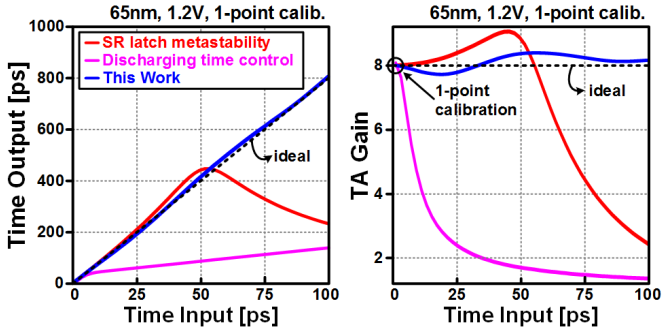


Fig.4. Simulated time amplifier output and gain for N=7 (i.e. 8x time amplifier) with 1-point calibration.

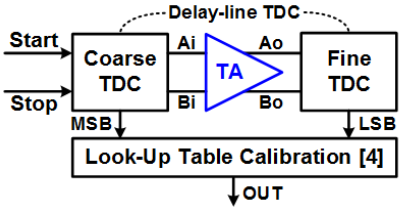
Fig. 4 shows the simulated 8x (i.e. N=7) TA transfer characteristics and the gain variation with respect to the input range. For a fair comparison, the three TAs ([1], [2] and the proposed TA) are designed and simulated in the same 65nm CMOS process using minimum device sizes. In addition, they are calibrated at one-point (i.e. 1ps, the minimum time input) to ensure all TAs have the initial 8x gain at the minimum input range. Compared to the existing TAs [1-2] with fluctuating or exponentially decaying gains, the proposed TA shows the most stable gain which is close to an ideal gain as indicated by the dotted lines. The simulated switched ROSC-based TA gain with a 100ps input range varies from -4% to 5% while the gains of the existing techniques vary from either -71% to 15% (for metastability based TA) or -83% to 3% (for discharging time control based TA).

	TA Principle	Analog/Digital (Gain Control)	Predictable TA Gain	Required Fine TDC
[1] VLSI'07*	Metastability	Analog	NO	Delay-line
[2] ISSCC'10*	Discharging Time Ctrl	Analog	YES (with calib.)	Delay-line
[3] VLSI'12*	Pulse Train	Digital	YES	Gated Delay-line
This Work	Switched ROSC	Digital	YES	Delay-line

*Original publications where the TA circuits were firstly introduced

Fig.5. Comparison with existing time amplifier circuits.

Fig. 5 compares the key features of the proposed TA with previous works. The proposed TA achieves a predictable and precise gain for wide input range with its all-digital circuit and gain controllability. While a prior digital TA [3] requires a special gated delay-line fine TDC circuit which asks for more attention on its impact on the TDC linearity, the proposed TA works with a simpler delay-line fine TDC circuit which utilizes replica unit delay cells from its coarse TDC.



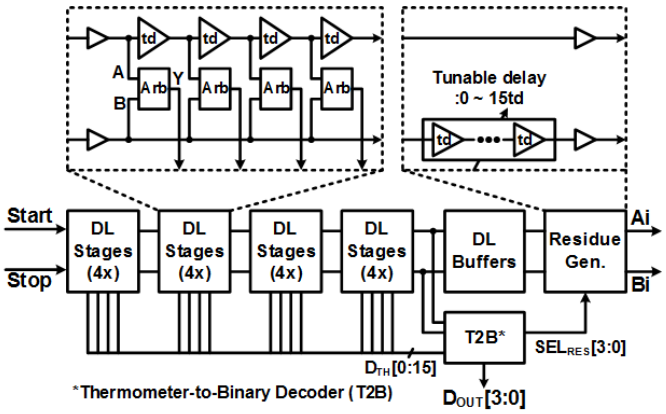
	6b	7b	8b
Coarse	4b		
TA	4x	8x	16x
Fine	2b	3b	4b

Fig.6. Two-step TDC circuit block diagram.

IV. Two-Step TDC Implementation

The block diagram of the two-step TDC implemented in a 65nm LP process is shown in Fig. 6. Delay-line TDC circuits are used for both coarse and fine TDCs and the proposed switched ROSC based TA is used as a TA circuit in between the two TDC circuits. A look-up table (LUT) based calibration technique [4] previously used for VCO-based ADCs is applied to reduce the TDC nonlinearity (i.e. INL). The TDC resolution can be reconfigured to 6-8 bits by changing the TA gain (4x, 8x and 16x). The corresponding resolution for the second-step fine TDC is 2-to-4 bits. The delay-line TDC circuit can be reconfigured by taping out outputs from different delay-line (DL) stages (i.e. 2/3/4bit for 1/2/4 output stages).

Fig. 7(a) illustrates the implemented coarse delay line TDC circuit. The delay line consists of four cascaded 4x delay line stages (i.e. total 16 delay buffers) for generating 4 bits. Each 4x delay line stages consist of a pair of input buffers, 4 delay buffers and arbiters. After generating 16bit thermometer code outputs (D_{TH}[0:15]) from the delay line stages, a thermometer-to-binary (T2B) decoder is used for converting them to 4bit binary code TDC outputs (D_{OUT}[3:0]). The 4bit binary code (SEL_{RES}[3:0]) also controls a tunable delay for generating the time residue. The arbiter circuit [5] used for the phase comparison at each delay stage is shown in Fig. 7(b).



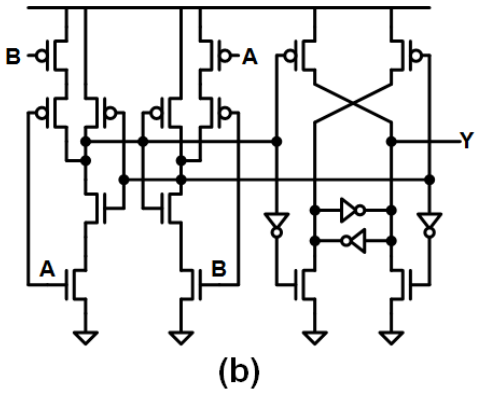


Fig.7. (a) 4bit coarse delay line TDC circuit. A reconfigurable 2/3/4b Fine TDC has the same circuitry while having 1/2/4 DL stages. (b) Arbiter circuit [5].

V. Test-Chip Measurement Results

Fig. 8 shows the measured TDC outputs for different TA gains for a ramp time input. The measured DNL is plotted in Fig. 9. The maximum DNL is 1.25/1.55/1.84LSB for 4x/8x/16x TA gains, respectively. The measured INL is shown

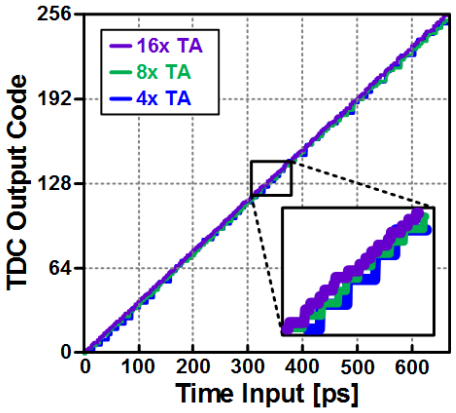


Fig.8. Measured TDC output with respect to a ramp time input.

in Fig. 10. The maximum INL after LUT calibration is 1.29/1.34/2.36LSB for 4x/8x/16x TA gains, respectively. The test-chip micrograph is shown in Fig. 11. TDC performance comparisons with prior TDC works are summarized in Fig. 12. The TDC consumes 2.0mW at 1.2V supply while occupying 0.07mm^2.

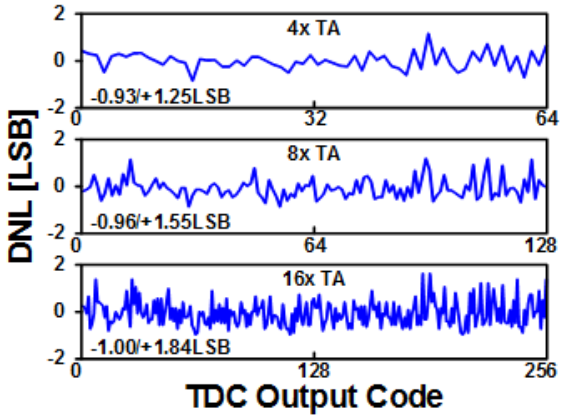


Fig.9. Measured DNL results.

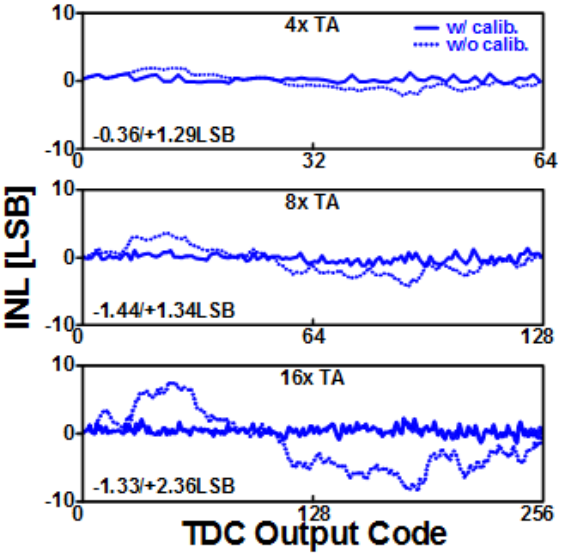


Fig.10. Measured INL results.

VI. Conclusion

To overcome the shortcomings of previous analog and digital TA circuits [1-3], a calibration-free switched ring-oscillator based TA with a digitally reconfigurable gain is proposed and demonstrated in a 65nm CMOS process. The proposed TA circuit provides a programmable (e.g. 4x, 8x and 16x) output delay that is highly linear using switchable ring-oscillator circuits. To verify the proposed idea, a 6-to-8bit two-step TDC circuit utilizing the proposed TA has been implemented using a conventional delay-line based TDC circuit. The performance of the proposed TA was tested under different gain configurations. The TDC circuit consists of a 4bit coarse delay-line TDC, the proposed TA, and a 4bit fine delay-line TDC. Using a 16x TA gain, the 8bit two-step TDC achieves a 2.6ps time resolution with a measured DNL and INL of 1.84LSB and 2.36LSB, respectively. The TDC consumes 2mW and occupies an area of 0.07mm^2.

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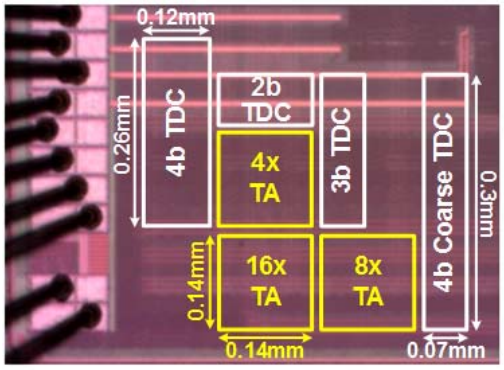

Fig.11. Chip micrograph.

	[6] CICC'09	[2] VLSI'11	[3] VLSI'12	This Work
Process	65nm	130nm	65nm	65nm
Scheme	Vernier	Pipeline	Two-Step	Two-Step
Resolution	4.80ps	0.63ps	3.75ps	2.60ps
Bits	7	11	7	8
Conv. Rate	50MS/s	65MS/s	200MS/s	80MS/s
Max. DNL	1LSB	0.5LSB	0.9LSB	1.84LSB
Max. INL	3.3LSB	9LSB	2.3LSB	2.36LSB
Power	1.7mW	10.5mW	3.6mW	2mW
Area	0.07mm^2	0.32mm^2	0.02mm^2	0.07mm^2

Fig.12. TDC Performance comparison.