Circuit Techniques for Mitigating Short-Term Vth Instability Issues in Successive Approximation Register (SAR) ADCs

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***Abstract* — Stress equalization and stress removal techniques for mitigating short-term Vth instability issues in SAR ADCs have been experimentally verified using an 80kS/s 10-bit differential SAR ADC fabricated in a 65nm LP CMOS process. The proposed techniques are particularly effective in enhancing the performance of high resolution and low sample rate SAR ADCs which are known to be more susceptible to short-term Vth degradation and recovery effects induced by Bias Temperature Instability (BTI). Experimental data shows that the proposed techniques can reduce the worst case DNL by 0.90 LSB and 0.77 LSB, respectively, compared to a typical SAR ADC.**

***Index Terms* — Short-term Vth instability, bias temperature instability, successive approximation register analog-to-digital converter, analog circuit reliability, aging, mitigation technique.**

I. Introduction

Parametric shifts and circuit failures induced by Bias Temperature Instability (BTI) has become more severe with technology scaling. The BTI mechanism manifests as short-term threshold voltage (Vth) instability [1] as shown in Fig. 1, and can be explained using either the trapping-relaxation model or the Reaction-Diffusion (R-D) model. When the device is in inversion mode with a high Vgs and a low Vds bias, the Vth degrades [2]. When the device is turned off, it immediately enters the "recovery" phase causing the Vth to retrieve back to its initial fresh value. Any permanent degradation in the Vth can cause a reduction in the circuit lifetime. Under long stress times (e.g., 10 years), the permanent and unrecoverable Vth degradation has been reported to be as high as 100mV [3]. Previous studies on BTI have mostly focused on the impact of both short-term and permanent Vth shifts on digital logic and memory circuit performance [4, 5]. Despite the growing interest on analog circuit reliability, almost no studies have taken place that analyze the impact of Vth instability on ADCs. Recently, it has been predicted that short-term Vth instabilities on the order of 1mV induced by a short stress pulse (e.g., 1μs) may cause erratic failure in the comparator of SAR ADCs [6, 7]. This suggests that ADC performance can degrade within microseconds of stress even for a fresh chip (not experimentally verified until this work). In this work, we quantify this effect for the first time through test chip studies and propose two simple circuit approaches that can be used to mitigate short-term Vth instability issues in SAR ADCs.

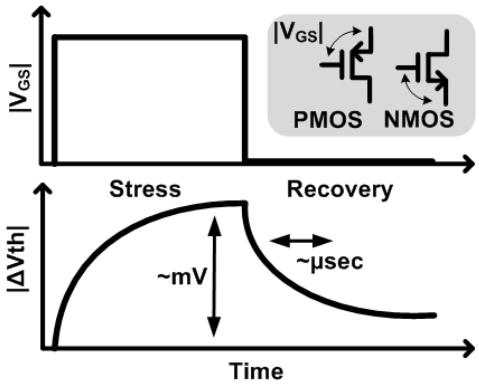


Fig. 1. Illustration of short-term Vth degradation and recovery in a CMOS transistor due to Bias Temperature Instability (BTI).

II. Impact of Short-Term Vth Instability on SAR ADC Operation

In most analog circuits (e.g., amplifiers, bias generators), the gate-to-source and drain-to-source voltages are typically lower than the supply voltage, so the absolute value of Vth degradation and recovery induced by BTI is inherently small compared to that of digital logic. However, in a comparator used in differential SAR ADCs, the two input transistors of a comparator may be subject to an asymmetric voltage stress during the initial SAR conversion steps as shown in Fig. 2, giving rise to a relatively large difference in their short-term Vth shifts. This may lead to an incorrect decision by the comparator especially during the second or third SAR conversion steps, which cannot be corrected by the subsequent conversion steps.

The example in Fig. 2 shows an incorrect conversion in the second SAR conversion step D8 when the input voltage difference (C) is smaller than Vth shift difference (B) caused by the large input voltage difference (A) applied during the preceding D9 step. In theory, an incorrect decision can occur during any SAR conversion step, from D8 to D0. However, the likelihood of an error is higher for the earlier steps since the input transistors are subject to a larger voltage difference in these steps.

To give a quantitative example, let us consider a 100kS/s 10-bit differential SAR ADC with a 1.2V supply voltage. Each conversion step takes 1/100k/10bits = 1μs to complete. Since one LSB corresponds to $1.2V/2^{10}$ =

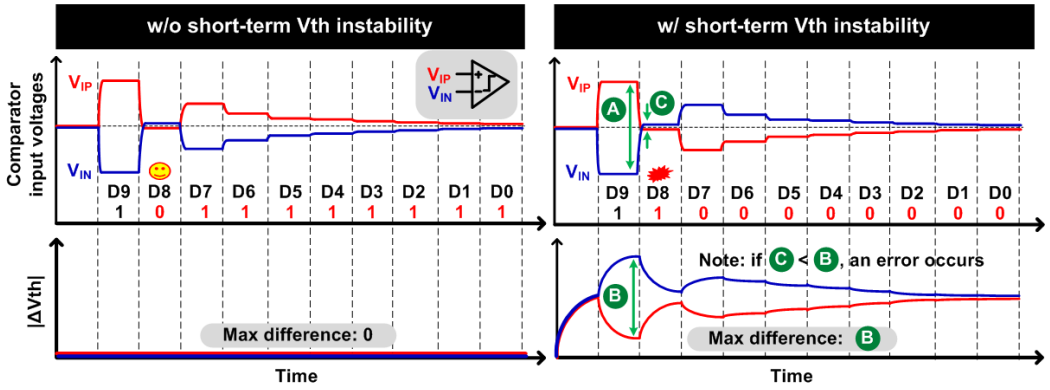


Fig. 2. Comparison of 10-bit SAR ADC operation without and with BTI induced short-term Vth instability. Comparator input voltages (top) and corresponding Vth shifts (bottom) for P-type input transistors are shown for each SAR conversion step. Comparators with N-type input transistors are equally susceptive to short-term Vth instability issues due to PBTI in high-k metal gate technologies.

1.17mV, any short-term Vth shift difference greater than this voltage can cause an incorrect comparator decision. Using the previously reported short-term Vth shift of 3.5mV under a 1µs, 1.1V stress pulse [6], we can predict that a conversion error will occur for this ADC. The aforementioned effect is expected to be worse in SAR ADCs with lower sample rates and higher bit resolutions due to the longer asymmetric stress time and higher sensitivity to any input offsets.

III. Proposed Stress Equalization and Stress Removal Techniques

We propose two techniques for mitigating the aforementioned effect. Fig. 3 illustrates the basic idea compared to a typical SAR ADC operation. By equalizing the input voltages to the common mode voltage VDD/2 (namely stress equalization), or by connecting them to VDD (namely stress removal), the comparator input offset Y due to the asymmetric voltage stress can be recovered prior to the next conversion step. Note that we chose VDD/2 as the equalization voltage since the common mode voltage for a rail-to-rail input signal is VDD/2.

The proposed stress equalization and stress removal techniques are demonstrated on a 10-bit differential charge-redistribution SAR ADC consisting of the new comparator, binary-weighted capacitor arrays, and successive approximation registers as shown in Fig. 4. To suppress the substrate and supply noise, and to ensure good common-mode rejection, a fully differential architecture is employed in the proposed SAR ADC. The comparator with the proposed techniques shown in Fig. 5, consists of a preamp, a latch, and a logic circuit with a feedback loop. The logic circuit controls the comparator input nodes by connecting them to either the recovery or equalization voltages VDD or VDD/2, right after the comparator makes a decision, and returning to the original input voltages V_{IN} and V_{IP} just prior to the next SAR conversion step. This specific sequence ensures that the comparator input offset due to asymmetric voltage stress is minimized without interfering with the original SAR operation.

A preamp stage is used in the SAR comparator to suppress the input-referred noise of the subsequent latch

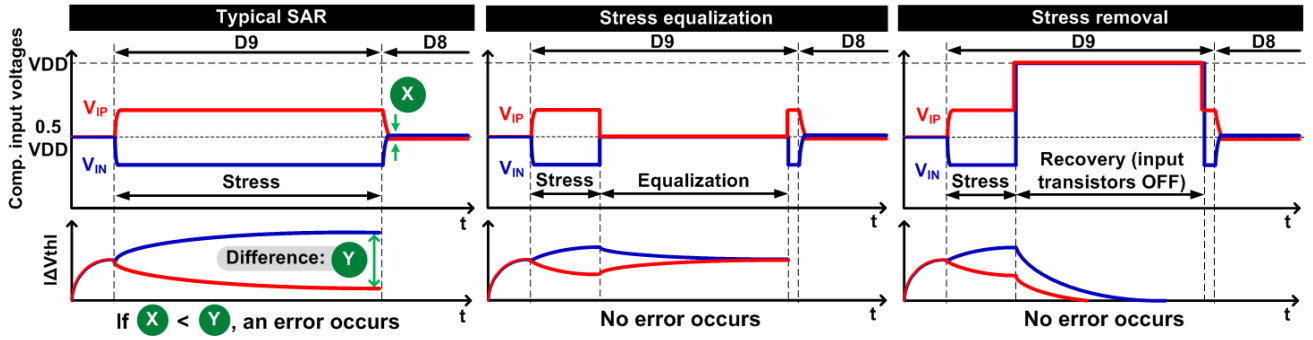


Fig. 3. Illustration of proposed stress equalization and stress removal techniques compare to a typical SAR ADC. Comparator input voltages (top) and corresponding Vth shift (bottom) are shown for just the first D9 conversion step here for simplicity. By either equalizing the input voltages or connecting them to VDD right after the conversion, the comparator input offset due to asymmetric voltage stress can be minimized in the next conversion step.

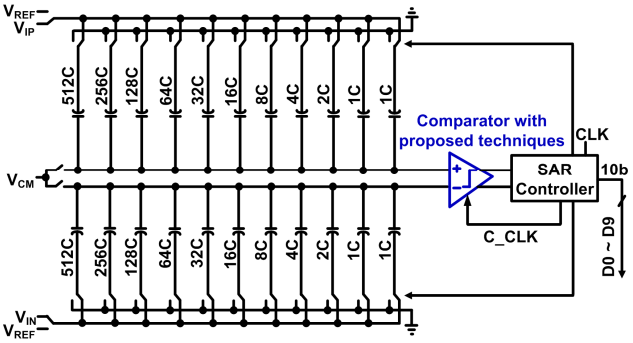


Fig. 4. Block diagram of a 10-bit differential charge-redistribution SAR ADC. The proposed stress mitigation techniques are implemented in the comparator circuit block.

stage. Although both NMOS and PMOS type input transistors can be considered in the preamp, we chose the latter option as PMOS NBTI is more dominant than NMOS PBTI in the 65nm process used for this study. An added benefit of using PMOS input transistor is the reduced 1/f noise [8]. Note that NMOS input transistors will be equally affected by PBTI in high-k metal gate technologies and hence the short-term Vth shift effect will occur regardless of the input transistor type in more advance nodes [9].

Fig. 5 (bottom) shows the simplified timing diagram of the proposed technique. When the comparator clock COMP_CLK is low, the two outputs of the latch VON and VOP are pre-discharged. The comparator evaluates on the rising edge of COMP_CLK and subsequently one of the two outputs will go high. A NOR gate detects this low-to-high transition and asserts a decision-complete-indication signal DONEb. A NAND gate with inputs C_CLK and DONEb generates a gate-control-signal GATE_CTRL to control the comparator input nodes. To ensure that the proposed techniques do not interfere with the original SAR operation, an additional delay t_D is inserted between the C_CLK and the COMP_CLK.

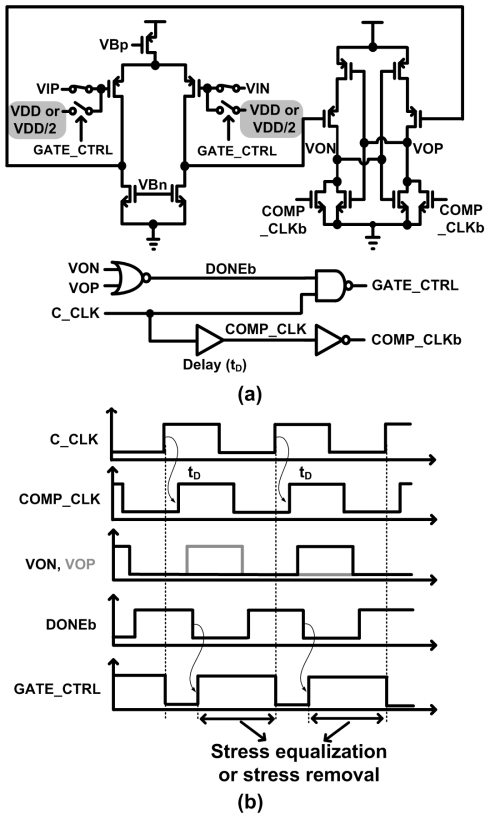


Fig. 5. (a) Schematic and (b) timing diagrams of comparator circuit consisting of a pre-amp stage and a latch circuit [8]. Additional switches are used for the proposed stress equalization and stress removal techniques.

IV. SAR ADC Test Chip Measurement Results

A 10-bit differential SAR ADC employing the two proposed techniques was implemented in a 65nm test chip. The sampling frequency of 80kS/s was used for the experiments. Fig. 6 shows the measured DNL and INL for the proposed and conventional SAR ADC design. The DNL is improved by 0.90 LSB and 0.77 LSB for the stress

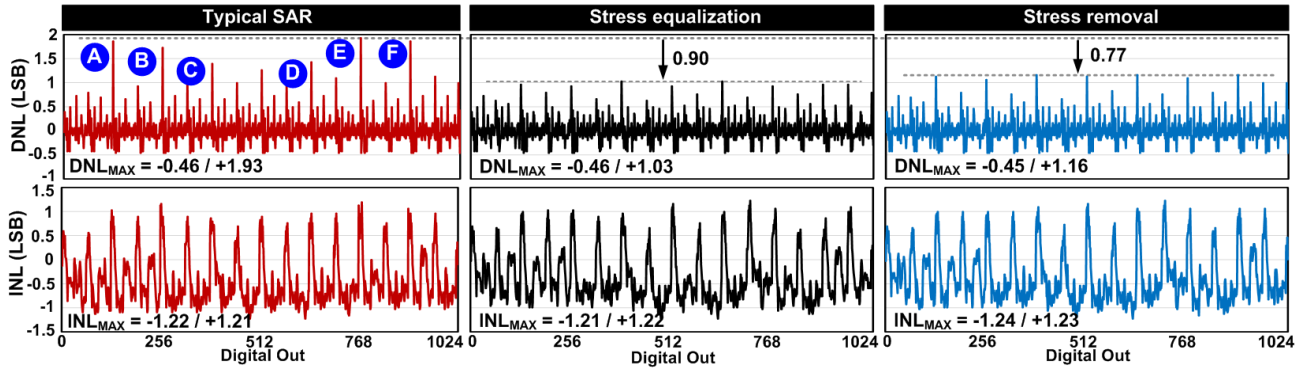


Fig. 6. Measured DNL (top) and INL (bottom) using the proposed techniques compared to a typical SAR ADC. Measured data from a 65nm test chip shows a DNL improvement of 0.90 and 0.77 LSB using stress equalization and stress removal, respectively. The impact on INL was negligible.

	Digital out						Conv. step generating error
	Decimal value	Binary D9	D8	D7	D6	D5	...
A	127 =	0	0	0	1	1	...
	128 =	0	0	1	0	0	...	D7
B	255 =	0	0	1	1	1	...
	256 =	0	1	0	0	0	...	D8
C	383 =	0	1	0	1	1	...
	384 =	0	1	1	0	0	...	D7
D	639 =	1	0	0	1	1	...
	640 =	1	0	1	0	0	...	D7
E	767 =	1	0	1	1	1	...
	768 =	1	1	0	0	0	...	D8
F	895 =	1	1	0	1	1	...
	896 =	1	1	1	0	0	...	D7

Fig. 7. Digital outputs that are most vulnerable to Vth instability. Results clearly indicate errors in the second or third conversion steps. A~F locations are shown in the upper left plot of Fig. 6.

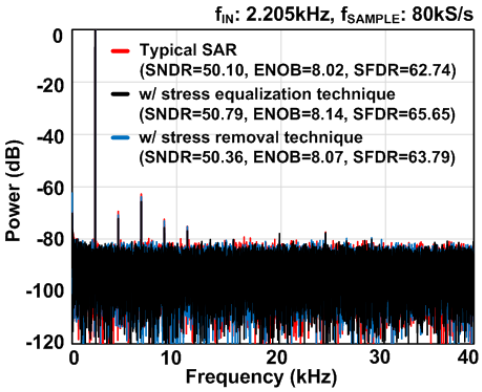
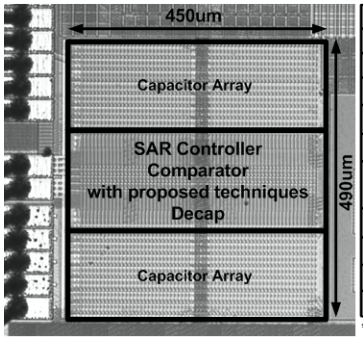


Fig. 8. FFT for a 2.205kHz differential sinusoidal input sampled at 80kS/s. Improvements in SNDR, ENOB, and SFDR using the proposed techniques can be seen.

equalization and stress removal techniques, respectively, while INL data showed no apparent advantage. The DNL plots also reveal that the actual improvement in DNL depends on the digital output code and that there are particular digital outputs, namely points A~F in Fig. 6, which show a large improvement in DNL. A careful inspection of these digital outputs, also summarized in Fig. 7, reveals that these are the output codes wherein an error occurs in the initial conversion steps. That is, a conversion error occurred in the D8 or D7 conversion steps which agrees with our hypothesis in Fig. 2. The relatively large asymmetric voltage stress applied during the first couple of steps (i.e. D9 or D8) are primarily responsible for the errors caused by device instability issues. A 65536-point FFT of a sinusoidal input with a frequency of 2.205kHz sampled at 80kS/s is shown in Fig. 8. Subtle improvements in SNDR, ENOB, and SFDR can be observed. The die photo and performance summary of the implemented SAR ADC are shown in Fig. 9. The active circuit area is 450x490μm^2 and the ADC employing the proposed stress mitigation techniques achieves a worst case DNL of -0.46/+1.03 LSB, worst case INL of -1.21/+1.22 LSB, SNDR of 50.79dB (or ENOB of 8.14), and an SFDR of 65.65dB.



Process	65nm CMOS
Supply	1.2V
Resolution	10bit
Sample rate	80kS/s
DNL_{MAX} (LSB)	-0.46 / +1.03*
INL_{MAX} (LSB)	-1.21 / +1.22*
SNDR (dB)	50.79* @ 2.205kHz input
SFDR (dB)	65.65*
ENOB	8.14bit*
Power	305μW
Area	450x490μm^2

*w/ stress equalization technique

Fig. 9. Die photo and performance summary table of the 65nm SAR ADC test chip with the proposed techniques.

V. Conclusion

In this paper, we present two circuit techniques for mitigating short-term Vth instability issues in SAR ADCs. The proposed techniques temporarily connect the comparator input nodes to the same voltage level right after each conversion is complete. This either equalizes or eliminates the short-term Vth instability of the input transistors, thereby preventing incorrect decision from being made by the comparator circuit. Measured data from a 65nm 10-bit SAR ADC test chip shows that the proposed techniques reduce the worst case DNL by 0.90 LSB using stress equalization, and by 0.77 LSB using stress removal, compared to a conventional SAR ADC.

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