A VCO-Based ADC Employing a Multi-Phase Noise-Shaping Beat Frequency Quantizer for Direct Sampling of Sub-1mV Input Signals

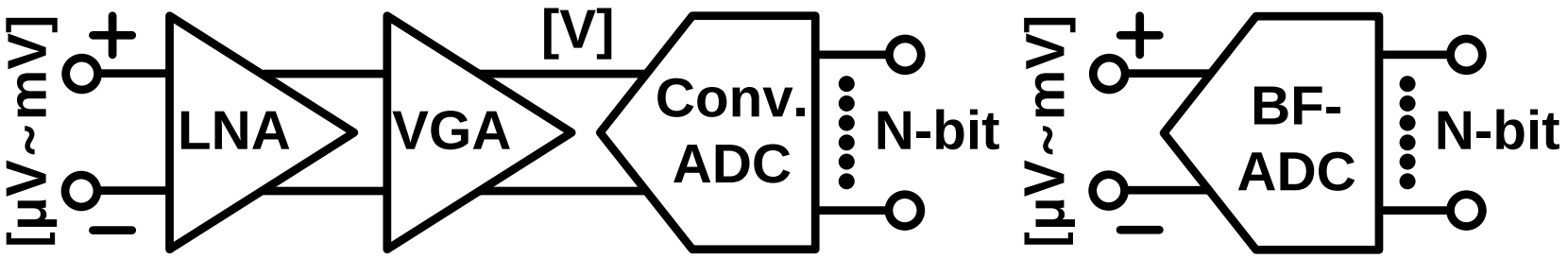
Bongjin Kim, Somnath Kundu, Seokkyun Ko and Chris H. Kim

University of Minnesota, Minneapolis
kimx2447@umn.edu

Agenda

- **Motivation**
- **Conventional vs. proposed VCO-based ADC**
- **Multi-phase & Noise-shaping BF Quantizer**
- **Test chip configuration**
- **Measurement results**
- **Conclusion**

Direct Sub-mV Signal Acquisition



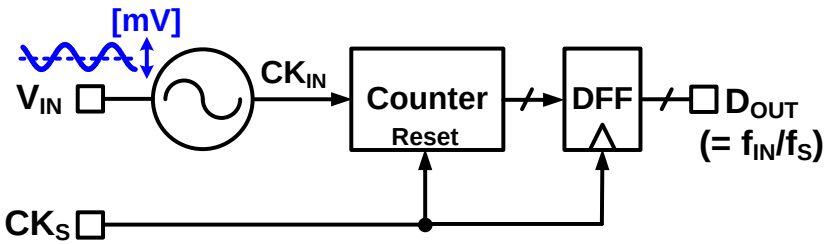
Conventional **This Work**

- **Conventional**
  - **Signal pre-conditioning amplifiers (LNA/VGA)**
  - **Conventional ADC for rail-to-rail input range**

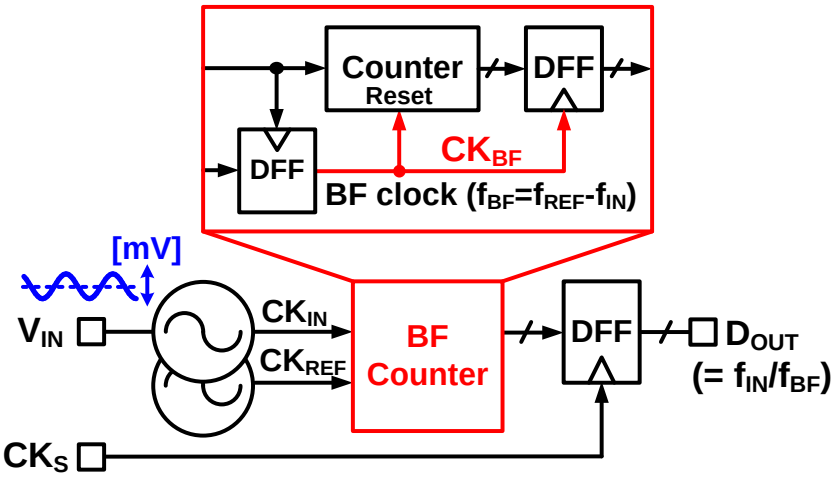
0

- **This work (Beat Frequency (BF) ADC)**
  - **Direct A-to-D conversion w/o signal amplification**

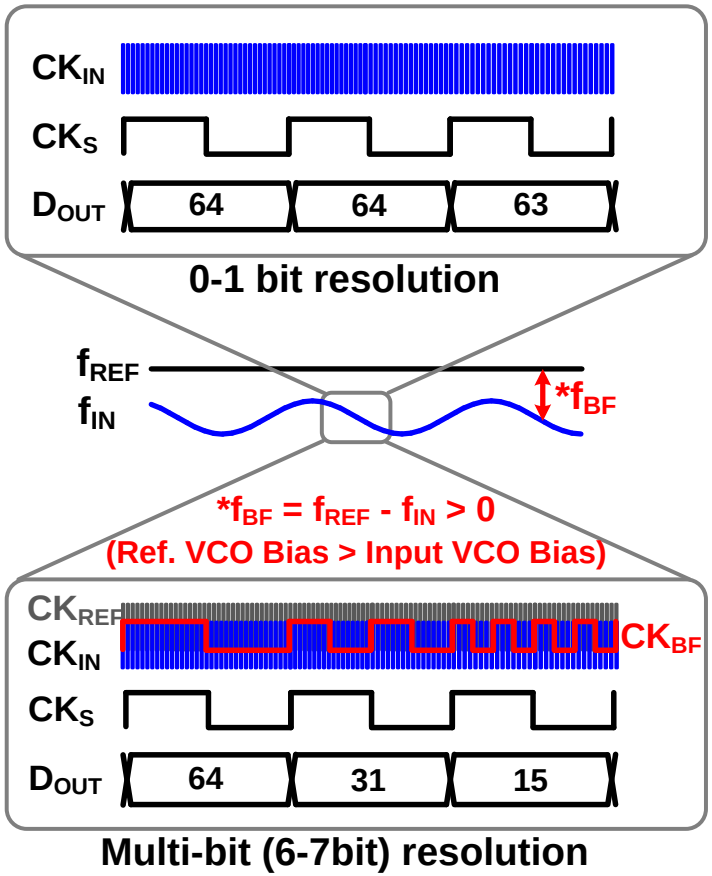
Conv. vs. Proposed VCO-Based ADC



Conventional (VCO + Counter)



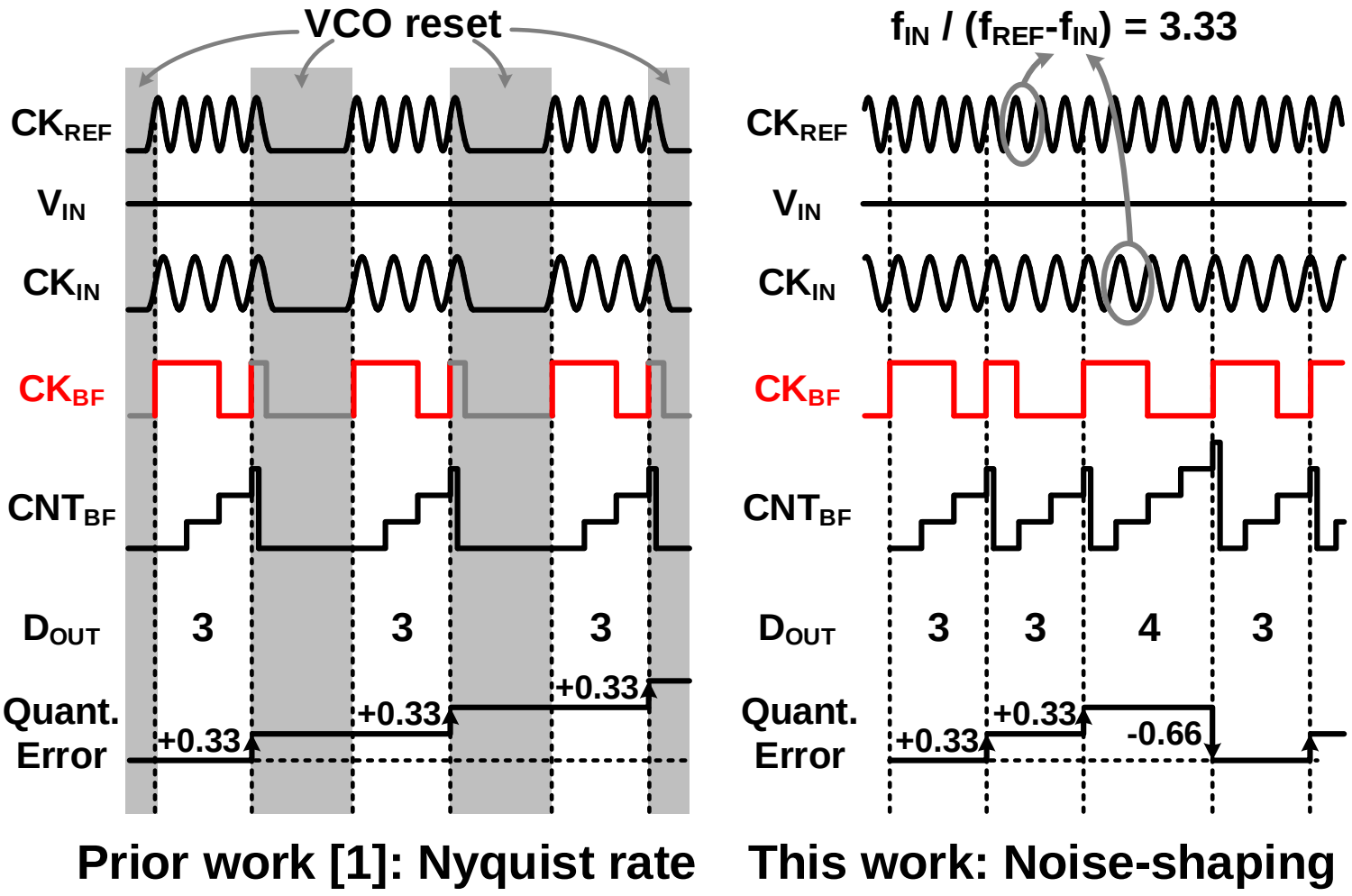
Proposed (VCO + BF-Counter)



- **Conventional : Linear freq. detection using VCO**
- **Proposed : High-resolution BF detection based [1]**

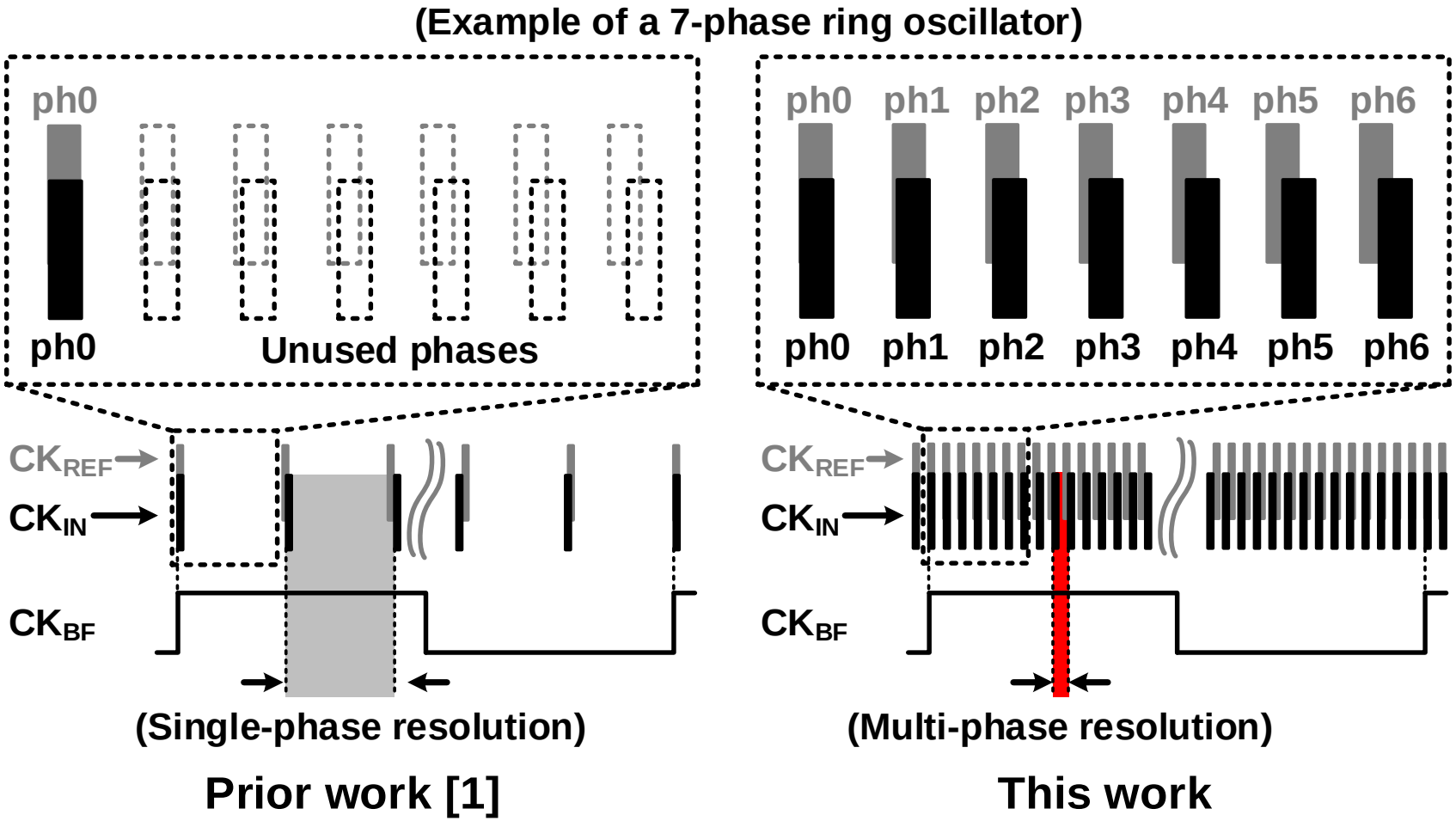
[1] B. Kim et al., IEEE Custom Integrated Circuits Conference 2013

Noise-Shaping Beat Freq. Quant.



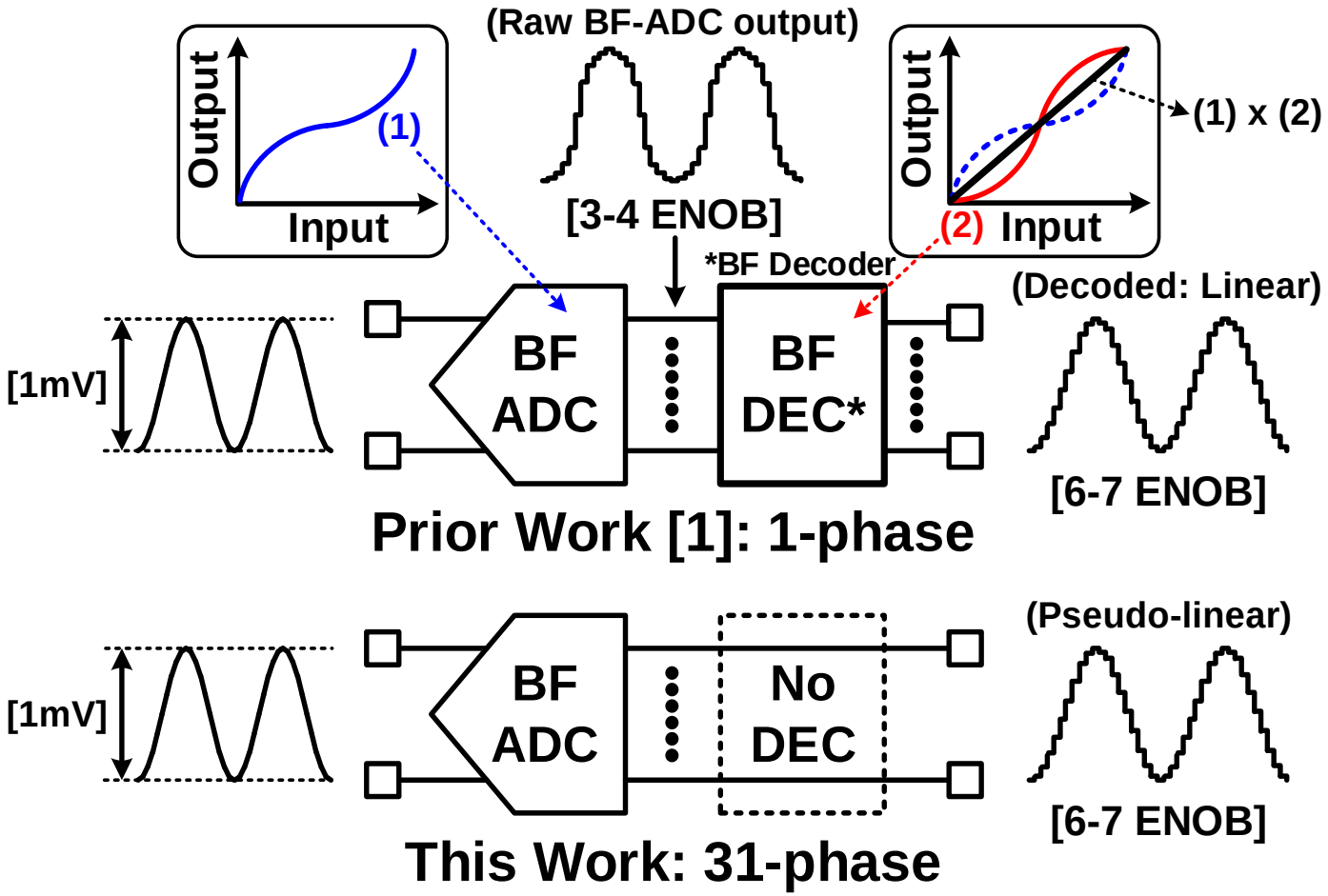
- **Noise-shaping improves BF detection resolution**

Multi-Phase Beat Freq. Quantization



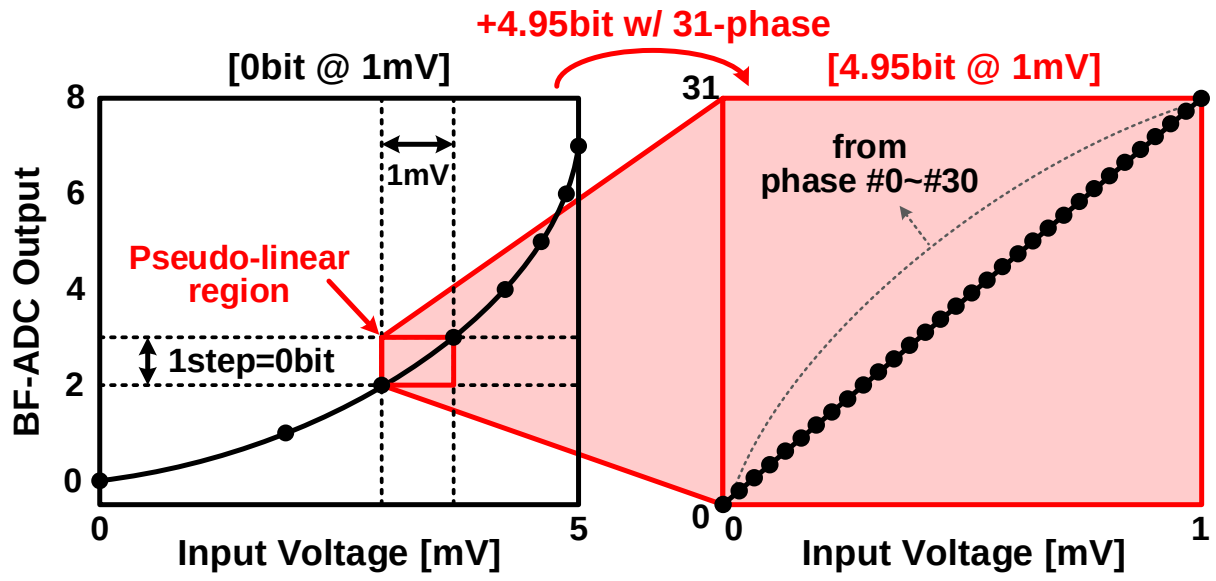
- **N-phase improves BF detection resolution N-times**

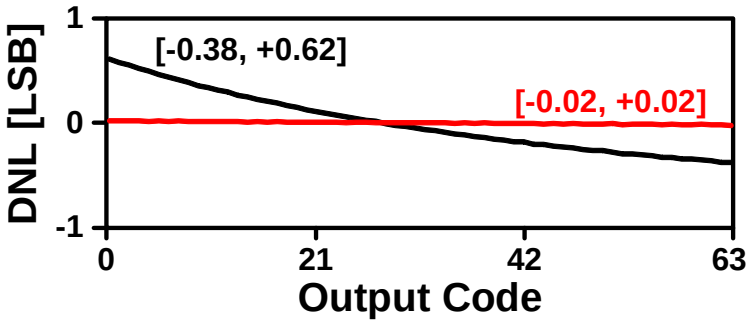
Linear BF-ADC with Multi-Phase

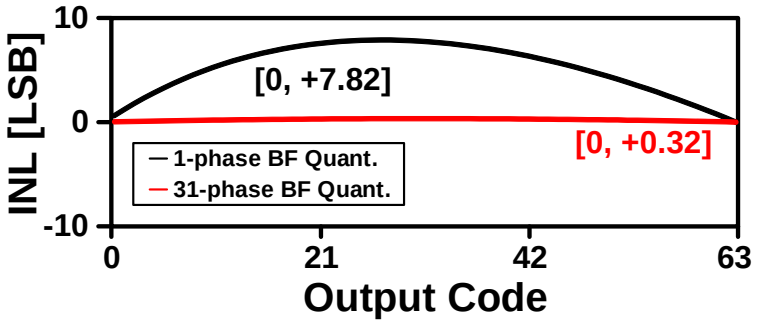


- **Does not require BF-decoding with the improved resolution from multi-phase**

Linearity of Multi-Phase BF-ADC







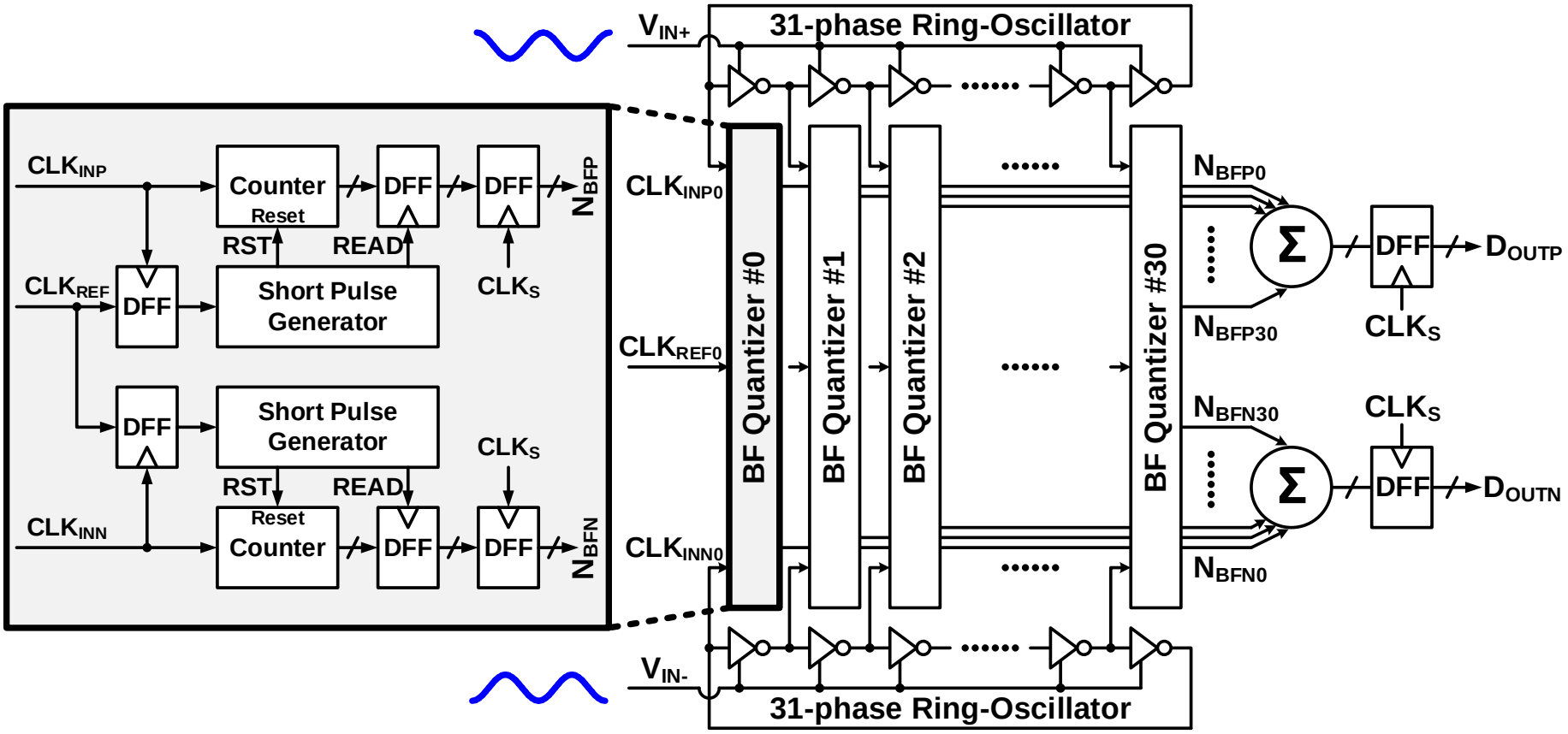
- **Simulated linearity: DNL_{MAX}/INL_{MAX}=0.02/0.32 [LSB]**

Comparison with Prior Arts

	Conventional VCO-based	Previous BF-ADC [1]	This work
Quantization Scheme	Linear Counting	Beat Freq. Counting	Beat Freq. Counting
Freq. Detection Sensitivity* (@ 100 counts)	Low (1%)	High (0.01%)	High (0.01%)
Noise-Shaping	Yes	No	Yes
Multi-Phase	Yes	No	Yes
BF Code Utilization	-	Wide (Nonlinear)	Narrow (Pseudo-linear)
BF Decoding	-	Required	Not Required

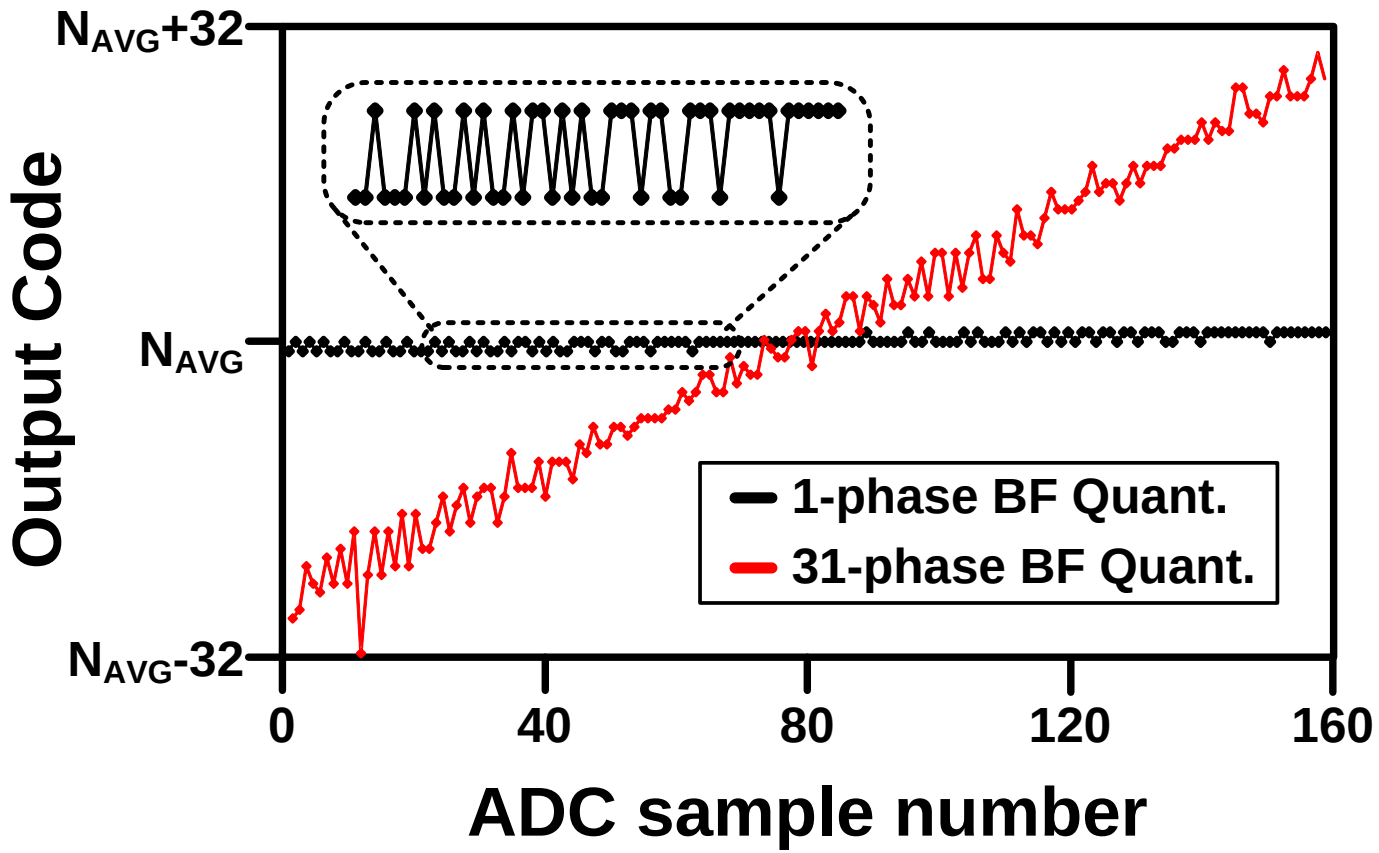
*Freq. step required for a count change of one

VCO-Based ADC w/ BF-Quantizer



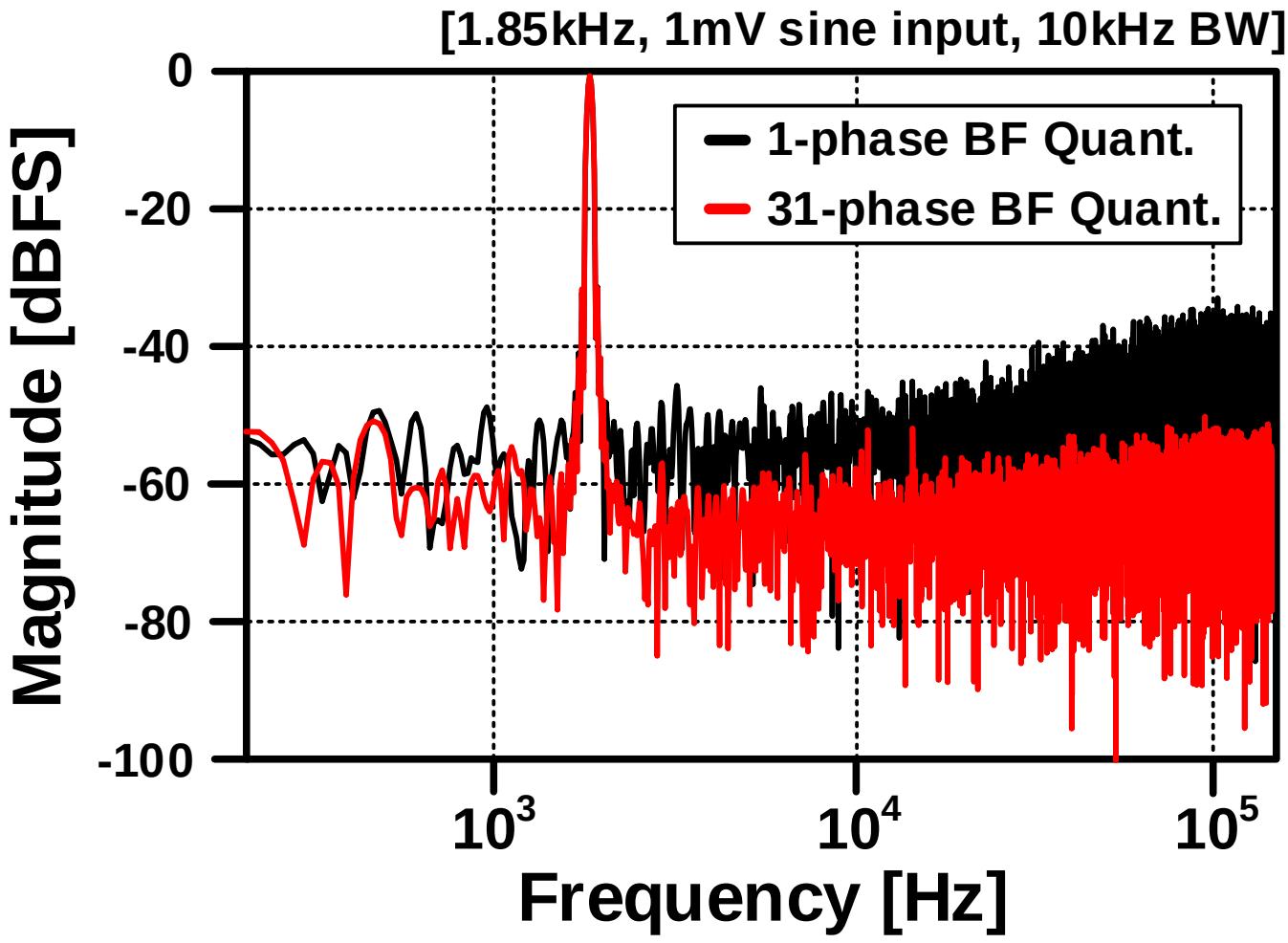
- **A pair of 31-phase ring oscillator for +/- inputs**
- **31x banks (each consists of +/- BF quantizers)**

Measured Code vs. Ramp Input



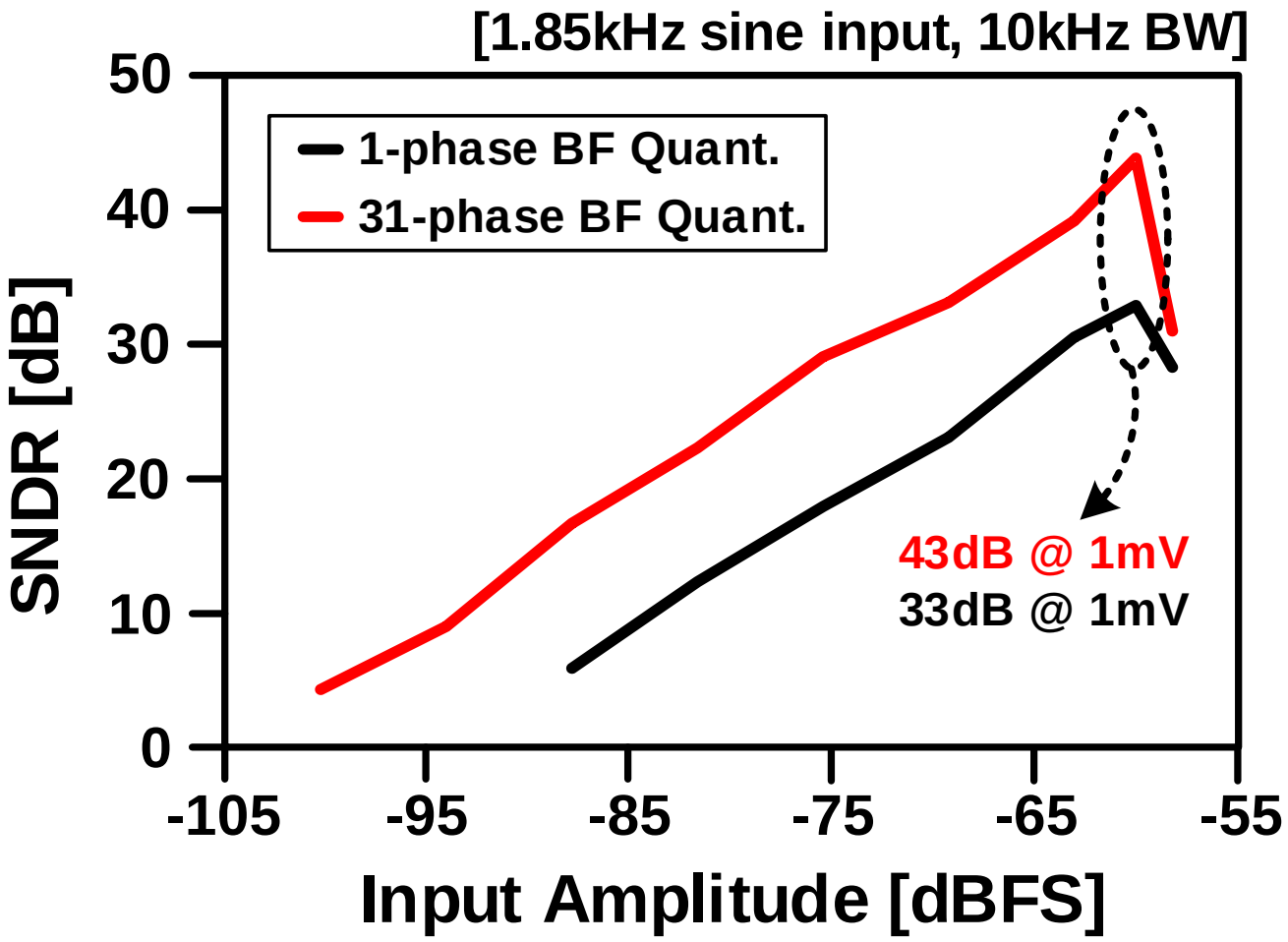
- Noise-shaping is clearly shown in the results
- 31-phase result shows 31x wider output range

Measured FFT Result w/ 1mV Input



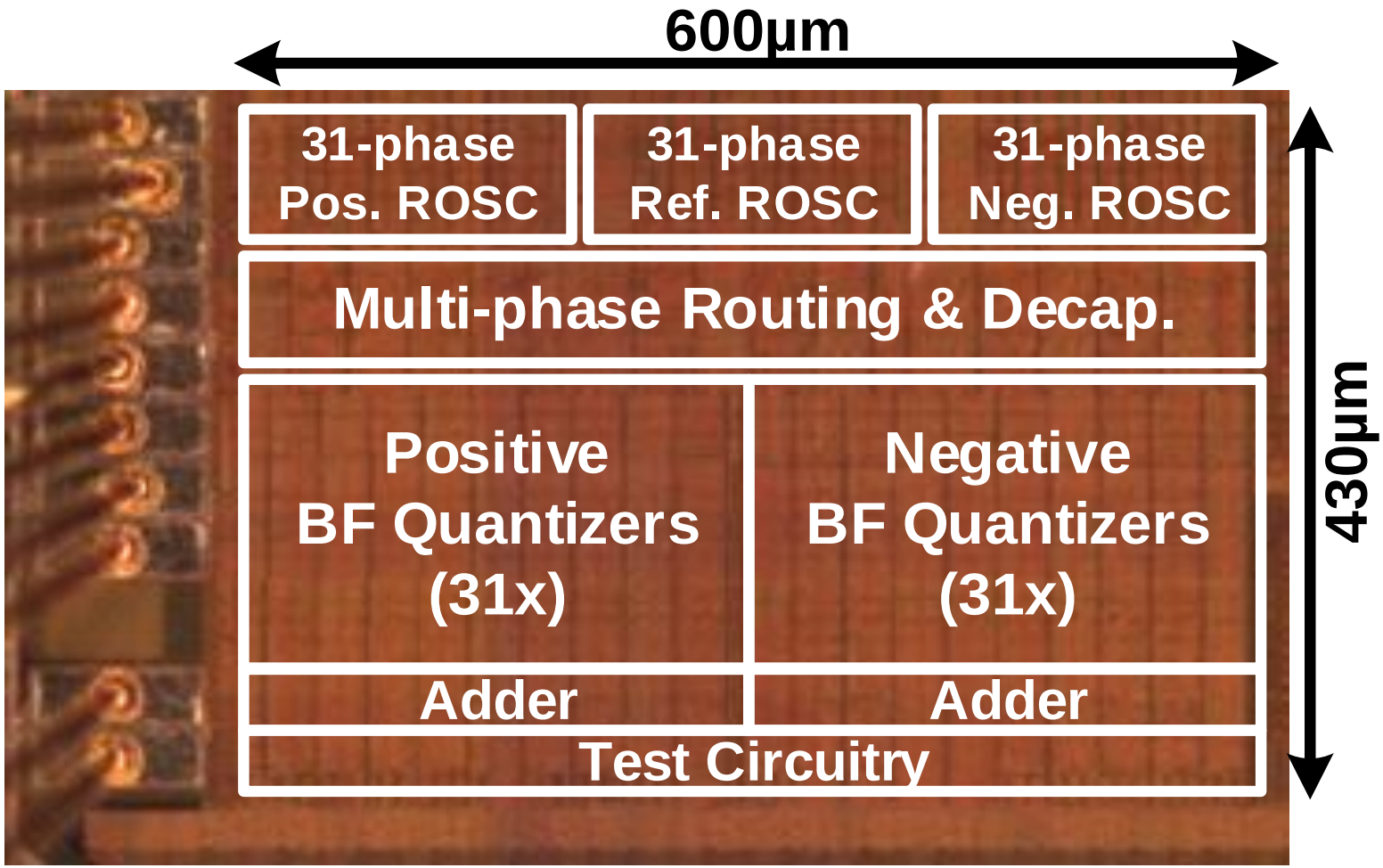
- SNDR = 43dB (i.e. ENOB=6.85) / SFDR = 56.7dB

Measured SNDR vs. Input Amplitude



- SNDR @ 1mV = 43dB @ 31-phase, 33dB @ 1-phase

Chip Micrograph



Performance Comparison

	VLSI'07	VLSI'11	[1] CICC'13	This work
Process	0.13µm	90nm	65nm	65nm
Supply	1.2V	N/A	1.2V	1.2V
Sample Rate	950MHz	640MHz	4.17kHz	300kHz
Input BW	20MHz	8MHz	2kHz	10kHz
$SNDR_{1mV}$*	12dB	3dB	35dB	43dB
$ENOB_{1mV}$*	1.70	0.21	5.52	6.85
SFDR[dB]	N/A	71.4	41.9	56.7
IN_{0dB}[dBFS]**	-70	-63	-89	-105
Power	38mW	4.3mW	0.92µW	36µW
Area[mm^2]	0.185	0.10	0.013	0.258

* Peak SNDR/ENOB for a 1mV input amplitude.

** Input amplitude at SNDR = 0dB (dBFS @ full-scale = 1V)

Conclusion

- **A VCO-based ADC featuring beat-freq. quantizer is designed using 65nm CMOS for a direct A-to-D conversion of sub-mV input signal**
- **Multi-phase and 1st order noise-shaping property improves ADC resolution without the use of beat frequency decoding**
- **43dB SNDR (6.85 ENOB) has been achieved for a 1mVppd input signal**