Impact of Interconnect Length on BTI and HCI Induced Frequency Degradation

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***Abstract*— The dependence of Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) induced frequency degradation on interconnect length has been examined for the first time. Experimental data from 65nm test chips show that frequency degradation due to BTI decreases monotonically with longer wires because of the shorter effective stress time, while the HCI-induced component has a non-monotonic relationship with interconnect length due to the combined effect of increased effective stress time and decreased effective stress voltage. A simple aging model is proposed to capture the distinct BTI and HCI effects in global interconnect drivers.**

Keywords – Aging; bias temperature instability; hot carrier injection; degradation; interconnect

I. INTRODUCTION

Interconnects fabrics used in clock networks, signal buses, network-on-chips, memory wordlines/bitlines, and high-speed I/Os are critical components in modern ICs. CMOS devices in interconnect drivers experience time-varying voltage stress that results in performance degradation due to bias temperature instability (BTI) and hot carrier injection (HCI).

BTI, frequently cited as the primary reliability concern in modern CMOS processes, occurs when a device is biased in strong inversion. Once a device is turned off, the degradation induced by previous stress phase starts to recover immediately [1]. HCI remains to be an important reliability concern even though it has become less prominent with the constant scaling of supply voltage. This is attributed to the 4-5x larger time exponent compared to BTI which makes HCI the dominant aging contributor towards the end of a product lifetime. In the context of interconnect drivers (for example, consider clock drivers) where the activity factor tends to be extremely high compared to random logic gates, the hot carriers pass through the channel more often and gets exacerbated by the lateral field making HCI a serious concern.

BTI and HCI mechanisms have different sensitivities to the operation conditions, which vary with specific circuit paths. Sheet resistance and parasitic capacitance of long wires have not been scaling favorably in advanced processes which could lead to interconnect dominated paths having drastically different aging behavior compared to logic dominated paths. Although there have been previous works showing the impact of fanout load on transistor aging [2-5], practically no attention has been paid to the aging behavior in interconnects with long wire loads. A correct understanding on the impact of interconnect length on circuit degradation will enable a more complete picture of system level aging.

For the first time, this work presents measurement results highlighting the dependence of BTI and HCI induced aging on wire length. The previous "all-in-one" silicon odometer framework [5] was adopted to separate the BTI and HCI contributions with picosecond order resolution and microsecond order measurement interrupts. Measurement data from a 65nm test chip shows that BTI-induced degradation decreases monotonically with longer interconnect length while HCI exhibits a non-monotonic behavior with interconnect length. Simple models for BTI and HCI induced degradation in interconnect drivers show good agreement with measured data.

II. INTERCONNECT ODOMETER DESIGN

The top level block diagram of the interconnect odometer test chip is shown in Fig. 1. Four ROSC configurations with different interconnect lengths ranging from 0µm to 1000µm were implemented. Among the four ROSCs: one suffers from BTI stress exclusively, one is under both BTI and HCI stress and the other two remain unstressed which are set as the frequency reference point. Each stressed oscillator is paired up with its unstressed counterpart, and fed into a beat-frequency detection system through multiplexers. Transistor dimensions of each ROSC stage are $(W/L)_{PMOS}$=6µm/0.06µm and

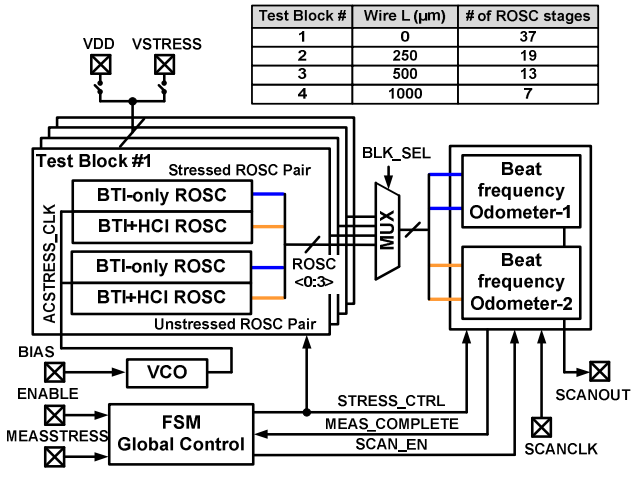


Figure 1. Interconnect odometer test chip diagram. Four ROSCs (stressed pair and unstressed pair) are used for each wire configuration to separately monitor BTI and HCI induced frequency shifts.

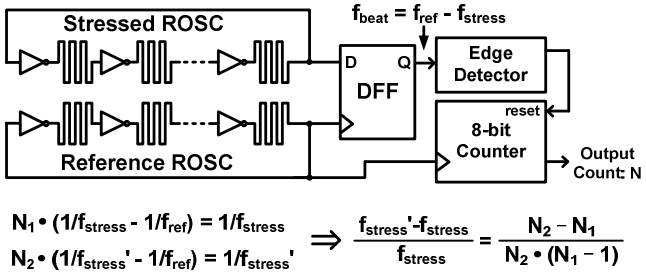


Figure 2. Beat frequency odometer system used in this work. N_1 and N_2 are the counts from the counter output, recorded before and after a certain stress period. Using the equations listed above, we can conveniently calculate the percentage frequency change with picosecond level precision.

$(W/L)_{NMOS}$= 3µm/0.06µm. On-chip power gates provide fast local stress voltage switching while a voltage controlled oscillator generates an AC stress frequency.

A. Beat-frequency detection technique

The beat frequency odometer system in Fig. 2 measures the percentage change in the stress ROSC frequency. We include a brief explanation of the beat frequency odometer system for convenience but further details can be found in [6-7]. The output of the reference ROSC is used as clock of the D flip-flop (DFF) to sample the stressed ROSC output. The initial frequency of the reference ROSC (f_{ref}) is set using trimming capacitors to be slightly higher than that of the stressed ROSC (f_{stress}). The DFF output toggles from low to high whenever the rising edge of the two ROSC outputs overlap. In other words, the output of the DFF exhibits the beat frequency f_{beat} defined as $f_{ref} - f_{stress}$. A counter is implemented at the output of the DFF to record the number of reference ROSC periods corresponding to the beat period. The count is registered after each stress period, and the frequency shirt in the stress ROSC can be conveniently calculated using straightforward algebraic equations shown in Fig. 2.

The highlight of the beat frequency odometer system is that it provides extremely high-resolution frequency shift measurements (>0.016%) with microsecond order measurement interruption which eliminates the unwanted BTI recovery effects. A detail comparison of various ROSC based frequency degradation measurement techniques can be found in our previous all-in-one odometer paper [5].

B. Separately monitoring BTI and HCI

The BTI and HCI contributions were separately measured by adopting the "all-in-one" odometer concept illustrated in Fig. 3 [5]. In stress mode, the top ROSC is gated off from the supply with the bottom ROSC driving the inputs and outputs of both ROSCs. Using this configuration, the transistors in the top ROSC experience the same BTI stress condition as those in the bottom ROSC but with negligible HCI degradation. Note that electromigration (EM) effect in the wires was negligible in the 65nm process used for the test chip and therefore was not the focus of this work. In measurement mode, the frequency degradations of the two stressed ROSCs are measured using two silicon odometer beat frequency detection systems. The HCI-induced aging can be then obtained by subtracting out the BTI component (top ROSC in Fig. 3) from the combined BTI+HCI effect (bottom ROSC in Fig. 3). The die photo and key features of the 65nm interconnect odometer test chip are given in Fig. 4.

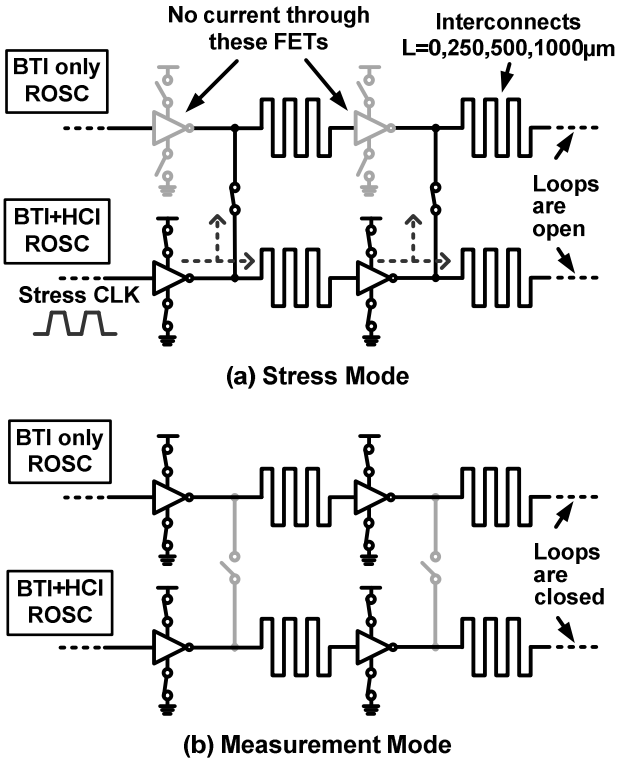
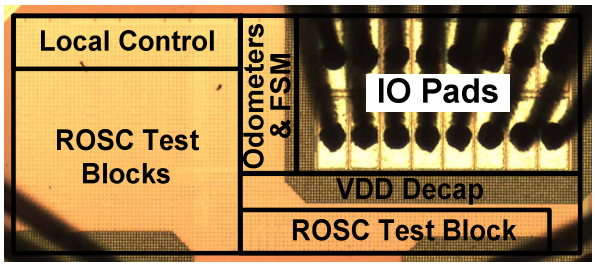


Figure 3. ROSC pair configuration in stress and measurement modes. The top ROSC exhibits the same amount of BTI as the bottom ROSC but without any HCI [5].



Process	65nm LP CMOS
Core / IO Supplies	1.2V / 2.5V
Stress Voltage	1.8V, 2.4V
Active Area	0.182mm^2
Interconnect Layer	M2, W=100nm, double shielded w/ 100nm spacing
Δf Resolution	> 0.016%
Meas. Interrupt	< 3µs

Figure 4. Die photo and feature summary of the 65nm interconnect odometer test chip.

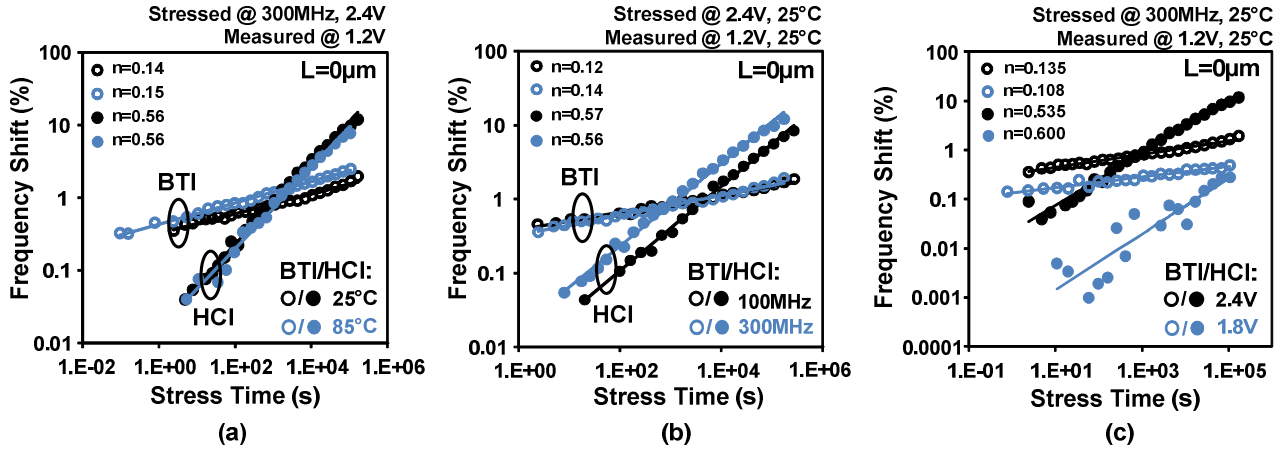


Figure 5. Measured BTI and HCI contribution under different (a) temperatures, (b) frequencies, and (c) stress voltages. The HCI component is obtained by subtracting out the BTI-only degradation from the BTI+HCI degradation.

III. Test Chip Results

A. Basic ROSC aging measurements

We first present experimental data from the test chip showing the general behavior of HCI and BTI degradation for ROSCs without any long interconnect between the inverter stages. As expected, BTI is the primary contributor of aging at early stress time as shown in Fig. 5 while HCI with its larger power law exponent surpasses BTI at longer stress time. Fig. 5 (a) indicates that BTI is positively correlated with temperature, while HCI is slightly reduced at higher temperatures due to the reduced drain current as a result of increased phonon scattering. BTI is weakly dependent on the frequency as verified in Fig. 5 (b), while the ROSCs suffer more HCI degradation at higher frequencies due to the increased switching activity. Fig. 5 (c) shows that both aging mechanisms are exacerbated at higher stress voltages with HCI displaying stronger voltage dependence. Fig. 6 shows BTI and HCI degradation versus stress time for different interconnect configurations. Under an identical stress condition, the ROSC without any interconnect suffers the most BTI degradation, while the HCI is worst for the ROSC with 500µm wire length.

B. Interconnect length vs. BTI aging

The BTI induced frequency shifts after 19 hours of stress at 2.4V are shown in Fig. 7 for different interconnect lengths. The

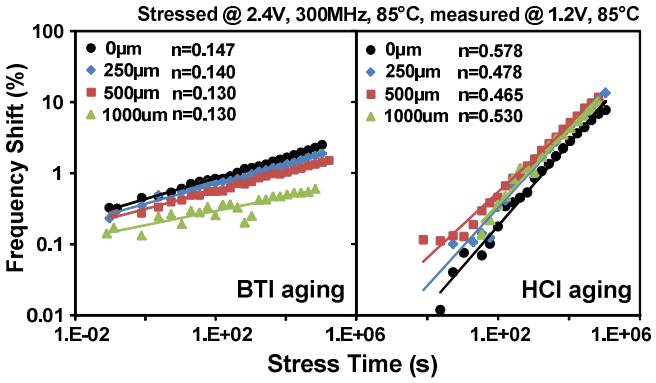


Figure 6. Measured frequency degradation induced by BTI and HCI for different interconnect lengths. BTI is the worst at L=0µm (left) while HCI is worst at L=500µm (right).

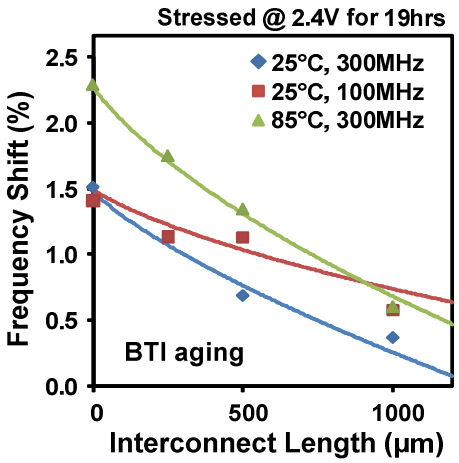
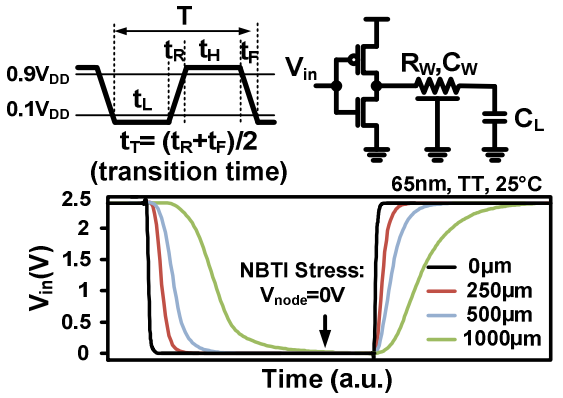


Figure 7. Measured data (in markers) and aging model proposed in section IV-B (curves) for BTI induced frequency degradation.

amount of BTI aging decreases monotonically with longer interconnects for all three stress conditions. This can be explained by the longer transition time observed in longer wires which translates into a shorter amount of time the PMOS transistor is actually exposed to a full BTI stress bias. The distributed RC induced by interconnects reduces the slew rate for each signal transition as shown in Fig. 8. HSPICE simulation results in the table of Fig. 8 confirm a 20X longer transition time ($t_T=t_R+t_F$) as the wire length is increased from 0µm to 1000µm. The duty cycle for the PMOS device in the interconnect driver is reduced with a longer interconnect due to the longer transition time, which is verified by simulation in Fig. 9. Note that PBTI in NMOS is negligible in this 65nm process as it does not employ high-k metal-gate devices. However, the general trend will not change in the presence of PBTI as the duty cycle for the NMOS is also reduced for longer interconnects. Fig. 7 also reveals a softer dependency on interconnect length for a lower AC stress frequency of 100MHz. This can be attributed to the smaller fraction of time spent for signal transition for lower input frequencies, which makes the duty cycle less sensitive to interconnect length as shown with the simulations of the different stress cycle time in Fig. 9.



Int. L (µm)	t_T (ps)	t_L/T (effective duty cycle)	
		100MHz	300MHz
0	50.4	49.7%	49.3%
250	197	49.0%	47.0%
500	406	47.9%	43.9%
1000	1018	44.9%	34.7%

Figure 8. Effective stress time (t_L) decreases in longer interconnects resulting in a smaller BTI degradation as shown in Fig. 7.

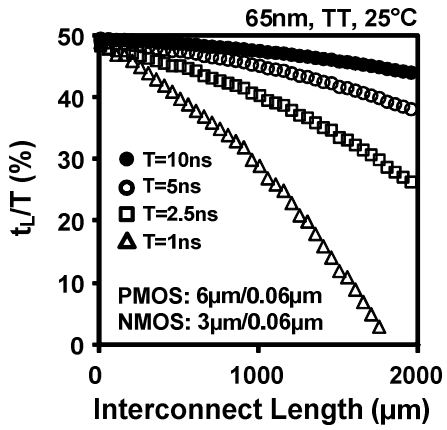


Figure 9. Normalized duty cycle for which the PMOS is deeply biased on decreases with a longer interconnect due to the decreased slew rate.

C. *Interconnect length vs. HCI aging*

The effect of HCI in Fig. 10 shows a non-monotonic relationship with wire length. This is counter-intuitive but can be explained using the following two factors:

(i) A driver with a longer wire has a smaller peak current due to the voltage division between the wire resistance and the driver's equivalent resistance as shown in Fig. 11. Simulation results in Fig. 12 confirm that the maximum discharging current through the NMOS decreases with longer interconnect due to the aforementioned voltage division action. Note that the peak current drops for wires shorter than 200µm due to the fast input slew rate that causes the NMOS to turn off before it enters the saturation mode. For the simulation, we use a driver size of $(W/L)_{PMOS}$=6µm/0.06µm and $(W/L)_{NMOS}$= 3µm/0.06µm and a distributed RC wire model to obtain accurate results. The reduction of the peak current has a similar effect as having a lower effective stress voltage and therefore leads to a smaller frequency shift.

(ii) A longer wire makes the current pulse wider due to the larger wire resistance and capacitance which have the effect of increased stress time compared to a shorter wire. The increase

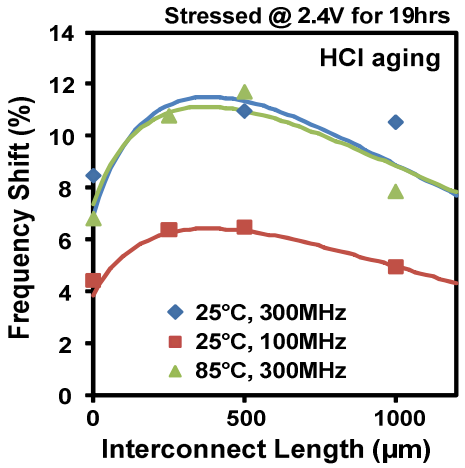
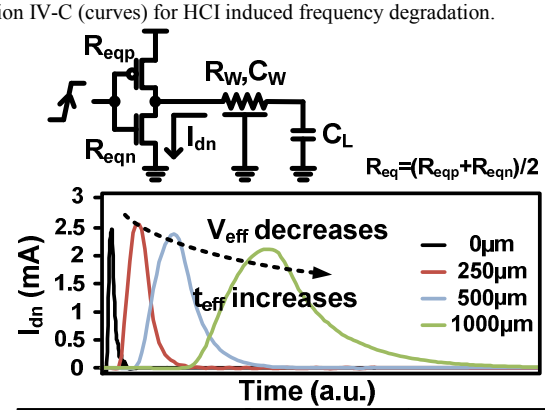


Figure 10. Measured data (in markers) and aging model proposed in section IV-C (curves) for HCI induced frequency degradation.



Wire Len. (µm)	I_{peak}(mA)	t_{eff}* (ps, eff. stress time)	V_{eff} (V, eff. V_{stress})
0	2.50	6.3	2.40
250	2.56	25	2.34
500	2.39	51	2.29
1000	2.12	127	2.19

*t_{eff} is a parameter proportional to rise (or fall) time [8].

Figure 11. Effective stress time increases in longer interconnects while the effective stress voltage decreases resulting in the non-monotonic HCI trend in Fig. 9.

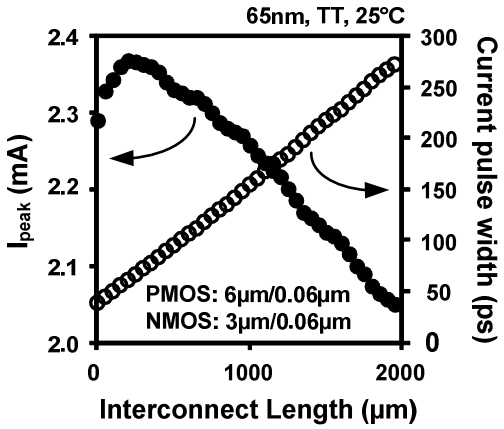


Figure 12. HCI parameters versus interconnect length. NMOS peak current decreases with interconnect length, while the pulse width increases. The combined effect is a non-monotonic dependence of HCI induced frequency degradation on interconnect length.

in the current pulse width shown in Fig. 12 has the effect of an increased HCI stress time which leads to increased HCI degradation for longer interconnects [8].

The combined effects of (i) and (ii) can be used to explain the non-monotonic relationship between HCI induced frequency shift and interconnect length.

IV. Aging Models for Interconnect Drivers

As we saw in the previous sections, the amount of BTI and HCI depends on the transition time and bias condition which vary based on the interconnect load. However, none of the existing models incorporate these interconnect related parameters. In this section, we propose analytical BTI and HCI models applicable to global interconnect drivers which agree well with experimental results. The general approach for modeling the frequency degradation in global interconnects follows the two-step approach described below.

- Step 1: The frequency degradation of an interconnect dominated path is less sensitive to the device aging compared to a logic dominated path due to the invariant interconnect RC delay components. We capture this difference by introducing the sensitivity factor.
- Step 2: The amount of BTI and HCI aging depends on the stress time and stress voltage that vary with respect to interconnect length. Existing BTI and HCI models with modified stress parameters are used to derive the final model.

Section A describes step 1 where we will first analyze the sensitivity factor and derive its mathematical expression. In sections B and C, we perform step 2 to derive analytical models for BTI and HCI, respectively.

A. Sensitivity factor

For a driver stage with long interconnects, the wire RC dominates the delay, so the degradation of the overall delay is less sensitive to the transistor V_t shift compared to a logic dominated path. This can be seen from the HSPICE results in Fig. 13 where a device Vt shift of 30% translates into a 12% frequency degradation for a ROSC with a 1000µm interconnect per stage, whereas the degradation for a ROSC with no interconnects is 15%. This effect can be easily captured in our

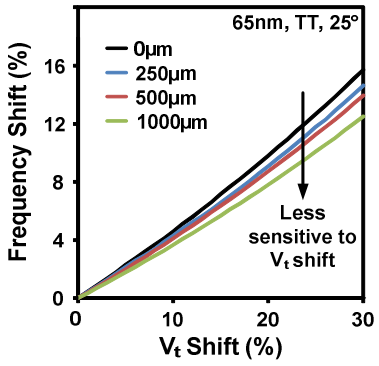


Figure 13. Frequency shift vs. V_t shift for different interconnect length. The frequency shift of a interconnect dominated signal path is less sensitive to the logic device aging due to the invariant wire RC delay. This is captured using the sensitivity factor parameter shown in section IV-A.

models by introducing a sensitivity factor α defined as the ratio between the % frequency degradation of an interconnect dominated path and that of a logic dominated path for the same amount of device aging:

$$\left(\frac{\Delta f}{f}\right)_{interconnect} = \alpha \left(\frac{\Delta f}{f}\right)_{logic} \quad (1)$$

For a given interconnect resistance (R_W), interconnect capacitance (C_W), load capacitance (C_L), equivalent driver resistance before stress (R_{eq}) and after stress (R_{eq}'), the % frequency degradation can be expressed as:

$$\left(\frac{\Delta f}{f}\right)_{interconnect} = \frac{\Delta R_{eq}(C_W+C_L)}{R'_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)} \quad (2)$$

Note that R_W and C_W of a wire can be simply calculated from the sheet resistance and metal capacitance parameters. Since the % frequency degradation for a logic only path can be written as:

$$\left(\frac{\Delta f}{f}\right)_{logic} = \frac{\Delta R_{eq} C_L}{R'_{eq} C_L} = \frac{\Delta R_{eq}}{R'_{eq}} \quad (3)$$

Here, $\Delta R_{eq}=R_{eq}'-R_{eq}$ which is the change in equivalent driver resistance before and after stress. Using equations (2) and (3), the expression of α can be derived as:

$$\alpha = \left(\frac{\Delta f}{f}\right)_{interconnect} / \left(\frac{\Delta f}{f}\right)_{logic}$$
$$= \frac{\Delta R_{eq}(C_W+C_L)}{R'_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)} \frac{R'_{eq}}{\Delta R_{eq}}$$
$$= \frac{R'_{eq}(C_W+C_L)}{R'_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)} \quad (4)$$

The above sensitivity factor will be applied to the BTI and HCI models proposed in sections B and C.

B. BTI aging model for interconnect drivers

BTI aging is determined by the time a device is biased in a full strong inversion mode. Hence, it can be expressed using the cycle time parameter t_L/T where t_L and T are defined in Fig. 8. Employing the methodology in [9], the deviation of BTI from the ideal 50% duty cycle case can be expressed using $(50\% - t_L/T)^k$, where k is determined empirically. The overall BTI induced frequency shift can be expressed as:

$$\left(\frac{\Delta f}{f}\right)_{BTI} = \left(\frac{\Delta f}{f}\right)_{@50\%} - B\left(50\% - \frac{t_L}{T}\right)^k$$
$$= Aexp(\gamma V_{str})t^n - B\left(\frac{2t_T}{T}\right)^k \quad (5)$$

Here, γ is the voltage acceleration factor, V_{str} is the stress voltage, t is the BTI stress time of a logic only path, n is the BTI time exponent, t_T is the transition time, and T is the AC stress cycle. B and k are empirical parameters found to be 0.01 and 0.7 @25°C, and 0.003 and 0.75 @85°C in the 65nm technology used for this work. Parameter A follows an Arrhenius behavior with temperature, i.e. $\exp(E_a/kT)$, where E_a is the temperature activation energy. Both E_a and γ values are experimentally determined constants, which can be found based on the type of CMOS device.

The transition time t_T is interconnect RC dependent, which can be simply denoted as:

$$t_T = R_{eq}(C_W + C_L) + R_W\left(\frac{C_W}{2} + C_L\right) \quad (6)$$

Using the sensitivity factor from section A, the overall BTI frequency degradation for long interconnects can be derived as:

$$\left(\frac{\Delta f}{f}\right)_{BTI\_interconnect} = \alpha\left(\frac{\Delta f}{f}\right)_{BTI} = \frac{R'_{eq}(C_W+C_L)}{R'_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)}$$

$$\times\left[Aexp(\gamma V_{str})t^n - B\left(\frac{2R_{eq}(C_W+C_L)+2R_W\left(\frac{C_W}{2}+C_L\right)}{T}\right)^k\right] \quad (7)$$

C. HCI aging model for interconnect drivers

From the general HCI models [10], the degradation of frequency can be approximated as:

$$\left(\frac{\Delta f}{f}\right)_{HCI} = Cexp\left(-\frac{D}{Veff}\right)t_{eff}^m \quad (8)$$

where C, D, and m are empirical process parameters, t_{eff} is the effective HCI stress time which is directly related to the transition time, and V_{eff} is the effective drain to source voltage during stress. The experimental and simulation results in section III show that the effective voltage and effective stress time depend on the interconnect RC load.

The interconnect resistance R_W divides the stress voltage applied on transistor drain while charging and discharging. So the effective HCI stress voltage can be estimated as:

$$V_{eff} = \frac{R_{eq}}{R_{eq}+R_W}V_{str} \quad (9)$$

where R_{eq} is the equivalent driver resistance, R_W is the interconnect resistance, and V_{str} is the HCI stress voltage in a path without interconnect.

Under the assumption that the HCI stress time is proportional to the transition time, the effective stress time considering interconnect impact can be expressed as:

$$t_{eff} = \frac{R_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)}{R_{eq}C_L}t \quad (10)$$

Here, t is the time a device in a logic dominated path is under HCI stress. Finally, the HCI induced frequency degradation can be derived using the sensitivity factor introduced in section A:

$$\left(\frac{\Delta f}{f}\right)_{HCI\_interconnect} = \alpha\left(\frac{\Delta f}{f}\right)_{HCI} = \frac{R'_{eq}(C_W+C_L)}{R'_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)}$$

$$\times Cexp\left[-D/\left(\frac{R_{eq}}{R_{eq}+R_W}V_{str}\right)\right]$$

$$\times\left(\frac{R_{eq}(C_W+C_L)+R_W\left(\frac{C_W}{2}+C_L\right)}{R_{eq}C_L}t\right)^m \quad (11)$$

The results from the proposed models (7) and (11) are overlaid as curved lines on top of the measured data in Figs. 7 and 10 showing good agreement with actual hardware.

V. CONCLUSIONS

Interconnect dominated paths frequently used in state of the art ICs have different aging performance compared to their logic dominated counterparts. The degradation caused by major aging mechanisms such as BTI and HCI in interconnect drivers depend on the interconnect RC load. This dependence must be studied in order to develop accurate aging models compatible to devices driving different interconnect loads. In this work, we successfully designed an interconnect odometer test chip to accurately capture the frequency degradation of signal paths with different interconnect lengths. The all-in-one odometer circuit technique was implemented to separate BTI and HCI aging and to suppress unwanted BTI recovery. The measurement interrupt was kept below 3µs. Experimental results from a 65nm test chip show that the frequency degradation caused by BTI decreases with increasing interconnect length, while HCI induced degradation peaks at around 500µm. Simulation results are used to demonstrate the impact of interconnect on transition time and node voltage under AC stress which attribute to the degradation and interconnect dependency. Finally, simple models are proposed to estimate the BTI and HCI induced frequency shift components in a global interconnect driver.

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REFERENCES

[1] T. Grasser and B. Kaczer, "Evidence that two tightly coupled mechanisms are responsible for negative bias temperature instability in oxynitride MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1056-1062, May 2009.

[2] W. Weber, H. M. Brox, T. Kunemund, M Muhlhoff, and D. Schmitt-Landsiedel, "Dynamic degradation in MOSFET's. II. application in the circuit environment," *IEEE Trans. Electron Devices*, vol. 38, no. 8, pp. 1859-1867, Aug 1991.

[3] W. Jiang, J. C. H. Le and T. Kopley, "Assessing circuit-level hot-carrier reliability," in *IEEE Int. Reliability Physics Symp*., 1998, pp. 173-179.

[4] T. H. Kim, R. Persaud and C. H. Kim. "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," *IEEE Journal of Solid State Circuits*, vol. 43, pp. 874-880, April 2008.

[5] J. Keane, Xiaofei Wang, D. Persaud and C. H. Kim. "An all-in-one silicon odometer for separately monitoring HCI, BTI, and TDDB," *IEEE journal of Solid-State Circuits*, vol. 45, pp. 817-829, April 2010.

[6] J. Keane, W. Zhang, C.H. Kim, "An On-Chip Monitor for Statistically Significant Circuit Aging Characterization", in *International Electron Devices Meeting*, pp. 4.2.1 – 4.2.4, December 2010.

[7] J. Keane, W. Zhang, C.H. Kim, "An Array-Based Odometer System for Statistically Significant Circuit Aging Characterization," *IEEE Journal of Solid-State Circuits*, pp. 2374 – 2385, October 2011.

[8] K. N. Quader, E. R. Minami, W. J. Ko, P. K. Ko and C. Hu. "Hot-carrier-reliability design guidelines for CMOS logic circuits," *IEEE Journal of Solid State Circuits*, vol. 29, pp. 253-262, Mar 1994.

[9] R. Fernandez, B. Kaczer, A. Nackaerts, S. Demuynck, R. Rodriguez, M. Nafria and G. Groeseneken. "AC NBTI studied in the 1 hz -- 2 GHz range on dedicated on-chip CMOS circuits," in *IEEE International Electron Devices Meeting*, pp. 1-4, Dec. 2006.

[10] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan and K. W. Terrill. "Hot-electron induced MOSFET degradation – model, monitor and improvement," *IEEE Trans. Electron Devices*, vol. 32, no. 2, pp. 375-385, Feb 1985.