Performance Characterization and Majority Gate Design for MESO-based Circuits

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***Abstract*—Magnetoelectric spin-orbit (MESO) logic is a promising spin-based post-CMOS logic computation paradigm. This work explores the application of the basic MESO device concept to more complex logic structures. A simulation framework is first developed to facilitate the performance evaluation of MESO-based circuits. Based on the analysis, it is seen that inadvertent logic errors may potentially be introduced in cascaded MESO stages due to sneak paths, and solutions for overcoming this problem with a short pulse and two-phase evaluation are discussed. Next, the generalization of the MESO inverter structure to majority logic gates is shown. Two implementations, based on different physical mechanisms, are presented and a relative analysis of their speed and power characteristics is provided.**

***Index Terms*—Spintronics, magnetoelectric coupling, inverse spin-orbit coupling, simulation, majority gate.**

I. Introduction

As CMOS-based designs reach their limits, there is an increasing interest in developing novel device technologies. Spin-based computing shows promise as it embraces emerging physical mechanisms and new materials to enable better device performance and enriched design functionality. Through mechanisms that allow material and feature scaling, spintronics provides a pathway for designing future electronic systems [1].

Magnetoelectric spin-orbit (MESO) logic [2] is a recently proposed spintronic logic device concept that achieves high energy efficiency by combining the magnetoelectric (ME) coupling effect [3]–[5] with the inverse spin orbit coupling (ISOC) effect [6]–[8]. Low energy magnetic state switching is enabled by the ME coupling effect and realized with the presence of multiferroic materials or heterostructures [9], [10]. The ISOC effect provides efficient spin-to-charge conversion and facilitates the use of charge-based signal propagation between stages of logic. Unlike technologies such as all-spin logic [11], [12] that use spin current to propagate signals, the use of charge current avoids the large overhead of repeater insertion [13]. Together, the ME and ISOC effects realize energy-efficient transduction between charge and magnetic state variables, and either could implement majority logic.

In this work, we first develop a simulation framework to determine the energy and delay of a single MESO device as well as cascaded stages of MESO structures. We introduce our method for estimating the delay and energy of the MESO device based on our modified circuit model with conventional elements as well as the FE capacitor model based on Landau-Khalatnikov (LKh) equation. The simulation method and performance measurement are described in Section II. Next, we examine issues related to cascading MESO logic stages in Section III, with particular attention to the potential for sneak paths that may disrupt correct operation. In Section IV, we propose and evaluate two approaches for implementing MESO majority gates based on the two different physical mechanisms in the MESO device, and conclude with Section V.

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II. Modeling a MESO inverter

A. Structure of a basic MESO inverter

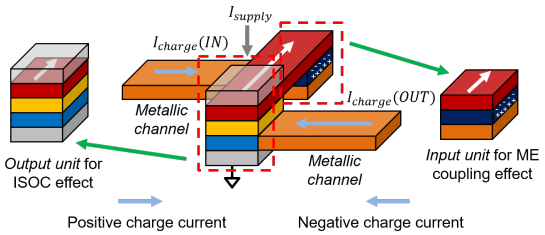

Fig. 1: Structure of a basic MESO inverter [2].

A basic MESO inverter [2] consists of several major components, as shown in Fig. 1: an *input unit* that uses ME coupling to transduce incoming charge current to a magnetic state variable in the in-plane ferromagnet (FM); an *output unit* that generates positive or negative charge current using the ISOC effect, depending on the magnetization in the FM; and a *metallic channel* that conducts charge current from an output unit of the previous stage to an input unit of the current stage.

Fig. 2(a) shows a pair of cascaded MESO inverters, each associated with a different state, as indicated by the magnetization direction of the FM in each stage. The presence of two states is characterized by the sign of a parameter, η, defined as the conversion ratio between the supply current from transistor and the current generated by the ISOC unit. The sign of η indicates whether the ISOC charge current injected by the output unit goes into ($\eta < 0$) or out of ($\eta > 0$) the metallic channel: this sign is determined by the direction of magnetization in the FM layer in the output unit. More details about η will be elaborated in Section II-B2. The operation of a single MESO inverter proceeds as follows:

(1) The charge current from the output of the previous stage is injected into the FE material in the input unit of the current stage. The FE material is modeled as a capacitor whose

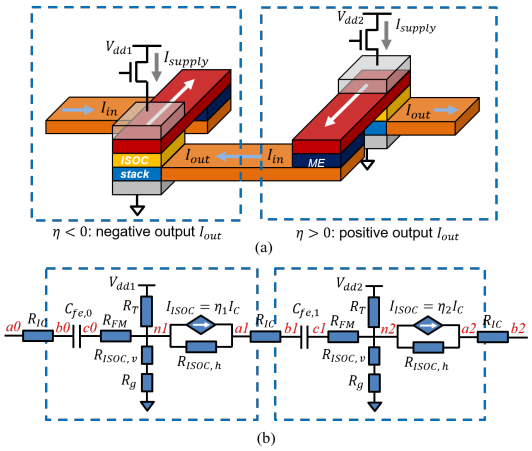

Fig. 2: Cascaded MESO inverters and their circuit model [2].

behavior is governed by the LKh equation [14], and the input current generates a voltage that switches its polarization.
(2) The FE capacitor voltage induces a magnetic field on the FM due to the ME effect, flipping its magnetization.
(3) The output unit has a transistor above the ISOC material stack and a ground contact beneath it. A charge current, injected through the transistor, is polarized to positive or negative spin current, depending on the magnetization in the FM [15]. This spin current flows into the ISOC conversion stack beneath the FM, which performs spin-to-charge conversion based on the inverse spin-Hall effect (ISHE) and the inverse Rashba-Edelstein effect (IREE) [6]–[8]. Depending on the spin current polarity, either positive or negative charge current flows into the metallic interconnect that drives the next logic gate.

B. Circuit model for a MESO inverter

In this section, we will introduce a circuit model of a MESO inverter and elaborate upon the ISOC current conversion model as well as the response of the FE capacitor polarization. We will then show how a MESO stage can be analyzed using numerical circuit simulation to extract its delay and energy.

1) Circuit model: A circuit model for the MESO inverter was proposed in [2]. We extend this model to show the model for cascaded pair of MESO inverters in Fig. 2(b), which shows the interations between successive stages. Our interest is in modeling the time required by this structure to charge the FE capacitor in the output unit, and accordingly we isolate the subcircuit that contributes to driving this capacitor and illustrate it in Fig. 3. This differs slightly from the model in [2], where node c was connected directly to ground; in contrast, we show that this path goes through a few resistors.

The transistor is connected to a supply voltage, V_{dd}, and is modeled as an effective resistance R_T. This is valid given that gate capacitance is small enough compared to the effective capacitance of the FE capacitor, and thus a gate transition does not induce a coupled voltage spike at the source that moves the transistor out of the linear region. Under the assumption that the transistor driving each stage is clocked during the transition, only the R_T for the current stage must be considered. The FM and the ISOC material stack are modeled as a vertical resistance $R_{ISOC,v}$, and are connected to the ground lead resistance, R_g. The generation of charge current from spin current is modeled as a current controlled current source (CCCS), with a horizontal resistance $R_{ISOC,h}$ representing the internal ISOC source resistance. The interconnect resistance R_{IC} associated with the metallic channels leads to one plane of the FE capacitor. The other plane of the FE capacitor is connected to a resistance R_{FM} representing entire horizontal resistance of FM. The FM is then connected to the vertical ISOC unit and the ground lead of the next MESO inverter, represented by $R_{ISOC,v}$ and R_g from the next stage.

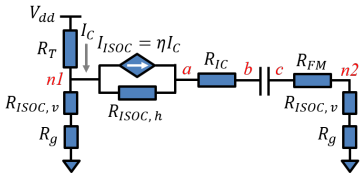

Fig. 3: Circuit model for a single MESO inverter [2].

2) Model for the ISOC unit: The spin-to-charge conversion occurs in the ISOC stack based on the ISHE and IREE effects. The conversion between the spin current I_s and the generated charge current I_{ISOC} can be written in the following form [2]:

$$I_{ISOC} = \frac{1}{w}\left[\lambda_{IREE} + \Theta_{SHE}\lambda_{sf}\tanh\left(\frac{t}{2\lambda_{sf}}\right)\right]\cdot I_s \quad (1)$$

Here, w is the width of the ISOC conversion unit and λ_{IREE} represents the IREE length [16]. The bulk ISHE is indicated by the spin-Hall angle Θ_{SHE}, spin diffusion length λ_{sf}, and thickness t. The spin current, I_s, injected into this stack is polarized by the FM from the charge current I_c, i.e.,

$$I_s = \pm P \cdot I_c \quad (2)$$

where P is the spin polarization. Therefore the conversion ratio $\eta = I_{ISOC}/I_c$ for the CCCS can be written as

$$\eta = \pm\frac{P}{w}\left[\lambda_{IREE} + \Theta_{SHE}\lambda_{sf}\tanh\left(t/2\lambda_{sf}\right)\right] \quad (3)$$

Using simulation parameters that will be detailed in Table I, the transient waveform for switching the voltage at node $n1$ and node b is shown in Fig. 4 when the sign of η changes from negative (before 0ps) to positive (after 200ps). It can be seen that the steady-state voltages for b are asymmetric about zero. To understand this, consider the steady state, where the FE capacitor can be treated as an open circuit, and no current flows through R_{IC}. Thus, the voltage drop on the FE capacitor equals the voltage drop at node b, i.e., the voltage across $R_{ISOC,h}$ plus the voltage of node $n1$. The plot shows that the voltage at node $n1$ settles to 8.0mV in the steady state. Since no current flows into R_{IC}, the charge current I_{ISOC} must flow to ground through $R_{ISOC,h}$. From Eq. (3), the magnitude of η is identical for either FM polarization, but the sign depends on the polarization: as a result, in this case, the voltage drop from node b to node $n1$ is $\pm$40mV. This results in asymmetric steady-state voltage levels of $8\text{mV}-40\text{mV} = -32.0\text{mV}$ and $8\text{mV}+40\text{mV} = +48.0\text{mV}$, as seen in Fig. 4.

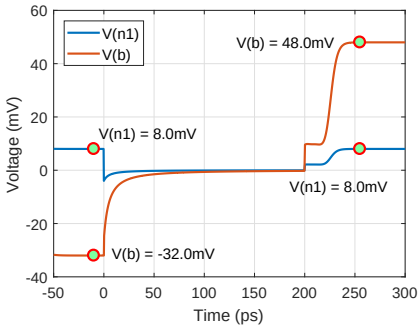

Fig. 4: Voltage at nodes $n1$ and b for a single MESO inverter, with negative η before 0ps and positive η after 200ps.

3) Model for the FE capacitor: The LKh equation [14], [17], [18] governs the temporal response of the electric polarization P in the FE capacitor to the electric field E:

$$\gamma \frac{dP}{dt} = \frac{1}{2}\beta E - g_2 P - g_4 P^3 - g_6 P^5 \tag{4}$$

where γ is a parameter indicating the switching speed, and β, g_2, g_4, and g_6 are obtained as fitting parameters that match experimental data to this theoretic model [18]. In the Supplementary Material, we demonstrate a hysteresis loop obtained based on Eq. (4) and the related remnant polarization.

C. Circuit simulation

The components associated with the MESO circuits in Figs. 2(b) and 3 can be classified into elements defined by linear algebraic equations (resistors, supply voltage source, CCCS), and by nonlinear differential equations (FE capacitor). We analyze this structure by discretizing the differential equations in time, and at each time step, using Newton-Raphson linearizations to obtain affine representations of circuit elements that are solved by modified nodal analysis (MNA).

We focus on the FE capacitor that is represented by the LKh equation, which is a nonlinear differential equation. We show below how the FE capacitor can be represented using an $I-V$ relationship, eliminating the polarization variable P.

We begin with the equation $Q = A(\epsilon_0 E + P) = A(\epsilon_0 V/T + P)$ that describes the free charge Q as a function of voltage V and polarization P on a capacitor with area A and a distance T between plates: here T is the thickness of the FE capacitor. Based on the above equation, we obtain the following linear relation between P, I, and V in the $(i+1)^{th}$ time step:

$$P = \left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0 V_i}{T}\right] \tag{5}$$

where V_i and V_i are the values of V and P, respectively, in the i^{th} time step, and h is the simulation time step. A derivation of Eq. (5) is provided in the Supplementary Material.

Next, we revisit Eq. (4) and replace electric field $E = V/T$:

$$\gamma \frac{dP}{dt} = \frac{\beta V}{2T} - f(P) \quad \text{where } f(P) = g_2 P + g_4 P^3 + g_6 P^5 \tag{6}$$

To eliminate P and create an $I-V$ relationship for the FE capacitor, we combine Eqs. (14), (5) and (6) to obtain the nonlinear $I-V$ relation at the $(i+1)^{\text{th}}$ time step:

$$g(I,V) = \left[\frac{\gamma}{A}\right] I - \left[\frac{\gamma\epsilon_0}{Th} + \frac{\beta}{2T}\right] V + \frac{\gamma\epsilon_0}{Th} V_i + f\left(\left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0}{T} V_i\right]\right) = 0 \tag{7}$$

where g is a polynomial in I and V. Using standard circuit simulation approaches, we now create an affine approximation to this function about a guess, (I^k, V^k), where the superscript k represents the Newton-Raphson iteration number:

$$g(I^k,V^k) + \left.\frac{dg}{dI}\right|_{I^k,V^k} (I - I^k) + \left.\frac{dg}{dV}\right|_{I^k,V^k} (V - V^k) = 0 \tag{8}$$

This provides a stamp [19] for the FE capacitor element, which when combined with the stamps for the resistors and CCCS, yields the MNA equations for each Newton-Raphson iteration.

The simulation method is summarized in Algorithm 1. After initialization (line 1), the entire simulation contains two nested loops: the outer loop (lines 2–12) performs time-stepping, setting up the computations for V, I, and P at each time step, while the inner loop (lines 5–10) performs Newton-Raphson iterations to solve the nonlinear equations at each time step. The Newton-Raphson iterations develop the affine form in Eq. (8) based on the partial derivatives of $g(I,V)$, (Eq. (7)), which is used to create and solve the MNA equations (line 8).

Algorithm 1 Simulation method for a MESO gate

Input: Circuit netlist, initial polarization P_0 and voltage V_0;
Output: Polarization P of the FE capacitor, voltage V and current I of every node in the circuit over the simulation period.
1: $t_i \leftarrow 0$, $i \leftarrow 0$, $P_i \leftarrow P_0$, $V_i \leftarrow V_0$. ▷ Initialization for time zero
2: **repeat**
3: $t_{i+1} \leftarrow t_i + h$, $i \leftarrow i+1$. ▷ Time-stepping to the next simulation time
4: $k \leftarrow 1$, $V^0 \leftarrow V_i$ and $I^0 \leftarrow I_i$. ▷ Newton-Raphson initializations
5: **repeat** ▷ Newton-Raphson iterations at time step i
6: Calculate dg/dI and dg/dV at I^k, V^k, based on $g(I,V)$ in Eq. (7).
7: Construct the affine relation between V and I based on Eq. (8).
8: Construct the MNA equations and solve them for V and I.
9: $k \leftarrow k+1$.
10: **until** V and I converge to the solution at time step i.
11: Use V and I to calculate P at time step i based on Eq. (5).
12: **until** End of simulation time.

D. Calculation of delay and energy for the MESO inverter

1) Calculation of the MESO inverter delay: The delay of a single MESO inverter includes two parts: the delay of switching the FE capacitor polarization, and the delay of switching the magnetization in the FM layer.

Delay of switching FE capacitor polarization: As mentioned in Section II-B2, the incoming charge current from previous MESO inverter is injected into the ME unit, creating a voltage drop across the FE capacitor and switching its polarization. The switching response of the FE capacitor polarization is governed by the LKh equation and simulated numerically using the techniques from the previous subsection. As a baseline example, we perform the simulation to measure the inverter delay based on the parameters in Table I. The resistances related to ISOC stack are estimated based on information from [20], with the rest of the parameters from [2]. For the FE capacitor, the parameters in Eq. (4) are set to

TABLE I: Simulation parameters for the MESO circuit.

Parameter	Value
V_{dd} (source voltage)	100mV
η (conversion ratio)	1.0
A (ferroelectric capacitor area)	$10 \times 10\text{nm}^2$
T (multiferroic layer thickness)	5.0nm
R_T (equivalent resistance of transistor)	23kΩ
R_g (ground lead resistance)	500Ω
$R_{ISOC,v}$ (vertical resistance of ISOC stack)	1.5kΩ
$R_{ISOC,h}$ (horizontal resistance of ISOC stack)	10kΩ
R_{IC} (resistance of interconnect)	1kΩ
R_{FM} (resistance of FM)	1kΩ
C_g (gate capacitance, per inverter)	0.2aF
V_g (gate voltage)	0.73V

$\beta = 500$, $\gamma = 3.5 \times 10^{-4}$, $g_2 = -2.0 \times 10^3$ Jm/C^2, $g_4 = -2.4 \times 10^9$ Jm^5/C^4, and $g_6 = 4.2 \times 10^{10}$ Jm^9/C^6 [18].

As elaborated in Section S.4 of Supplementary Material, the rise time t_r, defined as the time required for the signal to transition from its 10% point to its 90% point, is 28.9ps. The fall time is analogously defined and obtained as 46.8ps. The average switching delay is $t = (t_r + t_f)/2 = 37.9$ps.

As mentioned in Section II-B2, the voltage drop across FE capacitor (between node b and c) has a higher absolute value when η is positive (48mV) compared to the case when η is negative (32mV), leading to the asymmetry in the rising and falling transition as $t_r < t_f$. This symmetry is inevitable due to the circuit structure, but could be alleviated if the resistance to ground from $n1$, $(R_{ISOC,v} + R_g)$, could be reduced and/or if the conversion rate, η, could be increased. Both correspond to materials-related advances. For example, reducing the $(R_{ISOC,v}+R_g)$ from $2k\Omega$ to 500Ω at the same η would change the steady-stage voltages to 44.7mV for $\eta > 0$ and -40.4mV for $\eta < 0$, with $t_r = 26.6$ps and $t_f = 30.2$ps, and a smaller average delay of $t = 28.4$ps.

Delay of switching FM magnetization: After the polarization of the FE capacitor is switched, the FM magnetization will be switched due to the ME effect. This delay is added directly to the switching delay of the FE capacitor to obtain the inverter delay. As in [2], the switching delay of the FM is treated as a fixed time, which is determined by the in-plane FM material parameters and the FE material properties. When the sign of electric polarization P in the FE capacitor changes, this constant latency representing the switching of FM follows, after which the sign of η in the next MESO inverter becomes opposite to the sign of P in current MESO inverter.

2) Calculation of MESO inverter energy: The MESO device energy per transition consists of two parts: (i) the energy dissipated by the MESO inverter comes from the supply source through the transistor, i.e., the product of the source voltage V_{dd}, the current through the transistor resistance I_{supply}, and the delay of the MESO inverter t, and (ii) the energy for charging the gate capacitor, C_g. The total energy is given by

$$E = V_{dd} \cdot I_{supply} \cdot t + C_g \cdot V_g^2 \tag{9}$$

Note that the energy related to the ME coupling effect enabled FM switching is the charging energy of the FE capacitor. The charging process completes during the pulse t and is part of the first term in Eq. (9). For circuits with multiple MESO gates, if each gate i is pulsed for time t_i during its transition, the first term is altered to $V_{dd} \cdot I_{supply} \cdot \sum t_i$. Using the parameters in Table I, the rise and fall switching energies are 13.4aJ and 19.2aJ, respectively, where $C_g V_g^2 = 1.1$aJ in each case.

III. Sneak paths in cascaded MESO inverters

As stated in Section II-B2, since the FE capacitor acts as an open circuit at steady state, the voltage drop across a FE capacitor (between node b and c as shown in Fig. 3) in a single MESO inverter model is determined by the voltage drop across $R_{ISOC,h}$ (between node $n1$ and a), plus the node voltage at $n1$. In this figure, the voltage for one plate of the FE capacitor, at node c, is zero since no current flows through the resistors between c and ground in steady state; the same is true of the simpler model in [2], where c is directly connected to ground.

However, the simplifications of considering a single stage must be reexamined for the case where inverters are cascaded. The circuit model for this case is shown in Fig. 2(b). Assuming that each stage is clocked while it is switching, the transistor for the first gate is turned off after $C_{fe,1}$ is charged, and the transistor for the second gate is turned on. In other words, R_T for the second gate was an open circuit while $C_{fe,1}$ was being switched, but enters the circuit after the FE capacitor is charged. This creates two sneak paths:
(i) A discharging path from b to ground through $R_{ISOC,h}$ and R_g (the CCCS goes to zero since $I_s = 0$ when the transistor is off), that sets the voltage of b to zero in the steady state.
(ii) An additional charging path to c through $n2$ that could corrupt the stored value on $C_{fe,1}$.

If only the former path were present, this would not be a cause for concern, since the polarization would move to its nonzero remnant polarization value when the voltage across the capacitor decays to zero. In this section, we show that the latter sneak path, when coupled with the former, may change the voltage drop across the FE capacitor and thus inadvertently switch its polarization under some clocking scenarios. This can be avoided, but imposes additional overheads and delay constraints in the design of MESO gates. We now consider the following two clocking scenarios:

- *Pulsed clocking:* Each MESO inverter in a cascade is turned on by a single pulse for a certain period of time.
- *Always-on:* Every MESO inverter in a cascade is turned on for the entire period of operation of the circuit.

A. Sneak paths under pulsed clocking

Fig. 5 shows the voltage waveform that clocks the transistors for two successive stages in a cascaded MESO inverter chain, and the circuit models during these two pulses. The operation of the circuit can be divided into several steps:

• As shown in Fig. 5(b), when the first pulse $t_{on,1}$ turns on the supply current, the generated ISOC current will start to charge the FE capacitor in the first stage. For illustration, we consider the case where $\eta > 0$ (the $\eta < 0$ case is analogous): here, the voltage drop across $C_{fe,1}$ will be positive ($V(b) > V(c)$) and the polarization will switch to its positive saturation value.

• Next, in the off period t_{off}, the polarization in $C_{fe,1}$ drops towards its remnant value, and the magnetization in the

adjacent ferromagnet is switched by the ME effect.

• The second pulse, $t_{on,2}$ in Fig. 5(a) corresponds to the circuit shown in Fig. 5(c), and serves to charge node b_2, setting $C_{fe,2}$ to a negative polarization. However, this pulse will also pull up the voltage at node c_1 through the path $V_{dd2} \rightarrow n2 \rightarrow c2$, while the sneak path $b1 \rightarrow a1 \rightarrow n1 \rightarrow$ ground will discharge the plate of $C_{fe,1}$ on the node $b1$ side. Thus, a negative voltage between node $b1$ and $c1$ may be created. This voltage sets up a transient that can change the polarization of $C_{fe,1}$ from positive to negative, which may cause an inadvertent error.

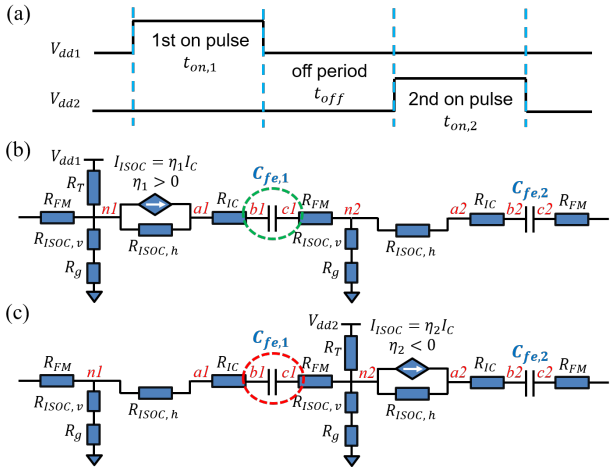

Fig. 5: (a) A pulsed clocking waveform. (b) and (c) Equivalent circuit representations during successive clock pulses.

For the case when $t_{on,1} = t_{on,2} = 50ps$ and $t_{off} = 200ps$, as shown in Fig. 6(a), under the technology parameters in Table I, we show the transient behavior of the polarization in the FE capacitor, $C_{fe,1}$, in Fig. 6(b). The choices for the on pulse width are based on our simulation results for single inverter transition time as in Section II-D1. The polarization should have remained positive after 50ps, but it can be seen an inadvertent error is caused as $C_{fe,1}$ is switched to a negative polarization during $t_{on,2}$ due to the sneak path.

This inadvertent error may be avoided by optimizing the operation periods. For example, in Fig. 7, when we alter $t_{on,1} = t_{on,2} = 25$ps, the polarization remains positive even after the second pulse, even in the presence of a sneak path.

B. Sneak path effects under always-on clocking

The always-on clocking model negates the effect of sneak paths completely. Under this model, all transistors are on for the entire duration, and the circuit model is identical to that shown in Fig. 2(b). In this mode, the two nodes $b1$ and $c1$ on the two sides of the two plates for $C_{fe,1}$ are both connected to supply current paths, and there is no sneak path discharging the FE capacitor. However, the energy consumption here is high as the V_{dd} supply constantly provides current to the system.

In summary, the pulse time matters in several respects. As explained in Section II-D2, smaller pulse time is preferred for lower energy consumption. Nonetheless enough pulse width is still required to guarantee successful switching. Pulse time is also important in the occurrence of sneak path effects as

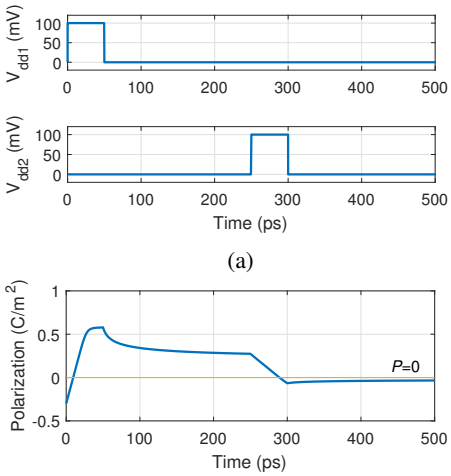

Fig. 6: (a) Waveform for two successive on pulses (50ps pulse width, 200ps off time) for two cascaded MESO inverters, resulting in (b) an inadvertent polarization error in $C_{fe,1}$.

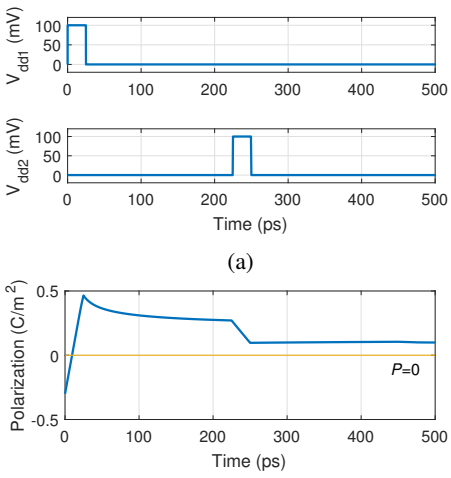

Fig. 7: (a) A modified waveform with 25ps pulse width, 200ps off time. (b) $C_{fe,1}$ functions correctly, retaining $P > 0$.

discussed in Fig. 6 and Fig. 7. Choosing a proper pulse time (25ps in Fig. 7) could prevent the electric polarization from going to the undesired negative region (as seen in Fig. 6(b) at 300ps) due to the sneak path, while the FE capacitor still have enough time to complete a successful switching.

IV. MESO-BASED MAJORITY GATE DESIGN

We now discuss how to construct a majority gate based on two approaches for switching the FE capacitor polarization at the next stage. We use the gate inputs to either

- generate competing domain walls (DWs) that switch the magnetization at the FM output, or
- generate competing charge currents.

These gates calculate the minority amongst the three inputs. Instead of using the term "minority gate" or "majority complementary gate", we use the term "majority gate" as in [21].

A. Majority gate using competing DWs in the FM

A three-input majority gate could be formed by feeding each input to a structure similar to a MESO inverter, and connecting their FMs together into a single merged structure driving an output ISOC unit, as illustrated in the Fig. 8. Each input ME unit switches the magnetization of the partial FM region above it, and propagates a domain wall that transmits the magnetization from three input branches to the junction. The majority magnetization will propagate to the output branch O in a properly designed FM [22] with a switching time of 200ps. Next, as in the case of the MESO inverter: the magnetization at the output O determines the direction of the charge current generated out of the ISOC unit in the output stack, switching the polarization of the input FE capacitor of the next gate.

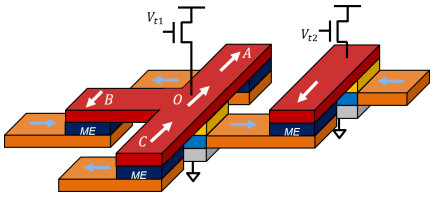

Fig. 8: A majority gate with competing DWs.

In computing the energy for a gate, we count the energy required to switch O and to switch the input FE capacitor of the next gate. Therefore, the energy for switching the polarization in the FE capacitors in each input ME unit of the current gate is counted towards the energy consumption of the previous MESO gates. Based on this approach, the energy for this majority gate is identical to a single MESO inverter, as given by Eq. (9), and consists of the energy required to drive the load FE capacitance and the energy required to switch the transistor above O. Similarly, the delay corresponding to switching the polarization of the load FE capacitor is the same as that for a single MESO inverter delay, and as before, the delay of propagating the signal through the FM is treated as a constant. Therefore, the delay and energy consumption of this majority gate is the same as that in Section II-D1.

B. Majority gate using charge currents

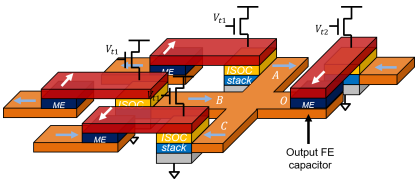

Fig. 9: A majority gate based on competing charge currents.

Alternatively, majority gates can be implemented using the charge current, as shown in Fig. 9. Here, the three metallic channels A, B, and C going out of each ISOC unit merge together and connect to a common FE capacitor though the output branch O. The majority direction of the charge current in the three metallic channels determines whether the voltage drop on the output FE capacitor is positive or negative, which realizes the majority function. We show that the current to the load is not the algebraic sum of the I_{ISOC} values in each of the three branches, and other circuit elements also play a part.

1) The output voltage of the majority gate: The operation of the gate is captured by the circuit model in Fig. 10. The polarization each FE capacitor $C_{fe,k}$ $(k = 1, 2, 3)$ determines the magnetization in the adjacent magnets through the ME effect, and consequently the sign of η for each ISOC unit. The sign of each η indicates not only the direction of charge current in the three channels, but also the voltage level at nodes $n4$, $n5$, and $n6$: a positive η results in $V(ni) > 0$ $(i = 4, 5, 6)$ in the corresponding branch; otherwise $V(ni) < 0$.

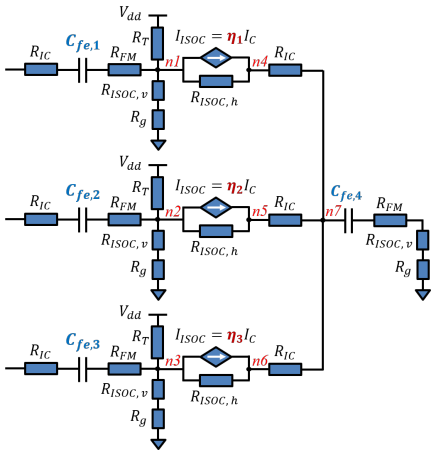

Fig. 10: Circuit model for the charge-based majority gate.

Since an FE capacitor is an open circuit in the steady state, the voltage drop across $C_{fe,4}$ is determined by $V(n7)$ with the opposite plate at ground. The voltage at node $n7$ is a result of voltage division between $V(ni)$ $(i = 4, 5, 6)$ through the channels: a branch with $\eta > 0$ induces a higher voltage and will inject current into the branch with $\eta < 0$, so that

$$\min_{i\in\{4,5,6\}} V(ni) \leq V(n7) \leq \max_{i\in\{4,5,6\}} V(ni) \qquad (10)$$

Therefore, if the inputs with positive η are in the majority [minority], $V(n7)$ will stabilize at a positive [negative] value.

TABLE II: Steady-state voltages in a charge current based MESO majority gate for different input combinations.

Sign of η on the inputs	Node voltages			
	$V(n4)$	$V(n5)$	$V(n6)$	$V(n7)$
$+\ +\ +$	48.0mV	48.0mV	48.0mV	48.0mV
$+\ +\ -$	25.5mV	25.5mV	19.4mV	23.5mV
$+\ -\ -$	1.2mV	−5.2mV	−5.2mV	−3.1mV
$-\ -\ -$	−32.0mV	−32.0mV	−32.0mV	−32.0mV

From Table II, the cases with three or zero positive η values show no voltage difference between $V(ni)$ $(j = 4, 5, 6)$, and thus $V(n7)$ equals each $V(ni)$ since no current flows through the metallic channel. In the other two cases, the positive η branch(es) inject(s) current into the negative η branch(es), even in the steady state. This creates a voltage divider that determines the voltage at the intermediate node, $n7$.

The voltage values are not symmetric, e.g., the case where all inputs have $\eta > 0$ has a larger output voltage than the case where all inputs have $\eta < 0$. The root cause of this is similar to the asymmetry seen in the voltage drop on the FE

capacitor in a MESO inverter under negative and positive η, as discussed in Section II-B2. For cases where all three η values do not have the same sign, the magnitude of $V(n7)$ is even lower, although for these parameter values, the majority gate operates correctly, i.e., the sign of the voltage at $n7$ matches the majority sign of the η values at the gate inputs.

However, this may not always be true, and $V(n7)$ depends on the voltage divider action. In fact, if the value of $(R_{ISOC,h} + R_g)$ is too high, the voltage for the $+\ -\ -$ case may not go below zero, and the output FE capacitor may incorrectly carry a positive P. This effectively places an upper bound on $(R_{ISOC,h}+R_g)$. Keeping all other simulation parameters unchanged, if this total resistance is increased from 2KΩ to 3KΩ, then the polarization will not be switched to a negative value. In this case, the values of $V(n4)$, $V(n5)$, and $V(n6)$, are 4.2mV, -1.9mV, and -1.9mV, respectively. The voltage divider action then sets $V(n7) = 0.13mV$, which incorrectly results in $P > 0$ at the output FE capacitor.

Practically, switching at small voltages such as 3.1mV is challenging under current technologies and may even fail since it is smaller than the coercive field of typical candidate materials. Increasing the value of η or $R_{ISOC,h}$ and decreasing R_g or $R_{ISOC,v}$ in new technologies can help in raising the voltage to a higher value. For example, reducing $R_g+R_{ISOC,v}$ from $2k\Omega$ to $1k\Omega$ and increasing η from 1.0 to 2.0 would raise the voltage from 3.1mV to 17.8mV.

TABLE III: Transition times for the output FE capacitor polarization in a charge current based MESO majority gate.

	Before transition		After transition		Delay	Energy
	Input η	$V(n7)$	Input η	$V(n7)$	(ps)	(aJ)
Rise	$-\ -\ -$	-32.0mV	$+\ +\ +$	48.0mV	13.5	18.5
	$-\ -\ -$	-32.0mV	$+\ +\ -$	23.5mV	26.0	34.1
	$-\ -\ +$	-3.1mV	$+\ +\ +$	48.0mV	11.7	16.4
	$-\ -\ +$	-3.1mV	$+\ +\ -$	23.5mV	22.4	30.6
Fall	$+\ +\ +$	48.0mV	$-\ -\ -$	-32.0mV	21.3	26.5
	$+\ +\ +$	48.0mV	$+\ -\ -$	-3.1mV	155.4	188.4
	$+\ +\ -$	23.5mV	$-\ -\ -$	-32.0mV	20.4	25.9
	$+\ +\ -$	23.5mV	$+\ -\ -$	-3.1mV	154.1	189.0

2) Energy and delay of the majority gate: Table III provides a summary of the rise and fall transition time under various input combinations. The overall delay of the majority gate is the transition time listed, added to the 200ps delay of the ferromagnet. A rise transition goes from a case where the majority of η values is negative to one where the majority is positive. From Table II, the negative and positive majorities each correspond to two cases, and therefore four cases must be considered. The same is true of the fall transition.

The table shows a large range of delay values for the 90% switching time of the output FE capacitor polarization, depending on the initial and final input states. This can be ascribed largely to the voltage drop on the FE capacitor after the transition: larger steady-state values of $V(n7)$ correspond to smaller delays. There are two cases in the fall transition time that are significantly larger than others, when inputs transition to $+\ -\ -$ from different input states. Here, the final steady-state voltage at $n7$ has the smallest magnitude. This causes a small electric field across the FE capacitor, resulting in a slow transition. Considering the worst-case transition, for a three-input majority gate based on charge current, we have $t_r = 26.0$ps, $t_f = 155.4$ps, and the average delay $t = 90.7$ps.

The last column in Table III shows the energy dissipation of the charge current based majority gate implementation. Similar to the single MESO inverter case, the energy of the majority gate is the summation of energy from the V_{dd} source at each branch within the transition time. Long transition times naturally involve large energy dissipation, e.g., the energy for the fall transition of $t_f = 155.4$ps is 188.4aJ, much higher compared to most of the other cases. Notice that there is another case with a delay of $t_f = 154.1$ps but a slightly higher energy of 189.0aJ. These two cases both share the same input states after transition, but the input state for the latter case before transition is composed of two positive η and one negative η, meaning that there are currents flowing between node $n4$, $n5$ and $n6$ at the beginning of the transition. Therefore the averaged current during the transition is slightly higher and incurs a larger energy in the latter case. These values are much higher than the DW based majority gate.

3) Improving the worst-case delay using STEM: For cases where the difference between the best- and worst-case delays is large, the work in [23] had proposed STEM, a two-phase majority gate scheme for faster operation. We now show how STEM can be applied here to reduce the energy and delay.

In the first phase, STEM uses an initialization pulse to preset the polarization at the output with only one input branch activated. Immediately after this initialization phase ends, a short evaluation pulse is applied to the other two branches. If η for these two branches have opposite signs, then the majority value corresponds to the initial value. In this case, under the short pulse, $V(n7)$ will be close to zero (even under asymmetric voltage levels), and the short pulse will not be applied for long enough to switch the polarization, and the majority function is correctly evaluated. On the other hand, if the two branches in the later phase have the same sign of ηs, they will induce a large voltage magnitude at $n7$, which will cause the polarization at the output to be switched very fast.

The two-phase STEM switching process is illustrated under an initialization pulse of 75ps and an evaluation pulse of 25ps, as in Fig. 11(a). We first consider the scenario where the input switches from η values of $+\ +\ +$ to $-\ -\ -$ in Fig. 11(b). During the 75ps initialization phase, the output switching to one of the incoming inputs, corresponding to a negative polarization. In the second phase, this polarization is reinforced by two negative inputs, resulting in a net negative polarization at the end of the second pulse. The FE capacitor then returns to its remnant polarization, as seen in the figure.

Next, in Fig. 11(c), we show the fall transitions when the input switches from from $+\ +\ +$ to $+\ -\ -$. If the initialization activates a branch of negative η, the first pulse results in an identical waveform as the previous case. The second pulse causes a small increase in the polarization: this is caused by a positive $V(n7)$ due to asymmetry, when one branch with negative η and one branch with positive η are activated at the same time, and is a result of the voltage divider that determines $V(n7)$. As stated earlier, this is influenced by $(R_{ISOC,v}+R_g)$: in the same figure, we show another curve that considers a smaller value of $(R_{ISOC,v} + R_g)$: here, the polarization at the end of the second pulse is more negative. The smaller

value demonstrates better switching and takes the polarization to saturation faster and suggests that the widths of the first pulse used in the two-phase scenario can be further reduced.

This STEM scheme reduces the worst-case delay from 155.4ps to 100ps, the sum of the two pulse widths, and results in an average energy of 42.5aJ, significantly better than the 188.4aJ associated with the worst case and the 66.2aJ average over all cases in Table III. The energy of charging the gate capacitor per transistor under STEM is also 1.1aJ, the same as that for charging a single MESO inverter. The two-phase scenario may incur slightly more overhead for clock distribution, which is not included in our energy estimate.

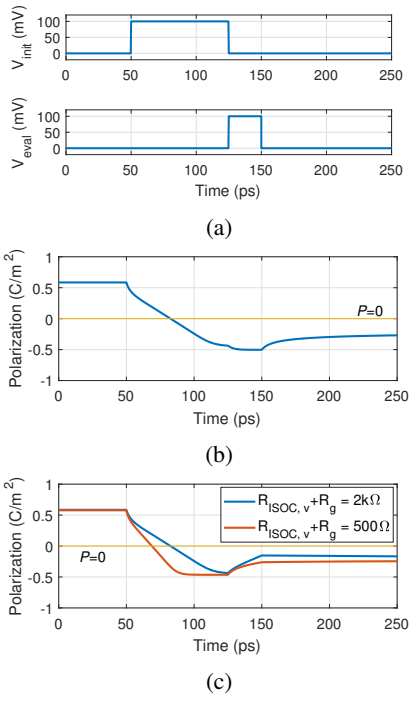

Fig. 11: (a) The two-phase STEM pulse. (b) A fall transition with inputs going from 3 positive η to 3 negative η. (c) Two fall transitions with inputs going from 3 positive η to 2 negative η and 1 positive η, for different values of $R_{ISOC,v} + R_g$. The initialization phase activates one of input branches with $\eta < 0$.

V. Conclusion

This paper has introduced a method to simulate the performance of the MESO device, incorporating the LKh equation for FE capacitor polarization switching into traditional MNA-based circuit simulation to compute the energy/delay under realistic parameters. The paper has also presented the potential sneak path issue that may induce inadvertent logic errors in the cascaded MESO inverter chain. Two different majority gate implementations are proposed and analyzed based on the two computation mechanisms in the MESO device. For the charge based majority gate, some input scenarios may be unable to reach the coercive field of the material, which results in switching failure: this is avoided by the STEM-based scheme.

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SUPPLEMENTARY MATERIAL

S.1 HYSTERESIS LOOP AND REMNANT POLARIZATION OF THE FE CAPACITOR

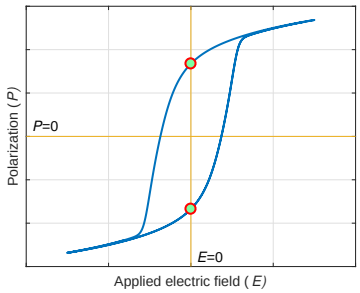


Fig. 12: A hysteresis loop in the $P-E$ plot of the FE capacitor.

Fig. 12 shows a hysteresis loop for P under a sinusoidal electric field, E. When E is turned off, the polarization settles at one of two remnant values in the plot along the $E = 0$ axis.

S.2 DERIVATION OF LINEAR $I-V$ RELATIONSHIP FOR THE FE CAPACITOR BASED ON LKH EQUATION

To develop the $I-V$ relation for the FE capacitor, we begin with the equation $Q = A(\epsilon_0 E + P) = A(\epsilon_0 V/T + P)$. In the derivative form, this yields the following equation:

$$I = \frac{dQ}{dt} = A\left(\frac{\epsilon_0}{T}\cdot\frac{dV}{dt} + \frac{dP}{dt}\right) \tag{11}$$

We can see from the above equation that in the steady state, where all d/dt terms are zero, the FE capacitor can be treated as an open circuit; this fact was used in Section II-B2.

We discretize time using the backward Euler numerical integration formula with a time step size of h. If V_i and P_i are the values of V and P, respectively, in the i^{th} time step, then in the $(i+1)^{\text{th}}$ time step,

$$V = V_i + h\cdot\frac{dV}{dt} \tag{12}$$

$$P = P_i + h\cdot\frac{dP}{dt} \tag{13}$$

Substituting Eq. (12) into Eq. (11),

$$\frac{dP}{dt} = \frac{I}{A} - \frac{\epsilon_0}{T}\left(\frac{V-V_i}{h}\right) \tag{14}$$

Further, Eq. (13) can be combined with Eq. (14) to obtain a linear relation between P, V, and I:

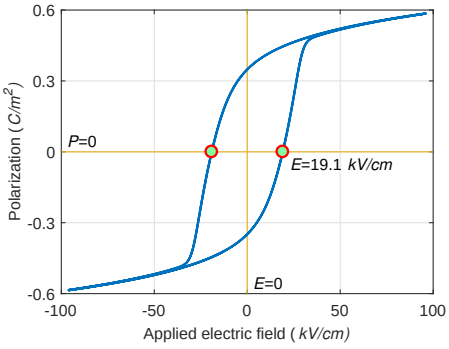
$$P = \left[\frac{h}{A}\right] I - \left[\frac{\epsilon_0}{T}\right] V + \left[P_i + \frac{\epsilon_0 V_i}{T}\right] \tag{15}$$

which is the Eq. (5) presented in Section II-C

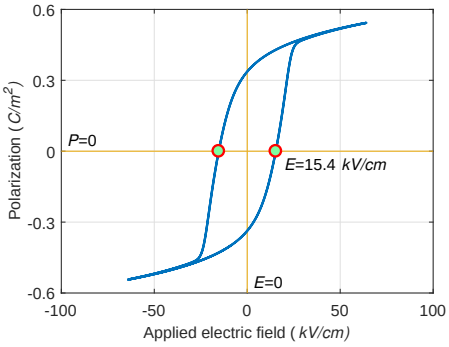
S.3 HYSTERESIS LOOPS UNDER VARIOUS APPLIED FIELDS

In this section, we show the hysteresis loops corresponding to a few switching voltages for the FE capacitor. The charge on the FE capacitor at the saturated voltage can be inferred, and the required coercive field is seen from these plots.

According to Eq. (4), we plot the hysteresis loops of P under sinusoidal electric fields E with the different maximum values E_m and mark the corresponding x-intercepts with electric field axis in Fig. 13. Formation of these hysteresis loops indicates that sucessful switching is achievable under these voltages. The concept that the shape of the hysteresis loop depends on E has been previously observed in [18]. The corresponding polarization charge under 48mV, and 32mV are 58.5aC, and 54.3aC with an area $A = 100\text{nm}^2$.



(a)



(b)

Fig. 13: (a) Hysteresis loop under (a) maximum voltage of 48mV ($E_m = 96$kV/cm) with corresponding x-intercept $E = 19.1$kV/cm; (b) maximum voltage of 32mV ($E_m = 64$kV/cm) with corresponding x-intercept $E = 15.4$kV/cm. The thickness of the ferroelectric material in each case is 5nm.

S.4 RISE AND FALL TRANSITION FOR A SINGLE MESO INVERTER

To measure the rise transition time, we set the electric polarization to the negative saturation value before applied the clocking pulse to the transistor. Then we use a pulse of 100ps long enough to make sure the complete the switching of the electric polarization P. When the pulse is applied, the transition of electric polarization P occurs. We measure the rise time of 28.9ps from the point of its 10% saturation value to its 90% point as illustrated in Fig. 14. Similarly, the fall transition time is 46.8ps as seen in Fig. 16. The dynamic responses of voltage and current associated with rise and fall transitions are also shown in Fig. 15 and Fig. 17.

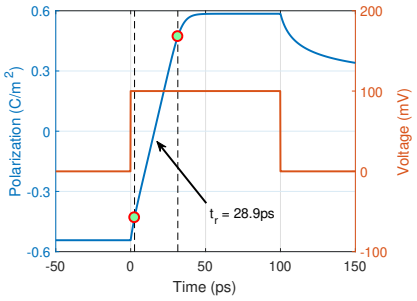


Fig. 14: Simulated rise transition in a MESO inverter: polarization and voltage pulse.

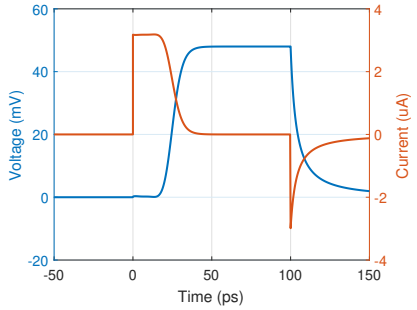


Fig. 15: Simulated rise transition in a MESO inverter: voltage and current versus time.

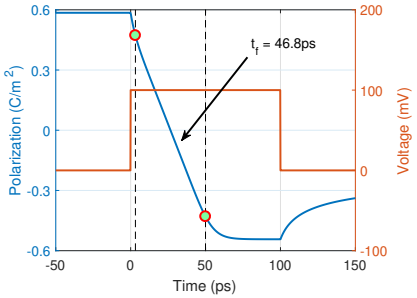


Fig. 16: Simulated fall transition in a MESO inverter: polarization and voltage pulse.

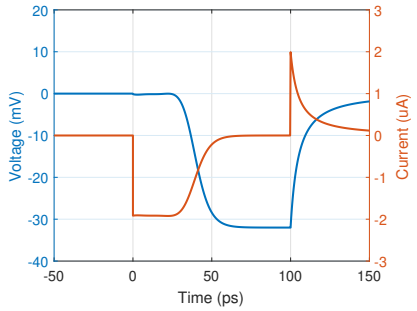


Fig. 17: Simulated fall transition in a MESO inverter: voltage and current versus time.