

OUTLINE

- Motivation
- Specific Power and Ground Problems and Solutions
- Symbolic Analysis Role
- Modeling of Power and Ground Buses
- Admittance and Current Estimation Techniques
- Moment Computations
- Time Domain Transformation
- Preliminary Experimental Results
- Conclusions
- Future Work

MOTIVATION

- High-speed circuits ->Gigahertz clock rates -> Increased switching activity
- Feature sizes to deep submicron levels
- · Vdd levels going down to conserve power
- Power and Ground buses cannot be assumed to be perfect conductors
- P&G buses must be designed carefully to ensure that supply voltage levels are maintained at appropriate levels.
- Better CAD techniques needed for estimation of voltage drops in P&G buses for functional and physical reliability in integrated circuits.

SPECIFIC P&G PROBLEMS

- Functional and Physical reliability
 - Increased resistivity in P&G distribution network due to smaller feature sizes
 - Reduces the current carrying capabilities of P&G networks
 - High current transients in P&G buses
 - Voltage drops across the P&G networks
 - Can lead to incorrect logic operation - and/or reduction in switching speeds

 - Lifetime reductions and complete failure due to electromigration
 - Also contributes to an increase in dynamic power dissipation

PROBLEM SOLUTIONS

- Accurate estimates of voltage drops and current densities in P&G buses
 - Use circuit level analog simulators (like SPICE) for current and voltage estimations
 - The main problems are the Time and Computational cost due to size of P&G networks
- Faster simulation times achieved by using
 - custom tools targeted towards solving this specific problem
 - simplified device models
 - make use of tree or mesh structures of P&G networks - find reduced order approximation of the transfer functions
 - problems include loss of accuracy and algorithm stability
- All solutions proposed so far are numeric in nature

SOME EXISTING ALGORITHMS

- J. E. Hall, D. E. Hocevar, P. Yang, and M. J. McGraw, "SPIDER-- a CAD system for modeling VLSI metallization patterns," IEEE Transactions on CAD, Nov. 1987.
 - Estimates Median-Time-to-Failure for each section of a metal bus
 - Makes use of SPICE runs
 - User must provide estimates of current sources
- S. Choudhury and M. A. Breuer, "Optimum design of IC power/ground nets subject to reliability constraints," IEEE Transactions on CAD, July 1988.
- More general technique
- Takes into consideration electromigration and voltage drops
- from leaf to node
- Transform the problem into an unconstrained optimization problem

SOME EXISTING ALGORITHMS (cont ...)

- R. Dutta and M. Marek-Sadowska, "Automatic sizing of power/ground P/G networks in VLSI," Proceedings DAC, pp. 783-786, 1989.
 - Modeled as a nonlinear programming problem
 - Cost function is the sum of the segments areas
 - Constraints are wire width
 - Convergance is not necessary, meaningful results are achieved at any time the iterations are terminated
 - achieved at any time the iterations are terminated

 T. Mitsuhashi and E. S. Kuh, "Power and ground network topology optimization for cell-based VLSIs," in Proceedings of the ACM/IEEE Design Automation Conference, pp. 524-529, 1992.

THIS ALGORITHM SYMBOLIC ANALYSIS

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- Motivation: Use of SPICE is computationally expensive and other current methods use simplified current estimation techniques but are limited to performing DC analysis
- Sapatnekar and Shah presented a method (1996) that uses frequency domain techniques:
 - not limited to a resistive or any one class of networks
 - can perform transient analysis (with simplified models)
 - near linear algorithm (in the size of the network)
 - results within 1% of SPICE
- The algorithm is very suitable for symbolic analysis because of its linear models, frequency domain techniques and repetitive evaluations





- Modeled as a set of segments connected in the form of a tree
- Each segment is modeled using a lumped RC







• where l_i is the length of the ith segment, $\,\omega_i$ is the width of the ith segment, $\,\rho$ is the sheet resistance and $\boldsymbol{\beta}$ is the wire capacitance per unit area



SYMBOLIC ANALYSIS **APPLICATION**

- The algorithm computes the time domain voltage waveform at each node for every time instance
- Two steps, which are repeated for every time point at which one or more switches changed states.
- 1) Solve a set of equations of the form
 - (G + sC) V(s) = J(s)

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- using an efficient path tracing algorithm, to obtain V(s). Given V(s) at every node, compute the time domain response by approximating V(s) with a rational Padé approximation.

Both steps are perfectly suitable for symbolic analysis: Linear, fixed topology network that requires many computational iterations



ALGORITHM OUTLINE

- Construct interval
- Select every element in the interval list in that order
- Set the corresponding switch states
- Process the interval (compute new states)
- Repeat with the the new switch states and computed initial conditions for next interval.
- Continue until all the intervals are processed.

COMPUTATION WITHIN AN INTERVAL

- The initial conditions on the capacitors are taken into consideration
- Compute the moments of each node voltage in the P&G networks
- Generate a stable Padé approximation
- Transform to a time domain voltage waveform
- The response is used to compute the initial conditions at all the nodes at the time of the next switching event
- Repeat the process

COMPUTATION WITHIN AN INTERVAL (continued...)

 $\label{eq:second} \begin{array}{l} \cdot S = Set of switches connected to the P&G bus \\ \cdot E = \{e_{1,\dots,m_k}\} is the set of all the segments in T \\ \cdot I = \{i_k \mid k = 1,\dots,m_k\} is the interval list \\ \cdot i_k is the i^k interval \\ \cdot associated with each interval is a subset of switches s_k and their states p_k \\ \cdot i_k is the time span of interval i_k \\ \textbf{BEGIN ALCORITHM Vdrop()} \\ I = IntervalList(); \\ \textbf{foreach } j \ in \ s_k \ and \ state(j) \ in \ p_k \\ SetSwitch(T_j, state(j)); \\ \textbf{foreach } n \ in \ Nodes(T) \\ \textbf{f}_{(0)} = TimeDomainResponse(moments(n)); \\ SetInitalCondition(n, f_0(k)) \\ \textbf{END ALCORITHM Vdrop()} \end{array}$

MOMENT COMPUTATION BY PATH TRACING

- Computation of moments of the voltage at any given node
- Recursively reduce the subtrees rooted at the given node n to an admittance $Y_{\rm Ti}(n)$ and a current source $J_{\rm Ti}(n)$

where

 $v_{Tri}(n)$ is the equivalent admittance of the subtree T_i , as seen from node n to the ground $J_{Tri}(n)$ is the combined effect of all the switch elements in T_i which have contributed to the current in the ground net.



MOMENT COMPUTATION (continued...)

- The equivalent current sources and admittances are computed for every node in linear time using a path tracing algorithm.
- The algorithm proceeds from the leaf-nodes, which are the contact points at the terminating segments of the ground net.
- A leaf-node could have multiple switches but exactly one segment connected to it.



SYMBOLIC MODEL COMPUTATION

- J(n) and Y(n) can be computed symbolically
- It is the same as a symbolic implementation of Norton's theorem
- SCAPP used to generate a sequence of expressions
- A simpler symbolic implementation possible
- The equivalent current source of a single switch i is given by:

$$J^{i} = \frac{V_{c}}{s} \frac{sC_{net}}{1 + R_{d}sC_{net}}$$

SYMBOLIC MODEL COMPUTATION

- + V_{c} is the initial voltage on the capacitor C_{net} at the start of the given interval.
- The pole at the origin in indicates that $C_{\text{net}} \, is \, modeled \, as$



SYMBOLIC MODEL COMPUTATION (continued....)

- Using Maclaurin series polynomial $J^i(n) = V_c(sC_{net} R_dsC_{net}^2 + R_ds^2C_{net}^3 + \dots)$ approximations we have
- Total admittance and equivalent current is: $Y^i = \frac{sC_{net}}{1 + R_dsC_{net}}$
- The expressions includes the effect of all the switches with binary Y operators controlling the closing and opening of the switches during the evaluation phase

$$\begin{aligned} r^{i} &= sC_{net} - R_{d}s^{2}C_{net}^{2} + R_{d}s^{3}C_{net}^{3} + \dots \\ Y(n) &= \sum Y^{i}\forall i \in \text{ Switches at n} \\ J(n) &= \sum J^{i}\forall i \in \text{ Switches at n} \end{aligned}$$

Page 7

EFFECT OF THE CURRENT SOURCES

- The effect of the equivalent current sources is propagated to every node in the network
- Terminate segment e in the ground network, connecting a single contact point u to the rest of the network, rooted at v



EQUIVALENT ADMITTANCE

• The admittance and the equivalent current source, as seen into edge e from node v is computed as

$$\begin{split} Y(v) = &\frac{1}{R(e) + \{Y_0(u) + (Y_1(u) + 0.5C(e)) * + ... + Y_{2n-1}(u): 2^{2n-1} \}^{-1}} + 0.5C(e) \\ = &\frac{Y_0(u) + (Y_1(u) + 0.5C(e)) * + ... + Y_{2n-1}(u): 2^{2n-1}}{(1 + R(e)Y_0(u)) + R(e)(Y_1(u) + 0.5C(e)) * + ... + \ell_R(e)Y_{2n-1}(u): 2^{2n-1}} + 0.5C(e) \end{split}$$

which yields

where

$$Y(v) = Y_0(v) + Y_1(v)s + Y_2(v)s^2 + \dots + Y_k(v)s^k + \dots$$

 $Y_k(v) = \frac{Y_k(u) - \sum_{i=1}^k R(e) Y_{k-i}(v) Y_i(u)}{1 + R(e) Y_0(u)}$

EQUIVALENT CURRENT SOURCE

Using Norton's theorem (shorting node v to ground) we get

$$J_k(v) = J_0(v) + J_1(v)s + J_2(v)s^2 + \dots + J_k(v)s^k + \dots$$

where

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$$J_{k}(v) = \frac{J_{k}(u) - \sum_{i=1}^{k} R(e)J_{k-i}(v)Y_{i}(u)}{1 + R(e)Y_{0}(u)}$$

Thus, we say that the equivalent admittance and current source have been propagated from node u to v

GENERALIZING THE ALGORITHM

- The above case only considers the switches connected to leaf-nodes
- In general, switches can be connected to any node
- In cases where a node has more then one segment and multiple switches connected, the switches are processed in a similar manner
- The admittance and current source can be propagated if and only if a maximum of one segment is left unprocessed at the given node.

GENERAL NODE CASE

 Since each node n in a P&G network is a root of a subtree T_i, the equivalent devices seen through edge e_i can be computed by



$$J^{e_i}(n) = \sum_{j=1, j \neq i}^k J_{T_j}(n)$$

$$Y^{e_i}(n) = \sum_{j=1, j \neq i}^k Y_{T_j}(n)$$

GENERAL NODE CASE (continued...)

• Voltage moments at n:

Voltage moments at ii.

$$J(n) = \sum_{i=1}^{k} J_{T_i}(n)$$

$$Y(n) = \sum_{i=1}^{k} Y_{T_i}(n)$$
where
$$Y(n) = \sum_{i=1}^{k} Y_{T_i}(n)$$

Moments of V(n):

$$V(n) = V_0(n) + V_1(n)s + V_2(n)s^2 + \dots + V_k(n)s^k + \dots$$

where
$$V_k(n) = \frac{J_k(n) - \sum_{i=1}^k V_{k-i}(n)Y_i(u)}{Y_0(n)}$$

GENERAL NODE CASE (continued...)

• The voltage moments can be computed at all nodes if equivalent Ys and Js have been propagated twice along each segment: once in each direction. Hence a linear time path tracing algorithm which traces each segment once in either direction can be used for the computation of voltage moments at all nodes.

COMPUTING TIME DOMAIN RESPONSE

• Use moment matching techniques

- We have V(s) for each node in the network
 2N moments for the node voltages have been computed
- Largest order of approximation can be N, let M=N-1
 Approximate V(s) with an M-zero N-pole expression
- Padé Approximation

 $\tilde{V}(s) = \frac{a'_0 + a'_1 s + a'_2 s^2 + \dots + a'_M s^M}{1 + b'_1 s + b'_2 s^2 + \dots + b'_N s^N}$

TIME DOMAIN (continued ..)

• The denominator coefficients are computed from the Hankel matrix

V_0	V_1	•••••	V_N	$\begin{bmatrix} b'_N \end{bmatrix}$	$\begin{bmatrix} V_{N+1} \end{bmatrix}$	
V_1	V_2		V_{N+1}	b' _{N-1}	<i>V</i> _{<i>N</i>+2}	
			•		=- :	
· ·	•	•••••	•	·	•	
V_N	V_{N+1}		V_{N+M-1}	b'1	$\left[V_{N+M}\right]$	
			$a'_0 = V_0$			
The	numer	ator coef	$a'_1 = V_1 + b'_1 V_0$			
are	comput	ed by eq				
pov	vers of s		$a'_{M} = V_{L} + \sum_{i=1}^{M} b'_{i} V_{M-i}$			

TIME DOMAIN (cont ...)

• Given the above symbolic coefficients, the time domain response can be found numerically by writing

$$\tilde{V}(s) = \hat{c} + \sum_{i=1}^{N} \frac{\hat{k}_i}{s - \hat{p}_i}$$

• which is transformed to the time domain as

$$\tilde{v}(t) = \hat{c}\delta(t) + \sum_{i=1}^{N} \hat{k}_i e^{\hat{p}_i t}$$

PRELIMINARY EXPERIMENTAL RESULTS

- Two randomly generated ground nets
 _ gnet1: 400 contact points
 gnet2: 4000 contact points
- total wire length=2cm
 total wire length=10cm

 wire width=3µ
 wire width=3µ

 • Accuracy was compared with HSPICE at four
- selected nodes A, B, C and D
- Comparing peak voltage and root mean square error
- Sample time points were 0.01ns
- Maximum order of the Padé Approximations was set to 3

PRELIMINARY EXPERIMENTAL RESULTS (continued)

• gnet1: Peak and RMSE Voltages

Node	Peak (Volts) Vdrop	Peak (Volts) HSPICE	V _{RMSE} (Volts)
A	0.350	0.342	0.00130
В	0.432	0.426	0.00150
С	0.688	0.689	0.00087
D	0.461	0.463	0.00054

• gnet2: Peak and RMSE Voltages

-		_			
Node	Peak (Volts)	Peak (Volts)	VRMSE		
	Vdrop	HSPICE	(Volts)		
A	0.216	0.229	0.00017		
В	0.225	0.243	0.00013		
С	0.419	0.419	0.00028		
D	0.129	0.125	0.00039		

CONCLUSIONS

- Expand the applications of symbolic analysis to a new field
- Application of symbolic analysis to Power and Ground interconnect analysis
- Provides mechanism for reducing cost of highly iterative process
- More testing of the algorithm in general and the symbolic role in particular is required
- Expand algorithm to perform P&G bus optimization, ie. produce an optimal P&G network based on the results