Table Look-up Based Compact Modeling for On-chip Interconnect Timing and Noise Analysis

Abstract

A compact model for RLC interconnect lines, in the form of a two-path hybrid ladder, is proposed for on-chip interconnect timing and noise analysis. The model parameters are synthesized through constrained nonlinear optimization to directly match the circuit response characteristics over a range of transition times and loads, both at the driving point and at the receiver end. The effect of capacitances on the return current distribution is explicitly considered in our work in obtaining the accurate responses for industrial circuits, and is found to have a significant effect. The parameters for this model are embedded in a table that is characterized once for a design and then used for the analysis of various structured interconnects. Compared with a prior compact modeling approach, our model is demonstrated to accurately predict responses such as the interconnect delay, gate delay, transition times at near and far ends of switching lines as well as the overshoot at the far ends of switching lines.

1. Introduction

On-chip inductance is a growing issue for high-performance circuits, and technology trends indicate that these effects will grow even more prominent in the future.

A commonly used inductance model is the PEEC model [1], which represents a complex multiconductor topology without predetermined current return paths. However, it results in a dense partial inductance matrix that makes simulation computationally expensive. Although the computational cost can be greatly decreased by sparsification techniques [2-6], the PEEC model is still computationally expensive for simulating large industrial circuits. Loop inductance is an alternative way to represent on-chip inductance system [7].

In this paper, we propose a computationally efficient compact model for fast and accurate on-chip interconnect timing and noise analysis, which is valid over a range of typical transition times. The technique utilizes a table look-up of model parameters which are characterized for different layout parameters, such as signal wire width, length, spacing to the nearest power/ground wires, shielding etc.. Parameters for layouts that do not directly correspond to a table entry are interpolated. We demonstrate the viability of our approach on a clock net built to industrial specifications.

When on-chip inductance is not important, a standard model for wire segments is the RC-π model that incorporates the loop resistance, which is dominated by the resistance of the wire segment. The loop inductance, calculated as the sum of the partial self and mutual inductance along a wire and its current return paths, can be introduced into this π model by connecting it in series with the loop resistance. Signals with different transition times τ have different frequency spectrum and will experience different loop electrical characteristics. The frequency dependency of the loop resistance and loop inductance arises primarily due to the proximity effect. As demonstrated in [8], the change in the loop resistance and inductance can be very large over a wife range of frequencies. Compared to its low-frequency value, the loop inductance decreases by about 50% at high frequencies, while the loop resistance increases monotonically as the frequency increases.

An RL ladder circuit, as shown in Figure 1(a), was proposed in [9] to approximate the frequency-dependent resistance and inductance due to the proximity and skin effects. This model was further developed in [8], as shown in Figure 1(b), to synthesize a layout-based hybrid ladder circuit. A shunt circuit of R_2 and L_2 in parallel with L_0 compensates for the additional reduction of the loop inductance at high frequencies. The model is synthesized in frequency domain by fitting input impedance. Specifically, the low-frequency inductance and resistance, the high-frequency inductance and the cross-over frequency (where $R=2p\ f_cL$) are calculated using an RL-only technique. The model parameters R_0, L_0, R_1, and L_1 are then calculated by forcing the low-frequency inductance and resistance, high-frequency inductance and the crossover frequency of the model to match the calculated values above. Next, R_2 and L_2 are obtained from the resistance and inductance of parallel plate return conductors.

This procedure has two limitations: first, in order to compute the loop inductance, it ignores the effect of capacitance on the return current distribution, thereby causing errors in the estimation of the frequency-dependent resistance and inductance. Second, it models the input impedance of the interconnect at the driving point, but not the transfer characteristics.

Our work overcomes both of these limitations and presents an extension of this hybrid ladder model to a two-path hybrid ladder model, using a different characterization technique. Specifically, the parameters are determined in time domain for a wide range of transition times and loads, through a constrained nonlinear optimization to match the response characteristics of the compact model, including the interconnect delay, the gate delay, the transition times at both the near and far ends of switching lines and the overshoot at the far ends of switching lines, to the exact response of the three-dimensional circuits under a comprehensive PEEC model, which includes the power grid decoupling capacitance and pad placements. Response characteristics are more directly related to the interconnect timing and noise analysis, accordingly time domain synthesis procedure gives higher accuracy. In addition, in time domain characterization capacitance effects on the estimation of current return paths could be considered. A comparison between the responses from the hybrid ladder model and the accurate response shows that hybrid ladder model could overestimate delay and overshoot by 100%.

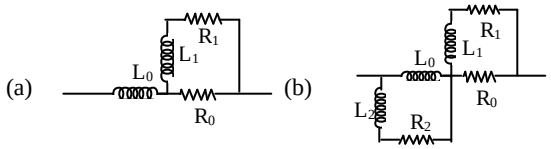

Figure 1: (a): The RL ladder circuit [9]. (b): The hybrid ladder model [8].

2. Two-path hybrid ladder model

A signal making a logic transition has a spectrum of frequencies. Current components corresponding to different frequencies choose different paths through the power grid and must be modeled correctly. We propose a compact model, a two-path hybrid ladder model as shown in Figure 2 (a), that is constructed to separate the paths through which the currents for different frequency components would flow. The path with R_0, L_0, R_3 and L_3, corresponds to the current flow for low-frequency components, and that with R_1, L_1, R_2 and L_2, represents the current flow for high-frequency components.

R_2 and L_2 form a branch to compensate for the change in the loop inductance at high frequencies, while R_3 and L_3 compensate for the change of the loop resistance at low frequencies.

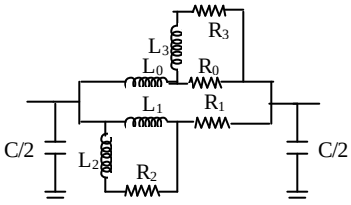

Figure 2: Two-path hybrid ladder model.

The intuition behind the approach may be explained as follows. The structure shown in Figure 1 (a) is known to be adequate for lower frequencies, and forms the upper path in Figure 2 (a). The structure in Figure 1 (b), attempts to perform high-frequency compensation through R_2 and L_2, but R_0 and L_0 are required to be involved in both the high-frequency and low-frequency behavior. We remove this constraint by creating the high-frequency path in parallel with the low-frequency path. In doing so, we use a larger number of parameters, which enables a better fit of the accurate response. At extremely high and low frequencies, both our model and hybrid ladder model behave similarly. At intermediate frequencies our approach provides a greater flexibility for a better fit.

At extremely high frequencies the two-path model is simplified to three parallel inductances L_0, L_1, and L_2, while at extremely low frequencies it is simplified to three parallel resistances R_0, R_1, and R_3, respectively. Note that the parameters R_2 and L_3 do not appear in either the high- or low-frequency reductions, so that they may be tuned to capture the circuit response at intermediate frequencies. The increased number of tunable parameters over hybrid ladder model is expected lead to a higher accuracy for a wide range of layout topologies and a range of frequencies.

3. Outline of the approach

Our approach is based on fitting parameters of our two-path hybrid ladder model by nonlinear optimization to match a set of desired characteristics of transient response from the compact model to that of the response from a comprehensive PEEC model, over the ranges of interest for the driver/receiver sizes and transition times. By performing this optimization for a variety of circuit topologies, representative structures are characterized and stored in a table. Subsequently, a compact model for a given structure may be interpreted by looking up entries in the table.

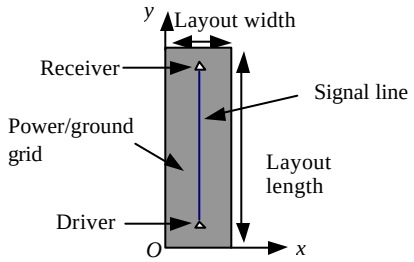

Figure 3: Top view of the layout of a four metal layer structure.

We study our approach applying to analyze the top level clock tree and signal lines routed on four metal layers, M6, M7, M8 and M9 in a nine-layer structure. The power/ground wires are distributed densely in the four layers. In order to accurately estimate the current return paths and inductance effects, a comprehensive PEEC model, described in [4], is used to determine the responses at the near and far ends of the switching wires. In addition to the interconnect net under consideration, the circuit model includes supply lines, drivers and receivers, vias, pads and intrinsic/explicit decoupling capacitances. The circuit in synthesis procedure, whose top view is shown in Figure 3, includes a switching wire with different wire lengths, widths and spacings to the nearest supply line, corresponding to different sets of model parameters in table. The layout width a chosen so that along the layout length, there are one row of pads on each side of the switching line.

Accurate transient response of this model is computed by our precise inductance analysis tool that uses precorrected-FFT technique [10] to accurately compute inductance effects, together with PRIMA algorithm building reduced order model of the circuit which is then simulated by SPICE.

It is desirable for the compact model to be independent of the gate parameters, so that it can be utilized under any value of the loads and input transition time. The response of a switching line is impacted by the driver size, the receiver size and the transition time at the near end. However, for a given line, only any two of these three parameters are independent. Here, we choose the receiver sizes and the transition times at the near end of the switching line as the independent parameters. For a given receiver size and a given transition time at the near end, the driver size can be calculated to produce the given transition time at the near end for the given receiver size. Let the ranges of interest for the receiver sizes and transition times consist, respectively, of the sets of discrete points:

$$\textit{Receiver sizes: } W = \{w_1, w_2, \ldots, w_m\}$$
$$\textit{Transition times: } S = \{s_1, s_2, \ldots, s_n\}$$

Thus, the compact model is required to be accurate over all mn combinations of the above parameters.

The compact model is constructed to capture the transient response characteristics of the line. Specifically, we match five response characteristics: the gate delay (from the input to the output of driver), interconnect delay (from the output of driver to the input of receiver), transition time at the near and far ends of the switching line and the peak overshoot at the far end for a transition. For a given interconnect topology with $p=mn$ distinct combinations of receiver sizes and transient times, there will therefore be $5p$ responses which should be matched. However in our work, we choose $p=4$, which corresponds to four combinations of heaviest/lightest receiver sizes and highest/lowest transition times, using constrained nonlinear optimization. The experimental results show that matching the response characteristics for these four circuits will automatically match for the mn circuits. The formulation of the non-linear optimization problems for the set of four objective circuits with *20* response characteristics:

minimize Relative error of *20* response characteristics

subject to all model parameters ≥ 0

We transform the multi-objective optimization problem to a single objective function through a weighted minmax objective. Specifically, the error is calculated as a weighted maximum of the percentage errors in all *20* response characteristics. In practice, we choose the weights to emphasize low errors in delay and overshoot. Thus, in summary, each model synthesis procedure involves a first step of simulating the objective circuits for accurate responses, followed by a second step of fitting the parameter values to the compact model through constrained nonlinear optimization. These model parameters are then put in a table.

Since a real layout consists of a large number of parameters, such as the number of switching lines, the metal layers the switching

lines are on, the width, length, spacing of these switching lines, the spacing between the switching lines to the nearest power/ground grid lines or shields, width and spacing of power/ground grid lines, the width of shields, the spacing between the shields and the nearest grid lines and the pad positions. Obviously it is impossible to build simple practical model and manageable table size to capture the effect of all these parameters, therefore we have selected through the experimentation only the most significant. The model is thus simplified by the following:

1. For now, we focus our attention to building a model for one switching line, such as a signal line or clock net. This restriction still yields useful solutions to important problems (for example, to a critical signal line, or a clock network structure). The line may be parameterized by factors such as its width, its length, its distance to the nearest supply line, whether it is shielded or not, etc.
2. For a reasonable design, even significant changes in the structure of the power grid do not noticeably influence the response characteristics of the logic. It has been demonstrated in [11] that a small deviation from the regular power/ground topology will not cause a significant change in the response characteristics. We utilize this fact to work with a representative power grid, under the assurance that to the first order, our model will remain reasonable even if the actual grid is perturbed from the assumptions under which our characterizations are performed. A high level structure for the regular power grid and regular pad locations is provided for characterization, including parameters such as the pitches and widths of power lines and pad spacings. Once the spacing from a signal line or shield to the nearest power/ground lines is given, the power/ground environment for that signal line is well determined. Our approach requires a single characterization step for each design using a model for the power grid.

With this simplified approach, each entry of the table corresponds to a set of values of the following parameters:

1. Metal layer on which the signal line lies.
2. Width of the switching lines.
3. Length of switching lines.
4. Distance to the nearest supply grid line.
5. Shielded and unshielded cases.

4. Experimental results

A multidimensional table was constructed for a 0.18µm technology, with 0.36 µm minimum line width and spacing. The transition times were measured from 10%-to-90% of V_{dd}. The ranges of the receiver sizes and transition times were set to be:

W = {15, 30, 90, 150, 210, 270, 330, 390} µm, and
S = {1000, 800, 600, 400, 200, 100, 80, 60} ps,

respectively. Each switching line was modeled by a cascade of two-path hybrid ladder models. The characterization was done on four circuits with receiver sizes of *15/390* µm and transition times of *1000/60* ps. The model was tested on all 64 combinations of W and S above, and the accuracy results are summarized in Table 1. In addition to the high accuracy, two-path ladder model also gives a high speed. The simulation time for each circuit in Section 4.1 in PEEC model is 16 mins, while it is reduced to seconds with the two-path ladder model.

4.1. Accuracy of the responses for signal lines

A set of experiments is carried out to test the accuracy of the responses of signal lines. The layout structure of this set of experiments is shown in Figure 3. Experiments are performed on various lengths of signal lines: 300 µm, 600 µm, 900 µm, 1200 µm, 1500 µm and 1800 µm, corresponding to six circuits S_{300}, S_{600}, S_{900}, S_{1200}, S_{1500} and S_{1800} respectively. Each circuit is modeled by a cascade of three two-path hybrid ladder model segments.

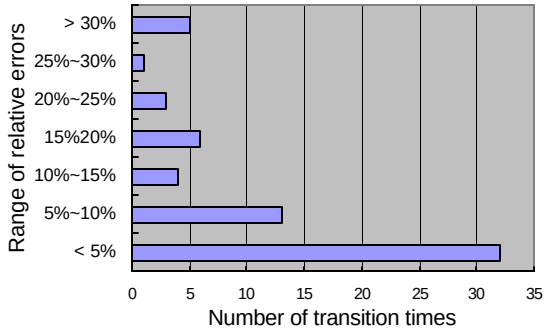

Figure 4: A histogram showing the distribution of errors in the far end transition time for the 64 combinations of W and S for circuit S_{900}. For example, the bar labeled "1" corresponds to the fact that 32 of the 64 combinations showed errors of < 5%.

For all six circuits, all the five critical response characteristics are matched well. For example, although the maximum error for interconnect delay can reach 11% for the six circuits, the average value is between 2% and 5%. Even the worst-case errors are acceptable in some cases for the accuracy requirements in current timing analysis tools. For the circuit S_{900}, a histogram of the distribution of the transition times at the far end for the 64 possible combinations of W and S are shown in Figure 4, and are seen to be acceptable.

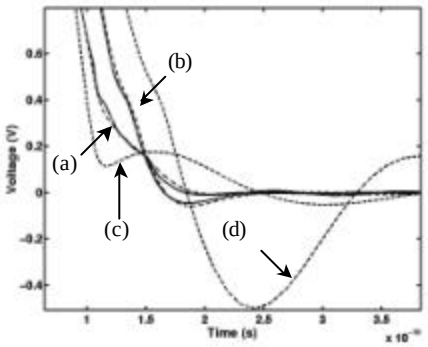

Figure 5: Comparison of the responses from the two-path ladder model, the hybrid ladder model and the PEEC model. (a) near end response under the accurate model and our two-path model (almost identical). (b) far end response under the accurate model and our two-path model (almost identical). (c) near end and (d) far end response for the hybrid ladder model.

A comparison between the accuracy of the two-path ladder model and the hybrid ladder model [8] was also carried out. Figure 5 includes the responses from both of these models, as well as the accurate responses using the full inductance matrix, for the circuit S_{900} under an 80ps input transition time to the driver and 150µm receiver size. The responses from the two-path model are almost indistinguishable from the accurate response, while the responses from hybrid ladder model are seen to overestimate the inductance effects. The interconnect delay error could reach 100%. The error in overshoot is even larger.

4.2. Accuracy of the responses for a clock net

Experiments are carried out to test the accuracy of two clock nets that have multiple switching line segments with non-uniform width, non-uniform spacing to the nearest power/ground grid lines and are on different metal layers. Circuit CLK_H, as shown in Figure 6, is a clock H-tree with one source and sixteen sinks. There are 31 line segments distributed on three metal layers M6, M7 and M8. The responses are measured at the output of the source and the input of the sink at node C, while the sizes of the other sinks are identical and are set to be 100 μm or 900 μm. The length of the path from the source to sink at C is 3900 μm with five line segments that are modeled by fifteen model segments on this path. Circuit CLK_{HBF} is an optimized version of circuit CLK_H with buffers inserted at all nodes marked *D* and *E*.

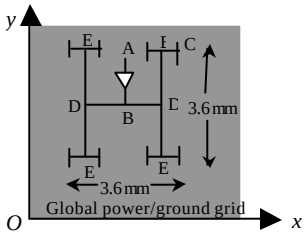

Figure 6: Top views of the structures of circuits CLK_H and CLK_{HBF}. (A: driver input, B: driver output, C: receiver input, D and E: buffer position in circuit CLK_{HBF}.)

The maximum and mean errors of timing characteristics for circuit CLK_H with 900 μm receiver sizes at all sinks except the one at C are 15% and 4%, while those for circuit CLK_{HBF} with the same sink sizes are 11% and 2% respectively. The overshoots in both the circuits are smaller than 50 mV. It is reasonable that the errors for circuit CLK_{HBF} are smaller than those for circuit CL_{KH} because the buffers are intended to reduce the inductance effects and this also has the side effect of making the modeling easier and more accurate.

5. Conclusion

A two-path ladder model for compact modeling of on-chip interconnect timing and noise analysis is proposed in this paper to accurately approximate the proximity effect in high speed circuits. The paths for both the high and low frequency currents are explicitly included in the model. The synthesis procedure uses constrained nonlinear optimization to match the response characteristics of the model to those under an accurate simulation, with comprehensive PEEC model and the effects of capacitances on the current return path estimation. A comparison with the hybrid ladder modeling shows that the proposed modeling results in more accurate responses. Extensive experiments on single signal lines and clock nets demonstrate that the proposed table look-up based compact modeling is a highly accurate and fast approach for on-chip interconnect timing and noise analysis in large circuits. In future work, we expect to extend this work to multiple-line buses.

References:

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Table 1: Mean and maximum relative errors for all the response characteristics in a set of test circuits.

Circuit	Relative error of Interconnect delay		Relative error of Gate delay		Relative error of Transition time at the far end		Relative error of Transition time at the near end		Relative error of >50mV overshoot at the far end	
	mean	max	mean	max	mean	max	mean	max	mean	max
S_{300}	2.5%	9.3%	1.2%	3.4%	2.3%	8.1%	2.0%	5.0%	15%	30%
S_{600}	3.5%	10%	0.7%	1.3%	2.6%	7.2%	2.5%	7.0%	10%	21%
S_{900}	2.3%	10%	0.9%	1.3%	3.3%	6.9%	3.5%	6.9%	12%	25%
S_{1200}	3.4%	11%	1.6%	2.6%	4.0%	8.5%	2.3%	7.2%	11%	35%
S_{1500}	4.0%	9.6%	1.1%	3.1%	3.7%	7.9%	3.6%	6.3%	10%	20%
S_{1800}	4.2%	8.6%	1.5%	3.6%	5.0%	10%	3.4%	8.0%	11%	30%
CLK_H	4.1%	5.6%	0.7%	2.6%	2.1%	5.7%	4.0%	15%	-	-
CLK_{HBF}	1.2%	4.0%	1.2%	4.2%	2.5%	11%	3.3%	5.8%	-	-

"-" implies that there was no overshoot for this case