Incorporating the Role of Stress on Electromigration in Power Grids with Via Arrays*

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ABSTRACT

Modern power grids use via arrays to connect wires across metal layers. These arrays are susceptible to electromigration (EM), which creates voids under the vias, potentially causing circuit malfunction. We combine the effect of via redundancy with models that characterize the effect of via array geometry on thermomechanical stress, and determine how the choice of via arrays can affect EM-induced failure in a power grid based on IR-drop threshold based failure criteria.

KEYWORDS

Electromigration, IR drop, power grid, redundancy, thermomechanical stress, via array

1 INTRODUCTION

In modern copper dual damascene (Cu DD) interconnects, interconnect failure times due to electromigration (EM) can vary significantly due to the sensitivity of EM to various parameters [1]. Although recent efforts have addressed the impact of process variations and EM physics [2, 3], the role of layout-dependent interconnect stress has not been adequately modeled. Most works on EM explicitly or implicitly model power grids vias as single-via structures that span the width of the wire. However, metal lines in the power grid may use wires as wide as 2–3μm, and interconnections between metal layers almost always involve an array of vias instead of a single via. These via arrays have complex geometrical and electrical characteristics that can affect EM. Preliminary work on examining via array structures has been performed in [4], which addresses redundancy and current crowding in via arrays, and [5], which performs a stress-EM analysis on a small 2×1 via array to determine the time-to-failure (TTF) under accelerated stress. However, at chip operating conditions, the impact of thermomechanical stress on circuit performance in addition to the redundancy and current crowding factors has not been adequately addressed. This is the focus of our work.

Today, circuit designers typically guard against EM by comparing current densities against a foundry-specified limit for a process technology. This limit is characterized through experiments on interconnect test structures, stressed at elevated temperature (typically 300°C [6]) and voltage values, to induce EM failure. The failure times are then mapped back to normal chip operating conditions [1]. While such experiments have been widely used to characterize EM in Cu DD interconnects, they fail to capture the effect of thermomechanical stress, generated due to a mismatch in the coefficient of thermal expansion (CTE) of the metallization and the surrounding dielectric [7]. The CTE differential results in compressive/tensile stresses when the wafer is annealed from high-temperature ($300 - 350$°C) manufacturing conditions to normal operating temperatures. This stress can greatly influence EM in normal conditions, but may be negligible at characterization [6] since the elevated temperature conditions used during characterization are closer to those at manufacturing.

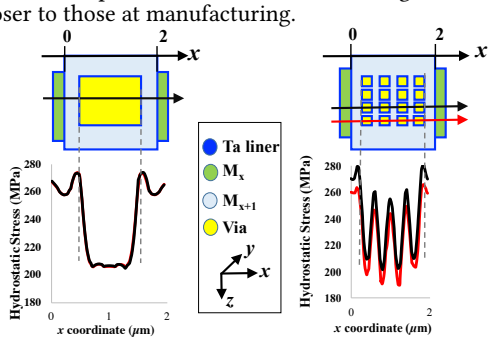

Figure 1: A 1×1 and 4×4 via array (top) and the hydrostatic stress along the wire beneath the via (bottom)

Thermomechanical stress is a function of the layout and the composition of the surrounding layers. Figure 1 shows two via configurations, corresponding to a single (1×1) via and a 4×4 via array. The vias connect an upper level of metal M_{x+1} with the next lower level, M_x, and the metal layer heights correspond to M7 and M8 in 32nm technology node [8]. The wire widths are chosen as 2μm for the interconnects, and are representative of wires in a power grid. Both vias have an effective area of 1μm^2, corresponding to the same resistance between M_x and M_{x+1}.

We plot the hydrostatic stress on the lower metal layer M_x, along a horizontal slice across each via, in the direction of the arrow through the via(s) as shown in the figure. The stress along the black [red] arrows through the 4×4 via array is displayed in the stress plots using black [red] line. The *local minima* of stress occur in the interior of each via. In the 4×4 array, the *local maxima* occur in the regions between the vias. The stress profile is different between the 1×1 and 4×4 scenarios, and although the largest stress in the 4×4 array is similar to the largest value for the single via, the inner vias of the former see lower stresses. It can be shown that this stress difference translates to a lifetime improvement of ~2 years for each inner via in the 4×4 array.

Current-induced EM stress adds to this stress value, and voids are formed when the net stress reaches a threshold value [6, 9]. The

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lower preexisting thermomechanical stress values in the inner vias results in a lower thermodynamic feasibility to achieve the critical threshold value needed for void formation. Additionally, for the 4×4 via array, even if a void does form, its impact is mitigated by the fact that the via array has more redundancy than a single via. Together, these factors imply that the choice of a via array can alter interconnect lifetimes. The change in interconnect lifetime affects the electrical characteristics of the power grid [2]: each wire failure perturbs the power grid, and after a sufficient number of failures, the power grid may no longer meet its IR-drop specifications.

This work models the layout-dependent impact of thermomechanical stress on via arrays in power grids into a physics-based EM failure model. We build an EM analysis methodology based on via characterization, and compute the reliability of power grids by incorporating via redundancy.

2 EM IN CU INTERCONNECTS

2.1 Interconnect structure and TTF modeling

The schematic in Figure 2 illustrates the dual-damascene interconnect structure used in modern integrated-circuits. The interconnect is made up of copper and is cladded with Ta barrier layer on the sides and bottom. The top surface is bounded by the Si_3N_4 capping layer, while the inter layer dielectric (ILD), made of low-k material, such as SiCOH lies between the copper lines. The whole structure rests on a silicon substrate a few hundreds of microns thick.

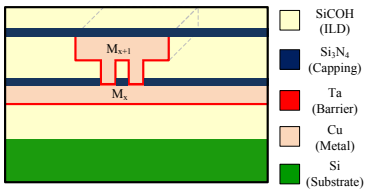


Figure 2: Schematic of Cu DD structure simulated in FEA

EM failures in Cu DD vias occur through the nucleation and growth of voids. For vias, experimental works have reported slit-like voids that result in early failure, characterized by rapid wire resistance increase [10]. The TTF for slit voids in Cu interconnects can be modeled by the nucleation time, t_n, defined as the time at which the void under a via nucleates. For previous Al based technologies, the TTF was typically represented as the sum of the nucleation time and the time elapsed for the void to grow to a catastrophic size [9]. However, for recent Cu based technologies, early nucleation due to slit like voids is observed [10]. In such cases, the TTF is dominated by the nucleation time since the void growth leading to an open circuit for these slit voids is rapid, and the void growth stage can be neglected, resulting in a quite accurate estimate of the TTF. Using the model from [9], the nucleation time is given by:

$$\text{TTF} \approx t_n = \begin{cases} \frac{(\psi_C - \psi_T)^2 C_{t_n}}{D_{eff}} & \text{when } \psi_C > \psi_T \\ 0 & \text{when } \psi_C < \psi_T \end{cases} \quad (1)$$

$$D_{eff} = D_0 \exp\left(-E_a / k_B T\right) \quad (2)$$

$$C_{t_n} = \frac{\pi}{4}\left[\frac{\Omega k_B T}{(e Z^{\star}_{eff} \rho_{Cu}\, j)^2 B}\right] \quad (3)$$

Here, ψ_C is the critical stress for void nucleation; ψ_T is a term that accounts for the thermomechanical stress and package stress in the wire; C_{t_n} is a constant that is dependent on properties of the Cu DD metallization; D_0 is the EM diffusivity constant; E_a is the effective activation energy for EM; Ω is the atomic volume; k_B is Boltzmann's constant; T is the temperature; e is the elementary charge on an electron; $Z^{\star}_{eff}$ is the effective charge number; ρ_{Cu} is the resistivity of copper and j is the current density in the wire; B is the bulk modulus for the Cu-dielectric system.

The nucleation time is related to $(\psi_C - \psi_T)^2/D_{eff}$, where $(\psi_C - \psi_T)$ is the *effective critical stress*, the threshold after which a void nucleates. As we will show, ψ_C is a lognormal, and so is D_{eff} [2]. Using these facts, simple algebra can be used to show that ***the TTF can be well approximated as a lognormal*** using Wilkinson's approximation. The proof and details are omitted due to space limitations.

2.2 The role of critical stress, ψ_C

Voids nucleate under vias due to the presence of circular flaws at the copper bulk and Si_3N_4 capping layer interface layer, as shown in Figure 2 [11]. The magnified illustration of this interface is shown in Figure 3. In the flaw region, the capping layer does not adhere to the copper metal: such a situation can occur during the Cu DD process as a result of a surface defect or contamination during manufacturing.

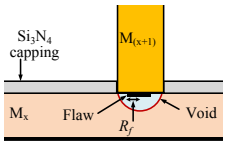


Figure 3: Cross-section of Cu DD interconnect showing a circular flaw of radius R_f leading to void

As the stress in the wire increases due to the combination of EM-induced atomic depletion combined with preexisting thermomechanical stress, the nucleation of a small void embryo at the flaw location becomes theromodynamically feasible. When the net tensile stress in the line crosses the critical stress value, void nucleation becomes feasible. The critical stress value required to achieve this is [11]:

$$\psi_C = \frac{2\gamma_s \sin\theta_C}{R_f} \quad (4)$$

where γ_s is the surface free energy for copper, θ_C is the contact angle, defined as the angle which the tangent to the void makes from the horizontal capping surface, chosen as 90° for the circular flaw; R_f is radius of the circular patch described previously and shown in Figure 3. For a power grid, which consists of millions of wires, the flaw size may vary across the large number of wires [12], leading to a variation in critical stress according to (4). We use a lognormal distribution for the flaw size, consistent with the fact that the TTF for slit voids is experimentally seen to be lognormally distributed [1]. The mean value of R_f is set to 10nm [12], and its standard deviation 5% of the mean value. Thus, ψ_C, which is the reciprocal of R_f is lognormally distributed, and it is easy to verify that it can vary by as much as 100 MPa.

2.3 The role of thermomechanical stress, ψ_T

We determine the magnitude of the thermomechanical stress, ψ_T, using a model that is built from exact finite element analysis (FEA) that precharacterizes typical Cu DD layout structures encountered in power grids. We construct the Cu DD structure shown in Figure 2 to perform FEA simulations, using the ABAQUS [13] FEA package, to evaluate local thermomechanical stress distributions.

As stated earlier, the multi-level Cu DD interconnect structure is fabricated at a high temperature of 300–350°C [6], while metal interconnects in ICs typically operate at 100–105°C in the worst-case. Thus, after manufacturing, due to the CTE mismatch between the materials, thermomechanical tensile stress develops inside the interconnects and the vias. Due to the close proximity of thermally

mismatched materials, the magnitudes of stress depend upon the geometry and the material properties of the interconnect and the surrounding structure. The material parameters used for thermo-mechanical stress computations are shown in Table 1.

Structure	Material	Young's modulus E(GPa)	Poisson's ratio ν	CTE (ppm/°C)
Substrate	Silicon	162.0	0.28	3.05
Bulk	Copper	111.6	0.34	17.7
ILD	SiCOH	16.2	0.27	12
Barrier	Ta	185.7	0.342	6.5
Capping	Si_3N_4	222.8	0.27	3.2

Table 1: Mechanical properties of materials in Cu DD

One source of thermomechanical stress in interconnects is the CTE mismatch of the structural materials used for Cu DD manufacturing. This component is local in nature and depends purely on interconnect geometry. A second component is attributable to the CTE mismatch between underfill, package bump, and the silicon chip causes stresses to develop in the interconnect layers. This stress depends on the relative location of the interconnect and packaging connections and is independent of interconnect geometries. We treat the package stress as an input to the method.

The thermomechanical stresses that modulate the tensile and compressive stresses in the line during EM are computed using the techniques in Section 3. For EM, the hydrostatic stress, $\psi_H = \frac{\psi_{xx}+\psi_{yy}+\psi_{zz}}{3}$, is of interest [9], where ψ_{xx}, ψ_{yy}, and ψ_{zz} are the normal stress components along the Cartesian coordinates. Our FEA simulations evaluate these components and compute the hydrostatic stress. From (1), the shortest TTF corresponds to the point of maximum thermomechanical stress, i.e., vias nucleate in regions of maximum stress. For each individual via, the thermomechanical stress is thus taken to be the peak value in the via.

3 ESTIMATING ψ_T IN A POWER GRID

We accurately account for the stress-related parameters responsible for EM in via arrays. Since it is prohibitively expensive to run FEA simulations on a full power grid, we propose a methodology that characterizes thermomechanical stress by performing FEA on smaller primitives that correspond to common via array configurations. For each pattern, for different wire widths, we store the peak tensile thermomechanical stress values underneath the vias.

3.1 Typical topologies in power grid

In upper levels of layouts (where via arrays are used), power grid networks have a two-dimensional mesh structure, where horizontal and vertical metal layers run in long stripes. Via arrays are placed at the intersections of the mesh, connecting horizontal and vertical wires. The interconnects at the edges of the mesh boundaries have a larger volume of adjacent ILD than those within the boundary, and experience different levels of thermomechanical stress.

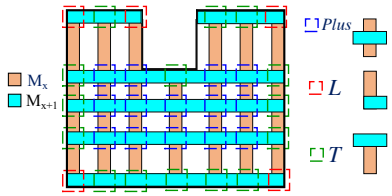


Figure 4: Typical intersection patterns observed in power grid

Figure 4 illustrates an example 2D power grid mesh. Adjacent via arrays are far away and do not influence each other, and we consider three patterns shown in the figure:

- *Plus-shaped* patterns inside the mesh boundary,
- *T-shaped* patterns at the edges of the mesh, and
- *L-shaped* patterns at the corners of the mesh.

We perform our analysis for pairs of adjacent layers since we experimentally observe that the stress at the base of a via connecting two metal layers is unaffected by a third metal layer (results omitted due to space limitations).

3.2 Characterizing ψ_T

As indicated in Figure 1, the use of single vias or via arrays of different dimensions affects the thermomechanical stress, ψ_T, and therefore impacts the TTF of the via according to (3). Therefore, for accurate TTF characterization, the appropriate stress value, as a function of the via configuration should be used. Additionally, in the upper layers of the power distribution interconnects, which typically carry the most current and are most susceptible to EM, the typical wire width is significantly larger than the minimum feature size allowed in a technology. Although interconnect thickness for a specific metal layer is fixed for a given technology, the wire width and the pitch could be design-dependent.

We characterize via structures connecting intermediate and top metal layers (frequently occurring in power grids). The total number of characterizations must cover:

- M_x and M_{x+1} pairs, where x and x+1 may be either intermediate or top layers (3 combinations: intermediate–intermediate, intermediate–top, and top–top)
- *Plus-*, *T-*, and *L-shaped* patterns (3 combinations)
- The number of possible via configurations, v_n
- The number of wire widths, w_n

Note that it is sufficient to consider x and x+1 to be intermediate and top layers: as shown in [14], several layers have the same thickness and these combinations could cover the top 5 metal layers, which use thick wires with via arrays.

The number of FEA simulations required to cover all via configuration is thus $9 \times w_n \times v_n$. The cost of these simulations is reasonable since they are performed *only once* for a process technology, similar to standard cell characterization. For power grids, which are mostly regular mesh structures, the wire widths are observed to have a small set of values, which implies a small value for w_n. However, in the general case, when the spread of wire width values is significant, we limit $w_n = 3$ and perform FEA only on a subset of wire width values, and we use interpolation to evaluate the stress at intermediate values of width, for computational efficiency.

Note that since the TTF scales with the current, it is adequate to characterize the TTF for a reference current value. For any other current, the TTF can be scaled using (3).

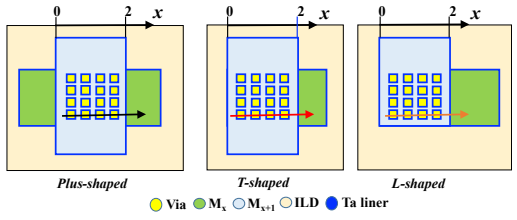


Figure 5: FEA model snapshot of the *plus-shaped* (left), *T-shaped* (centre), and *L-shaped* (right) structure simulated using ABAQUS

Figure 5 shows the schematic of our FEA model for the three intersection patterns. For the *plus-shaped* pattern on the left side, the interconnects run continuously on both sides of the via array location as shown in the figure. In contrast, for the *T-shaped*

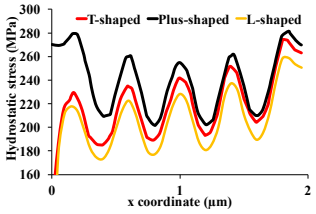


Figure 6: Thermal stress, ψ_T, for various intersection patterns, corresponding to a 4×4 via array (as shown in Figure 5)

(centre) and *L-shaped* (right) patterns have at least one metal layer terminating at the via intersection (near the boundary of the chip). This information is captured by invoking appropriate boundary conditions in FEA. Stress magnitudes can vary between the three types of patterns owing to the difference in the surrounding materials, such as ILD. Figure 6 shows the thermomechanical stress under the first row of vias (indicated by the arrows in Figure 5) in the M_x metal layer of a 4×4 via array.

Observing the stress values, it is evident that even identical via array configurations experience different stresses in these three cases due to disparities in the volume and location of surrounding material such as the ILD. Note that the value of the stress is attenuated for the *T-shaped* and the *L-shaped* structure. This can be attributed to a larger CTE for Cu relative to ILD. The presence of more ILD near the via, which increases the magnitude of CTE mismatch, making it easier for Cu to deform (contract) in these patterns. In contrast, the *Plus-shaped* structure, is surrounded by *Plus-shaped* structures on all the four sides, making deformation of Cu difficult, thereby resulting in more stress.

Today's technologies allow large via arrays in the upper metal layers. We analyze the stress distribution for an 8×8 via array, with the same effective cross section area as 4×4 via array. Figure 7 shows the two via arrays and the thermomechanical stress for each case. Using the arrow notation of Figure 1, we show the stress through each via, along an arrow using a curve of an identical color as the arrow, as a function of distance $\boldsymbol{x}$.

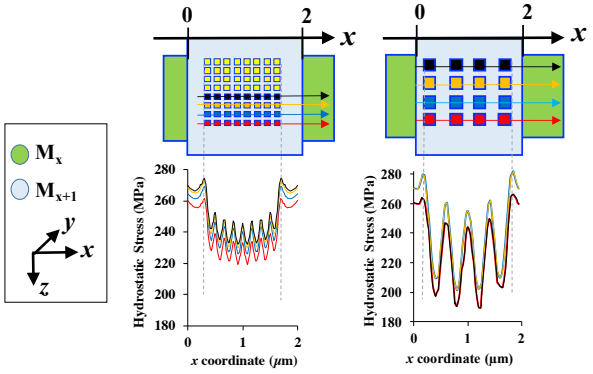


Figure 7: FEA simulation 8×8 vs. 4×4 via array

The vias at the perimeter of the 4×4 and 8×8 arrays see similar peak thermomechanical stress, but for each row, internal vias in the 8×8 experience a significantly different stress from the 4×4 via array. In general, internal vias in the 8×8 array experience smaller peak stress compared to the 4×4 via array. This can be attributed to the reduced volume of ILD between vias as well as the reduced via volume in the former case. The mismatch in the thermal contraction for the reduced volumes has a smaller impact on the stress, and therefore the stress fluctuations are lower for the 8×8 via array. Under the smaller peak stress, Eq. (1) implies a larger TTF. This is explicitly quantified in Fig. 9 in Section 5.

4 CIRCUIT IMPACT OF VIA ARRAYS

In contrast with the prior art, where the vias are "lumped" as a single component during power grid analysis [2, 3], we attempt to capture the impact of redundancy. We see redundancy at two levels: *via array redundancy*, where multiple vias are placed together in the array, and the failure of one does not imply the failure of the array, and *power grid redundancy*, where via arrays are placed redundantly in the grid. At the power grid level, the failure of one via array may not imply system failure under an IR drop failure criterion. We present an approach that hierarchically analyzes the impact of failures in via arrays on the performance of a circuit. As mentioned earlier, unlike a lumped 1×1 via, a via array has some inherent redundancy: the failure of a single via does not cause the entire array to fail, but increases its resistance. Complete failure occurs only when all vias fail. Within a power grid, the failure in a via array will cause an increase in the IR drop, and system failure is deemed to occur when the IR drop crosses a designer-specified threshold.

Algorithm 1 Monte Carlo simulation for redundant system [15]

For step 1, System: via array; Component: via
For step 2, System: power grid; Component: via array
Input: System netlist, component TTF distribution.
Output: Cumulative distribution function (CDF) of TTF for the system.
Perform system SPICE simulation at $t = 0$, obtain the current in each component.
while #MC_simulations $< N_{trials}$ **do**
  Generate random TTF sample for every component.
  Order the components based on the TTF.
  EM void forms on component with lowest TTF: C_{min}
  Change the resistance of C_{min}
  while system performance $<$ failure criterion **do**
    Recalculate new current flow, TTF for components.
    Order the component based on the TTF.
    EM void on component with least TTF: C_{min}.
    Change the resistance of C_{min}.
  end while
  Report circuit TTF
end while
Generate circuit CDF

Our approach to solving this problem consists of two parts. First, we characterize each via array for its TTF, taking into account the fact that individual vias may have different TTF values based on the thermomechanical stress. Next, we determine the TTF of the entire circuit, using the TTF models for individual via arrays.

In our framework, we separate via array failure from the power grid failure, and perform our analysis in a hierarchical manner, in two steps. First, we characterize the TTF for the via array reliability, incorporating the impact of variation in thermomechanical stress and redundancy due to the presence of multiple vias. The via array characterization process can be considered as analogous to the standard cell characterization, as it is performed only once for a given technology. Next, we use the via array reliability characterization to determine the TTF of the power grid.

For both steps described above, we utilize a core simulation framework summarized in Algorithm 1 in terms of a generic component that could fail within a redundant system [15]. For the first step of the via array characterization, the vias correspond to components in a via array system, while for the second step of power grid analysis, the components correspond to via arrays in a power grid system.

The approach performs Monte Carlo simulations by generating a TTF sample for all components based on the underlying distribution. By rank-ordering the TTF, the order of failure in a specific

part is known. Each of these components is allowed to fail one by one until the system failure criterion is breached. At that point, the circuit TTF corresponds to the failure time of the last component that caused system failure. If the system continues to function, then the currents are redistributed from the failed component to the functioning components, and the process is repeated. Note that as successive vias fail, the current in other vias increases, potentially reducing the TTF of the remaining vias.

For a via array, we frame the system failure criterion in terms of the allowed percentage resistance shift for the via array. This parameter can be designer-specified. If n_F out of n vias in an array fail, then the resistance increase, ΔR, as a fraction of the nominal resistance, R, is obtained as

$$\frac{\Delta R}{R} = \frac{n_F}{n - n_F} \tag{5}$$

For a 4×4 via ($n = 16$), the failure of one via ($n_F = 1$) results in a 6.7% resistance change, and the failure of eight vias will result in a 100% increase. At a user-specified resistance increase, the via is deemed to have failed.

5 CIRCUIT RELIABILITY ANALYSIS OF POWER GRIDS

We apply our framework to analyze the circuit performance impact on industrial power grid benchmark circuits from [16]. We present our findings with respect the circuit reliability of the power grid system consisting of via arrays.

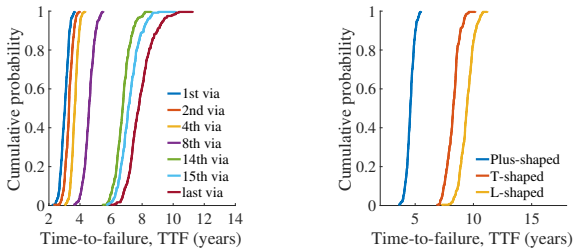
5.1 Via array TTF characterization

Precharacterization of various via topologies is a one-time step for each technology, and is based on stress simulations performed using the ABAQUS [13] FEA engine. For each topology, given a set of material parameters, the thermomechanical stress is determined. This information is passed to the redundancy calculations described in Section 4, which are then used to calculate the distribution for TTF corresponding to the via configuration and the via array failure criterion, specified as the percentage resistance change.

We perform statistical simulations to characterize the reliability of via array under various failure criteria represented by the number of vias allowed to fail, n_F. Based on Algorithm 1, we perform a Monte Carlo analysis to model sequential failures up to the specified failure criterion, n_F.

We illustrate the characterization process using the example of a *Plus-shaped*, 4×4 via array in Figure 1. The 16 vias in via array jointly conduct a total current density of $1{\times}10^{10}$A/m^2. We plot the distribution of TTF of the via array, at an operating temperature of 105°C. Figure 8(a) shows the CDF of the failure time, TTF, corresponding to different failure criteria based on the number of vias failing. For initial via failures, which corresponds to a small value of n_F relative to n, the resistance barely changes. Under such a scenario, it is likely that the power grid that contains the via array may not be significantly impacted, since the power grid structure is also redundant, and thereby EM-resilient [2]. Therefore, in practice, a via array failure criterion corresponding to small value of n_F may not be necessary and in practice, a larger value for n_F may be chosen.

Figure 8(b) shows the TTF obtained from the via array characterization, corresponding to the three intersection patterns, corresponding to a via array failure criterion of eight vias ($n_F = 8$). From the figure, we can observe that the reliability of the via array corresponding to *L-shaped* and *T-shaped* patterns is better than the case corresponding to the *Plus-shaped*. This is a direct consequence of the difference in the thermomechanical stress experienced in these intersection patterns, as discussed in Section 3.1.



(a) CDF of the TTF for various via array failure criterion corresponding to *plus-shaped* pattern

(b) CDF of the TTF for the three intersection patterns corresponding to 8th via failure

Figure 8: Failure scenarios in a 4×4 via array

Next, we quantify the impact of via redundancy by comparing the failure time corresponding to 4×4 and 8×8 via array with that of a single wide 1×1 via, under similar conditions of current stress. The results are shown in Figure 9 compares the TTF for the three via arrays, corresponding to the open-circuit failure criterion, $R_{\text{via array}} = \infty$, when all vias in the array fail, and for the criterion, $R_{\text{via array}} = 2\times$, where half the vias in the array fail. Under each criterion, the performance of 1×1 via array is the worst, followed by the 4×4 and then the 8×8 via arrays. The differences due to redundancy are magnified by the reduction in thermomechanical stress as we go from 1×1 to 8×8.

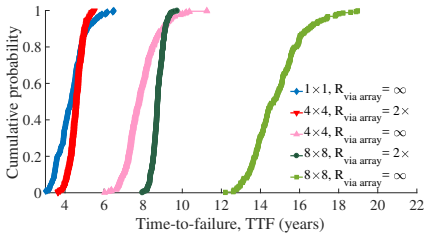


Figure 9: TTF comparison: 1×1, 4×4, and 8×8 via arrays

For the failure criterion corresponding to $R_{\text{via array}} = 2\times$, we observe that the worst-case TTF value (0.3%ile point) is about 8 years for the 8×8 via array, which is significantly better than the corresponding value of 4 years for the 4×4 via array, and also better than the TTF value of 6 years corresponding to the more relaxed failure criterion of $R_{\text{via array}} = \infty$ for the 4×4 array.

This precharacterized data, based on a fixed failure criterion for a given via array size and geometry (e.g., plus-, L-, or T-shaped) is to be passed on to the power grid TTF analysis framework. To enable this analysis, the TTF of the via array is fitted to a two-parameter lognormal distribution that is sampled during power grid TTF analysis.

5.2 Power grid TTF analysis

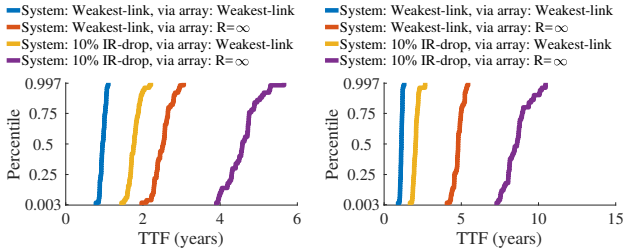
The analysis of the power grid TTF is performed for benchmark power grid circuits, stored as SPICE netlists [16]. The configuration for each via, e.g., 4×4 or 8×8, is specified at this stage. In this work, we select one configuration for a given power grid and use this configuration for all the via arrays in the power grid. This enables the performance comparison as a function of a given via array configuration. In practice, a combination of the via array configuration can be used. We do not use large 1×1 single vias as these are not observed in realistic process technologies.

The netlist and the output of the TTF characterization corresponding to the selected via array configuration is transferred on to the MC circuit simulation framework summarized in Algorithm 1.

The number of iterations for the MC simulation, N_{trials}, depends on the confidence level, which can be given as an input to the MC simulation framework. In this work, we limit the iterations, $N_{trials} = 500$. We compute the power grid TTF, for a given failure criterion, specified as a fraction of the nominal IR drop.

In practice, the benchmark circuits require minor modifications since the via connections in some of the original circuit netlists from [16] are short-circuited, implying the vias are represented by zero resistance. We have modified the netlist to alter the resistance of the vias according to the nominal resistance value for the corresponding via array. As in other work [2,3], we have tuned the wire geometry in the power grid benchmarks to obtain a reasonable IR drop. To highlight and focus on the impact of voids in via arrays, we assume that the PG network is designed such that spanning voids in wires have a very low probability, and for all practical purposes, EM failures occur in via arrays.

We fix the performance failure criterion as an IR-drop specification of 10% of V_{dd}. For quantifying the impact of redundancy due to via arrays, we perform simulations corresponding to two via array failure criteria: (a) the weakest-link criterion for via array, which renders a via array fail on the onset of the first via failure, and (b) the open-circuit criterion where a via array fails when all vias fail, i.e., $R = \infty$.



(a) TTF with 4×4 via arrays (b) TTF with 8×8 via arrays

Figure 10: TTF for PG1 employing 4×4 or 8×8 via array, for various choices of failure criteria

For PG1, under the two choices of via array configuration (4×4, 8×8) we show a set of curves in Figure 10 that indicate the CDF of the TTF. For the via array, we consider the weakest-link and $R = \infty$ (open-circuit) failure criteria, while for the power grid, we consider failure criteria to be based on the weakest link or on the 10% IR drop criterion. For a given via array failure criterion, we can observe that the worst-case TTF (at the 0.3%ile value) corresponding to the realistic system performance based failure criterion is larger compared to the weakest link system failure criterion. This occurs because the power grid continues to function satisfactorily well and meets the IR drop specifications well after the first via array failure, due to the inherent resiliency of power meshes. Table 2 shows the worst-case TTF (at the 0.3%ile value), elaborating on the data in Fig. 10, for a wider set of power grid benchmarks.

PG Benchmark	Weakest-link		Performance (10% IR-drop)	
	Via array failure criteria		Via array failure criteria	
	Weakest-link	$R = \infty$	Weakest-link	$R = \infty$
	Worst-case TTF (years) when 4×4 via array used			
PG1	0.8	2.0	1.5	3.9
PG2	0.9	3.1	2.2	5.5
PG5	1.7	4.4	3.1	10.2
	Worst-case TTF (years) when 8×8 via array used			
PG1	0.9	4.2	1.7	7.6
PG2	1.0	4.9	2.8	7.9
PG5	1.9	8.4	4.5	16.7

Table 2: TTF for power grid benchmarks using via arrays

For a given system failure criterion, the worst-case TTF corresponding to the traditional weakest-link via array failure criterion is seen to be significantly smaller than the value for more realistic via array failure criteria. This procedure therefore indicates and quantifies the benefit of modeling vias as via arrays that have redundant conducting elements, in contrast to modeling them as single conducting elements, as in prior work on power grid EM. Therefore, the notion of treating a via array as a single unit, with its own characterized TTF, capturing redundancy as well as thermomechanical stress effects, can be used to significantly improve the analysis of the circuit TTF.

Lastly, as expected, for a given choice of system and via array failure criteria, the power grid that employs 8×8 via array shows better EM performance compared to the 4×4 via array. Specifically, for a system performance criterion of 10% IR-drop and the open-circuit via array criterion, the worst-case TTF increases by several years between the two configurations. This suggests that there is a benefit of employing a via array with larger granularity. Our method helps to quantify this improvement.

6 CONCLUSION

We have demonstrated a methodology to analyze EM-induced performance degradation of power grids in the context of via arrays. Our analysis demonstrates that the important parameters which determine EM performance degradation, such as thermomechanical stress and the electrical redundancy, are a function of the via array configuration. We quantify the EM-induced performance degradation for power grids and we compare the EM reliability of the power grid using various via array configurations. Our analysis assumes that each via array configuration occupies the same area. In practice, a larger via array may occupy a larger area as a consequence of minimum spacing rules for vias and this is part of our future work.

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