

CURRICULUM VITAE

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EDUCATION

- Ph.D., Electrical Engineering and Computer Sciences, University of California, Berkeley, September 1988, Research Advisor: Prof. David G. Messerschmitt.
THESIS: Algorithm and Architecture Designs for High-Speed Digital Signal Processing
- M.S.E.E., Univ. of Pennsylvania, Philadelphia, May 1984, Concentrated on signal processing and VLSI IC design. Research Advisor: (Late) Prof. Raymond S. Berkowitz.
THESIS: Application of Importance Sampling for False Alarm Setting in Complex Multi-Dimensional Signal Processing Systems
- B.Tech. (Honors), Indian Institute of Technology, Kharagpur, India, May, 1982, Electrical Engineering.

INDUSTRIAL AND ACADEMIC EXPERIENCE

- Professor (Tenured), Department of Electrical Engineering, University of Minnesota, Minneapolis, MN, 55455 (starting July 1995). Edgar F. Johnson Professor (Starting July 1997). Distinguished McKnight University Professor (Starting July 2000). Associate Professor with Tenure (July 1992 - June 1995), Assistant Professor (Oct. 1988 - June 1992), Research efforts directed towards VLSI Architectures for Digital Signal Processing with Applications to Wireless and Video Processing, VLSI Digital Filters, Adaptive Filters and Beamformers, Video Compression, Error Control Coders, Cryptography, Computer Arithmetic, Low-Power Digital Systems, CAD for Low-Power, Digital IC Design and FPGA System Prototyping, DNA computing and DNA signal processing, and Hardware Security. Current research is also directed towards biomedical signal processing and signal classification, particularly with the use of machine learning techniques. Current applications include biomarkers for schizophrenia, epilepsy, and mental disorders from MEG, EEG, and functional MRI. Other applications include retinal image analysis from fundus images and OCT.
- Visiting Professor, Fudan University, Shanghai, China, 2017
- President, Leanics Corporation, 2005-2012
- Medtronic, Inc., Minneapolis, MN, 2006-2007, on Sabbatical Leave

- Broadcom Corp., Irvine, (2000-2002), Senior Principal Scientist and Technical Director - DSP Systems, Office of CTO (on Leave)
- Technical Advisory Board, Morphics, Inc. (2002-2003)
- Visiting Professor, Lund Univ., Sweden (April 1999)
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (1996-97 Academic Year, on Leave as National Science Foundation Fellow)
- Visiting Professor, Delft Univ., The Netherlands (March - April, 1996)
- Associate Professor (Tenured), Department of Electrical Engineering, University of Minnesota, Minneapolis, (July 1992 - June 1995).
- Assistant Professor, Department of Electrical Engineering, University of Minnesota, Minneapolis, (October 1988 - June 1992).
- Visiting Researcher, NEC C&C Laboratories, Kanagawa, Japan (April 1992 - June 1992), Researched VLSI Architectures for Discrete Wavelet Transforms.
- Consultant to Dorsey and Whitney (2007), Theseus Logic (1996-1999), United Nations Development Program (1995), Top-Vu Technology, Inc. (1994) US West Advanced Technologies (1989), Bell Labs (1987 - 1988),
- Summer Job at AT&T Bell Laboratories, Holmdel, NJ during Summer 1987.
- Summer job at the IBM T.J. Watson Research Center, Yorktown Heights, NY, during Summer 1986.

AWARDS AND HONORS

- Mac Van Valkenburg Award, IEEE Circuits and Systems Society (2017)
- IEEE Trans. VLSI Systems Prize Paper Award (2017)
- Best Paper Award at the 2017 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2017)
- Best Paper Award at the 2016 ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED) (2016)
- Best (Student) Paper Award for the Design and Implementation of Signal Processing Systems (DISPS) Track at the IEEE ICASSP Conference (2015)
- Best (Student) Paper Award at the 6th IEEE Int. Conference on Neural Engineering (2013)
- Distinguished Alumnus Award, Indian Institute of Technology, Kharagpur (2013)

- Award for Outstanding Contributions to Postbaccalaureate, Graduate, and Professional Education, University of Minnesota (2013)
- Best (Third Place Student) Paper Award, 2012 Asilomar Conference on Signals, Systems and Computers (2012)
- IEEE Charles A. Desoer Technical Achievement Award, IEEE Circuits and Systems Society (2012)
- Frederick Emmons Terman Award from American Society of Engineering Education (2004)
- Best (Student) Paper Award at the Asilomar Conference on Signals, Systems and Computers (2004)
- ACM Great Lakes Symp. Best Paper Award, 2004
- IEEE Kiyo Tomiyasu Technical Field Award (2003)
- IEEE W.R.G. Baker Best Paper Award (2001)
- Distinguished McKnight University Professorship (2000-)
- IEEE Circuits and Systems Society Golden Jubilee Medal (1999)
- Judge, IEEE Fellow Selection Committee (1998-2000)
- Fellow, IEEE (1996)
- Best Paper Award at 33rd Design Automation Conference, June 1996
- IEEE Circuits and Systems Society Distinguished Lecturer (1996-1997)
- Darlington Best Paper Award of the IEEE Circuits and Systems Society, 1994
- Guillemin-Cauer Best paper Award of the IEEE Circuits and Systems Society, 1993
- National Science Foundation Young Investigator Award, 1992-1997
- McKnight - Land Grant Professorship at the Univ. of Minnesota, 1992 - 1994
- IEEE Signal Processing Society Paper Award, 1991,
- IEEE Browder J. Thompson Memorial Prize paper Award, 1991
- NSF Research Initiation Award, 1989
- Eliahu Jury Award (for excellence in systems research), 1987, U.C. Berkeley
- Demetri Angelakos Award (for altruistic activities afforded fellow graduate students), 1987, U.C. Berkeley
- IBM Graduate Fellowship, 1987-88
- U.C. Regents Fellowship, 1986-87

Patents

1. R.A. Freking and K.K. Parhi, "Fast and Small Serial Variable Length Encoder with an Optimally High Rate for Encoding Including Huffman Encoding", U.S. Patent Number 6,271,689, August 7, 2001
2. R.A. Freking and K.K. Parhi, "Concurrent Method for Parallel Huffman Compression Coding and Other Variable Length Encoding and Decoding", U.S. Patent Number 6,304,197, October 16, 2001
3. R.A. Freking and K.K. Parhi, "Fast and Small Serial Huffman Decoder for Decoding at an Optimally High Rate", U.S. Patent Number 6,307,489, October 23, 2001
4. W. Freking and K.K. Parhi, "Fast Parallel cascaded Array Modular Multiplier", U.S. Patent Number 6,892,215, Issued May 10, 2005
5. K.K. Parhi, "System and Method for Generating Cyclic Codes for Error Control in Digital Communications", US Patent Number 6,895,545, Issued May 17, 2005
6. W. Freking and K.K. Parhi, "Systolic Cylindrical Array Modular Multiplier", US Patent Number 6,907,440, Issued June 14, 2005
7. K.K. Parhi, J.G. Chung, and K.J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier", US Patent Number 6,978,426, Issued December 20, 2005
8. W. Freking and K.K. Parhi, "Systolic Ring Planarized Cylindrical Array Modular Multiplier", US Patent 7,010,561, Issued March 7, 2006
9. K.K. Parhi, "Pipelined Add-Compare-Select Circuits and Methods, and Applications there of", US Patent 7,020,831, Issued March 28, 2006
10. K.K. Parhi, J.-G. Chung and S.-M. Kim, "Low-Error Canonic-Signed-Digit Fixed-Width Multiplier, and Method for Designing Same", US Patent 7,080,115, Issued July 18, 2006
11. T. Zhang and K.K. Parhi, "LDPC Code and Encoder/Decoder Regarding Same", US Patent 7,120,856, Issued Oct. 10, 2006
12. Z. Wang and K.K. Parhi, "Area-Efficient Parallel Turbo Decoding", US Patent 7,200,799, Issued April 3, 2007
13. K.K. Parhi, "Pipelining of Multiplexor Loops in a Digital Circuit", US Patent 7,239,652, Issued July 3, 2007
14. K.K. Parhi and J. Kong, "Low-Latency Architectures for High-Throughput Viterbi Decoders", US Patent 7,308,640, Issued December 11, 2007
15. K.K. Parhi, "Pipelined Parallel Processing of Feedback Loops in a Digital Circuit", US Patent 7,333,580, Issued Feb. 19, 2008

16. K.K. Parhi, J.-G. Chung, K.-C. Lee, K.-J. Cho, "Low-Error Fixed-Width Modified Booth Multiplier," US Patent 7,334,200, Feb. 19, 2008
17. K.K. Parhi, "System and method for generating cyclic codes for error control in digital communications", US Patent 7,539,918, Issued May 26, 2009
18. K.K. Parhi and Y. Gu , "System and Method for MIMO Equalization for DSP Transceivers", US Patent 7,561,633, Issued July 14, 2009
19. A.E. Cohen and K.K. Parhi, "Low-Complexity Hybrid LDPC Code Encoder", US Patent 7,657,816, Issued Feb. 2, 2010
20. Y. Gu and K.K. Parhi, "Parallel Tomlinson Harashima Precoders", US Patent 7,693,233, Issued April 6, 2010
21. S.M. Kim, K.K. Parhi, and R. Liu, "System and Method for Designing RS Based LDPC Code Decoder", US Patent 7,716,553, Issued May 11, 2010
22. K.K. Parhi and Y. Gu, "High-Speed Precoders for Communications Systems", US Patent 7,769,099, Issued August 3, 2010
23. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", US Patent 7,933,341, Issued April 26, 2011
24. K.K. Parhi and Y. Gu, "System and Method for Low-Power Echo and NEXT Cancellers", US Patent 8,009,823, Issued August 30, 2011
25. A. Cohen and K.K. Parhi, "System for Secure Variable Data Rate Transmission", US Patent 8,416,948, Issued April 9, 2013
26. O.E. Agazzi, G. Ungerboeck, K.K. Parhi, C.A. Lutkemeyer, P. Vorenkamp, K.T. Chan, and M.H. Wakayama, "System and method for high speed communications using digital signal processing", US Patent 8,422,591, Issued April 16, 2013
27. J. Chen and K.K. Parhi "System for MIMO equalization of multi-channel transceivers with precoding," US Patent 8,498,343, Issued July 30, 2013
28. J. Chen and K.K. Parhi, "System for Low-Complexity Adaptive Echo and NEXT Cancellers", US Patent 8,600,039, Issued Dec. 3, 2013
29. J. Chen and K.K. Parhi, "System for FEXT Cancellation of Multi-Channel Transceivers with Precoding", US Patent 8,699,551, Issued April 15, 2014

IEEE 802.3 Standards Presentations

1. K.K. Parhi, C. Lutkemeyer, A. Abnous and M. Hatamian, "Parallel Implementation of the DSP Functions of the PAM-5 10 Gb/s Transceiver", IEEE 802 Plenary meeting, March 2000, http://grouper.ieee.org/groups/802/3/ae/public/mar00/parhi_1_0300.pdf
2. O. Agazzi, V. Gopinathan, K. Parhi, K. Kota, A. Phanse, "DSP Based Equalization for Optical Channels", http://grouper.ieee.org/groups/802/3/ae/public/sep00/agazzi_1_0900.pdf
3. K.K. Parhi and Y. Gu, "Interleaved Trellis Coded Modulation and Decoding", http://grouper.ieee.org/groups/802/3/10GBT/public/jul03/parhi_1_0703.pdf
4. K.K. Parhi and Y. Gu, "Pipelining Tomlinson Harashima Precoders", http://grouper.ieee.org/groups/802/3/an/public/sep04/parhi_1_0904.pdf

Books

1. N.R. Shanbhag, and K.K. Parhi, *Pipelined Adaptive Digital Filters*, Kluwer Academic Publishers, 1994
2. R.I. Hartley, and K.K. Parhi, *Digit-Serial Computation*, Kluwer Academic Publishers, 1995
3. T. Nishitani and K.K. Parhi, ed., *VLSI Signal Processing VIII*, IEEE Press, 1995
4. J.-G. Chung and K.K. Parhi, *Pipelined Lattice and Wave Digital Recursive Filters*, Kluwer Academic Publishers, 1996
5. J. Fortes, C. Mongenet, K. Parhi, and V. Taylor, Ed., *Proceedings 1996 International Conference on Application Specific Systems, Architectures, and Processors*, IEEE Computer Society Press, 1996
6. K.K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, NY 1999
7. K.K. Parhi and T. Nishitani, Ed., *Digital Signal processing for Multimedia Systems*, Marcel Dekker, NY, 1999

Book Chapters

1. K.K. Parhi, and M. Hatamian, "A High Sample Rate Recursive Filter Chip", in *VLSI Signal Processing III*, Chapter 1, IEEE Press, (Proc. of the Third IEEE VLSI Signal Processing Workshop), Monterey, CA, Nov. 1988, pp. 3-14
2. K.K. Parhi, and G. Shrimali, "A Concurrent Loss-Less Coder for Video Compression", in *VLSI Signal Processing V*, IEEE Press, Oct. 1992 (Proc. of the Fifth IEEE VLSI Signal Processing Workshop, Napa Valley, CA), pp. 257-266
3. K.K. Parhi, "Parallel Processing and Pipelining in Huffman Decoder", (Chapter 12) in *VLSI Implementations for Image Communications*, Series Advances in Image Communications (Edited by Peter Pirsch), **Vol. 2**, Elsevier Science Publisher, Amsterdam, 1993, pp. 365-395
4. K.K. Parhi, "VLSI For Signal Processing: Special Architectures", in *The Electrical Engineering Handbook*, edited by Richard C. Dorf, CRC Press, 1993, pp. 370-384 (Chapter 17, Section 17.1)
5. N.R. Shanbhag, and K.K. Parhi, "VLSI Implementation of a 100 MHz Pipelined AD-PCM Codec Chip", in *VLSI Signal Processing VI*, IEEE Press, Oct. 1993 (Proc. of the sixth IEEE VLSI Signal Processing Workshop, Veldhoven, Netherlands), pp. 114-122

6. C.Y. Wang, and K.K. Parhi, "The MARS High-Level DSP Synthesis System", in *VLSI Design Methodologies for Digital Signal Processing Architectures*, edited by M. Bayoumi, pp. 169-205, Kluwer Academic Press, 1994
7. J.-G. Chung and K.K. Parhi, "Pipelined Wave Digital Filter Design for Narrow-Band Sharp-Transition Digital Filters", in *VLSI Signal Processing VII*, pp. 501-510, IEEE Press, Oct. 1994 (Proc. of the Seventh IEEE VLSI Signal Processing Workshop, La Jolla, CA)
8. S. Jain and K.K. Parhi, "Efficient Power Based Galois Field Arithmetic Architectures", in *VLSI Signal Processing VII*, pp. 306-315, IEEE Press, Oct. 1994 (Proc. of the Seventh IEEE VLSI Signal Processing Workshop, La Jolla, CA)
9. K.K. Parhi, "High-Level Transformations for DSP Synthesis", Chapter 8.1 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 575-587, IEEE Press, 1995
10. N.R. Shanbhag and K.K. Parhi, "Pipelined Adaptive Digital Filters", Chapter 8.2 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 589-601, IEEE Press, 1995
11. C.-Y. Wang and K.K. Parhi, "High-Level DSP Synthesis", Chapter 8.4 in *Microsystems Technology for Multimedia Applications: An Introduction*, edited by B. Sheu *et al.*, IEEE ISCAS-95 Tutorial Book, pp. 615-627, IEEE Press, 1995
12. T.C. Denk and K.K. Parhi, "Systematic Design of Architectures for M-ary Tree-Structured Filter Banks", pp. 157-166, in *VLSI Signal Processing VIII*, IEEE Press, October 1995 (Proc. of the 1995 IEEE Workshop on VLSI Signal Processing, Sakai, Japan)
13. K. Ito and K.K. Parhi, "Register Minimization in Cost-Optimal Synthesis of DSP Architectures", pp. 207-216, in *VLSI Signal Processing VIII*, IEEE Press, October 1995 (Proc. of the 1995 IEEE Workshop on VLSI Signal Processing, Sakai, Japan)
14. K.K. Parhi and F. Catthoor, "Design of High-Performance DSP Systems", Chapter in *Emerging Technologies: Designing Low-Power Digital Systems*, Edited by R. Cavin and W. Liu, pp. 447-507, IEEE Press (ISCAS-96 Tutorial Book)
15. L. Montalvo, K.K. Parhi, and J.H. Satyanarayana, "Estimation of Average Energy Consumption of Ripple-Carry Adder Based on Maximum Average Carry Chains", in *VLSI Signal Processing IX*, pp. 189-198, IEEE Press, October 1996 (Proc. of the 1996 IEEE Workshop on VLSI Signal Processing, San Francisco)
16. K.K. Parhi, "Low-Power Digital VLSI Approaches", Chapter in *Circuits and Systems in the Information Age*, Edited by Y. Huang and C. Wei, pp. 3-22, IEEE Press, June 1997 (ISCAS-97 Tutorial Book)
17. K.K. Parhi, "Video Compression", *Chapter 2 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 17-41, Marcel Dekker, New York, 1999

18. T.C. Denk and K.K. Parhi, "Wavelet VLSI Architectures", *Chapter 13 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 329-353, Marcel Dekker, New York, 1999
19. K.J. Raghunath and K.K. Parhi, "Pipelined RLS for VLSI: STAR-RLS Filters", *Chapter 19 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 519-550, Marcel Dekker, New York, 1999
20. H.R. Srinivas and K.K. Parhi, "Division and Square-Root", *Chapter 20 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 551-587, Marcel Dekker, New York, 1999
21. L. Song and K.K. Parhi, "Finite Field Arithmetic Architectures", *Chapter 21 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 589-621, Marcel Dekker, New York, 1999
22. J.H. Satyanarayana and K.K. Parhi, "Power Estimation Approaches", *Chapter 25 in Digital Signal Processing for Multimedia Systems*, Edited by K.K. Parhi and T. Nishitani, pp. 741-772, Marcel Dekker, New York, 1999
23. J.P. Ma and K.K. Parhi, "On Pipelined Implementations of QRD-RLS Adaptive Filters", *Chapter in QRD-RLS Adaptive Filters*, Edited by J.A. Apolinario, Jr., pp. 269-297, Springer-Verlag, 2009
24. K.K. Parhi and Y. Chen, "Signal Flow Graphs and Data Flow Graphs", *Handbook of Signal Processing Systems*, Vol. 4, Edited by S.S. Bhattacharyya, E.F. Deprettere, R. Leupers and J. Takala, pp. 791-816, Springer-Verlag, 2010
25. H.A. Patil, A.E. Cohen, and K.K. Parhi, "Speaker Identification over Narrowband VoIP Networks", *Chapter 6 in Advances in Forensic Speaker Recognition: Criminal Justice and Counterterrorism*, Edited by A. Neustein and H. Patil, Springer Science+Business Media LLC, 2011, pp. 125-151
26. V. Kulkarni, H. Jiang, E. Kharisov, N. Hovakimyan, M. Riedel, K. Parhi, "Synchronous Sequential Computations with Biomolecular Reactions," *Chapter 14 in Systems and Synthetic Biology Book*, Edited by V. Singh and P. K. Dhar, Springer Verlag, Netherlands, 2015, pp. 255-279
27. S. Roychowdhury, D. Koozekanani, M. Reinsbach and K.K. Parhi, "Automated OCT Segmentation for OCT Images with DME," Invited Book Chapter for *Medical Image Analysis and Informatics: Computer-aided Diagnosis and Therapy*, edited by R. Rangayyan, P.M. de Azevedo-Marques, and M. Salmeri, CRC Press, 2017

Journal Publications

1. K.K. Parhi and D.G. Messerschmitt, "Concurrent Cellular VLSI Adaptive Filter Architectures", *IEEE Transactions on Circuits and Systems*, **Vol. CAS-34**, No. 10, October 1987, pp. 1141-1151
2. K.K. Parhi and R.S. Berkowitz, "On Optimizing Importance Sampling Simulations", *IEEE Transactions of Circuits and Systems*, **Vol. CAS-34**, No. 12, December 1987, pp. 1558-1563
3. K.K. Parhi, and D.G. Messerschmitt, "Concurrent Architectures for Two-Dimensional Recursive Digital Filtering", *IEEE Trans. on Circuits and Systems*, **Vol. CAS-36(6)**, June 1989, pp. 813-829
4. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part I: Pipelining using Scattered Look-Ahead and Decomposition", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1099-1117
5. K.K. Parhi, and D.G. Messerschmitt, "Pipeline Interleaving and Parallelism in recursive Digital Filters, Part II: Pipelined Incremental Block Filtering", *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **Vol. 37(7)**, July 1989, pp. 1118-1135
6. K.K. Parhi, "Algorithm Transformation Techniques for Concurrent Processors", *Proceedings of the IEEE*, Special Issue on Supercomputer Technology, **Vol. 77(12)**, December 1989, pp. 1879-1895
7. K.K. Parhi, and D.G. Messerschmitt, "Static Rate-Optimal Scheduling of Iterative Data Flow Programs via Optimum Unfolding", *IEEE Trans. on Computers*, **Vol. 40(2)**, February 1991, pp. 178-195
8. K.K. Parhi, "A Systematic Approach for Design of Digit-Serial Signal Processing Architectures", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 4, April 1991, pp. 358-375
9. K.K. Parhi, "Pipelining In Dynamic Programming Architectures", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1442-1450
10. K.K. Parhi, "Finite Word Effects in Pipelined Recursive Filters", *IEEE Trans. on Signal Processing*, **Vol. 39**, No. 6, June 1991, pp. 1450-1454
11. K.K. Parhi, "Pipelining in Algorithms with Quantizer Loops", *IEEE Trans. on Circuits and Systems*, **Vol. 38**, No. 7, July 1991, pp. 745-754
12. K.K. Parhi, "Technology for the 90s: VLSI Signal and Image Processing Systems", *IEEE Circuits and Devices Magazine* (special technology forecast issue), **7(4)**, July 1991 (invited article), pp. 16-17

13. K.K. Parhi, "Research on VLSI For Digital Video Systems in Japan", *Asian Scientific Information Bulletin of the Office of Naval Research Office*, **16**(4), October - December 1991, pp. 93-98
14. K.K. Parhi, C.Y. Wang, A.P. Brown, "Synthesis of Control Circuits in Folded Pipelined DSP Architectures", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 1, January 1992, pp. 29-43
15. M. Hatamian and K.K. Parhi, "An 85-MHz Fourth-Order Programmable IIR Digital Filter Chip", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 2, February 1992, pp. 175-183
16. H.R. Srinivas, and K.K. Parhi, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", *Journal of VLSI Signal Processing*, **Vol. 4**, No. 2/3, 1992, pp. 177-198
17. H.R. Srinivas, and K.K. Parhi, "A Fast VLSI Adder Architecture", *IEEE Journal of Solid State Circuits*, **Vol. 27**, No. 5, May 1992, pp. 761-767
18. K.K. Parhi, "High-Speed VLSI Architectures for Huffman and Viterbi Decoders", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 6, June 1992, pp. 385-391
19. K.K. Parhi, "Video Data Format Converters Using Minimum Number of Registers", *IEEE Transactions on Circuits and Systems For Video Technology*, **Vol. 2**, No. 2, June 1992, pp. 255-267
20. K.K. Parhi, "Systematic Synthesis of DSP Data Format Converters using Life-Time Analysis and Forward-Backward Register Allocation", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 39**, No. 7, July 1992, pp. 423-440
21. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Differential Vector Quantizer for Low-Power Speech Coding Applications", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **40**(5), May 1993, pp. 347-349
22. N.R. Shanbhag, and K.K. Parhi, "A Pipelined Adaptive Lattice Filter Architecture", *IEEE Trans. on Signal Processing*, **41**(5), May 1993, pp. 1925-1939
23. K.J. Raghunath, and K.K. Parhi, "Parallel Adaptive Decision Feedback Equalizers", *IEEE Transactions on Signal Processing*, **41**(5), May 1993, pp. 1956-1961
24. K.K. Parhi, and T. Nishitani, "VLSI Architectures for Discrete Wavelet Transforms", *IEEE Trans. on VLSI Systems*, **1**(2), June 1993, pp. 191-202
25. L.E. Lucke, and K.K. Parhi, "Data-Flow Transformations for Critical Path Time Reduction For High-Level DSP Synthesis", *IEEE Transactions on Computer Aided Design of Integrated Circuits And Systems*, **12**(7), July 1993, pp. 1063-1068

26. N.R. Shanbhag, and K.K. Parhi, "Relaxed Look-Ahead Pipelined LMS Adaptive Filters and Their Application to ADPCM Coder", *IEEE Transactions on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **Vol. 40**(12), December 1993, pp. 753-766
27. K.K. Parhi, F.H. Wu, and K. Ganesan, "Sequential and Parallel Neural Network Vector Quantizers", *IEEE Transactions on Computers*, **43**(1), pp. 104-109, January 1994
28. J.-G. Chung, and K.K. Parhi, "Pipelining of Lattice IIR Digital Filters", *IEEE Transactions on Signal Processing*, **42**(4), pp. 751-761, April 1994
29. L.E. Lucke, and K.K. Parhi, "Parallel Processing Architectures for Rank-Order and Stack Filters", *IEEE Transactions on Signal Processing*, **42**(5), pp. 1178-1189, May 1994
30. N.R. Shanbhag, and K.K. Parhi, "Finite Precision Analysis of the ADPCM Coder", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(5), pp. 364-368, May 1994
31. K.K. Parhi, "Calculation of Minimum Number of Registers in Arbitrary Life Time Chart", *IEEE Circuits and Systems Transactions - Part II: Analog and Digital Signal Processing*, **41**(6), pp. 434-436, June 1994
32. N.R. Shanbhag, and K.K. Parhi, "Corrections to "Finite Precision Analysis of the ADPCM Coder"", *IEEE Transactions on Circuits and Systems-Part II: Analog and Digital Signal Processing*, **41**(7), pp. 493, July 1994
33. G.B. Adams III, E.J. Coyle, L. Lin, L.E. Lucke, and K.K. Parhi, "Input Compression and Efficient VLSI Architectures for Rank-Order and Stack Filters", *Signal Processing*, **38**, pp. 441-453, August 1994
34. H.R. Srinivas, B. Vinnakota, and K.K. Parhi, "A C-Testable Carry-Free Divider", *IEEE Trans. on VLSI Systems*, **2**(4), pp. 472-488, December 1994
35. K.K. Parhi, "High-Level Algorithm and Architecture Transformations for DSP Synthesis", *Journal of VLSI Signal Processing*, **9**(1), pp. 121-143, January 1995
36. C.-Y. Wang, and K.K. Parhi, "High-Level DSP Synthesis using Concurrent Transformations, Scheduling, and Allocation", *IEEE Transactions on Computer Aided Design*, **14**(3), pp. 274-295, March 1995
37. J.-G. Chung, and K.K. Parhi, "Scaled Normalized Lattice Digital Filters", *IEEE Transactions on Circuits and Systems - Part II: Analog and Digital Signal Processing*, **42**(4), pp. 278-282, April 1995
38. N.R. Shanbhag, and K.K. Parhi, "Pipelined Adaptive DFE Architectures using Relaxed Look-Ahead", *IEEE Trans. on Signal Processing*, **43**(6), pp. 1368-1385, June 1995

39. H.R. Srinivas, and K.K. Parhi, "A Fast Radix-4 Division Algorithm", *IEEE Transactions on Computers*, **44**(6), pp. 826-831, June 1995
40. J.-G. Chung, H. Kim and K.K. Parhi, "Pipelined Lattice WDF Design for Wideband Filters", *IEEE Trans. on Circuits and Systems, Part II: Analog and Digital Signal Processing*, **42**(9), pp. 616-618, September 1995
41. C.-Y. Wang, and K.K. Parhi, "Resource Constrained Loop List Scheduler for DSP Algorithms", *Journal of VLSI Signal Processing*, **11**(1/2), pp. 75-96, October 1995
42. K. Ito and K.K. Parhi, "Determining the Minimum Iteration Period of an Algorithm", *Journal of VLSI Signal Processing*, **11**(3), pp. 229-244, December 1995
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327. Y. Wang, B. Yuan, K.K. Parhi and R. Victora, "Two-Dimensional Magnetic Recording using a Rotated Head Array and LDPC Code Decoding," *2014 IEEE International Magnetism Conference (INTERMAG) Digest*, Dresden, Germany, May 2014
328. B. Yuan and K.K. Parhi, "Architectures for Polar BP Decoders Using Folding," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 205-208, Melbourne, Australia, June 2014
329. K.K. Parhi and Y. Liu, "Architectures for IIR Digital Filters Using Stochastic Computing," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 373-376, Melbourne, Australia, June 2014

330. C. Zhang and K.K. Parhi, "Interleaved Successive Cancellation Polar Decoders," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 401-404, Melbourne, Australia, June 2014
331. Y. Lao and K.K. Parhi, "Protecting DSP Circuits Through Obfuscation," *Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 798-801, Melbourne, Australia, June 2014
332. Z. Zhang and K.K. Parhi, "Seizure Detection using Wavelet Decomposition of the Prediction Error Signal from a Single Channel of Intra-Cranial EEG," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4443-4446, Aug. 2014, Chicago, IL
333. M. Bandarabadi, C. Teixeira, T. Netoff, K.K. Parhi, and A. Dourado, "Robust and Low Complexity Algorithms for Seizure Detection," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4447-4450, Aug. 2014, Chicago, IL
334. T. Xu, K.R. Cullen, A. Hourri, K.O. Lim, S.C. Schulz, and K.K. Parhi, "Classification of Borderline Personality Disorder based on Spectral Power of Resting-State fMRI," *Proc. of 2014 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 5036-5039, Aug. 2014, Chicago, IL
335. Q. Tang, B. Kim, Y. Lao, K.K. Parhi and C. Kim, "True Random Number Generator Circuits Based on Single- and Multi-Phase Beat Frequency Detection," *Proc. of 2014 IEEE Customs Integrated Circuits Conference*, September 2014, San Jose, CA
336. B. Yuan and K.K. Parhi, "Successive Cancellation List Polar Decoder using Log-likelihood Ratios," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014
337. M. Parhi, Y. Lao and K.K. Parhi, "Canonic Real Valued FFT Structures," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014
338. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Asynchronous Discrete-time Signal Processing with Molecular Reactions," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014
339. B. Yuan and K.K. Parhi, "Algorithm and Architecture for Hybrid Decoding of Polar Codes," *Proc. 2014 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, November 2014
340. S. Chu, C. Lenglet and K.K. Parhi, "Brain connectivity from diffusion and functional MRI using a network flow model," *Proc. of 2015 SPIE Medical Imaging Conference*, Feb. 2015, Orlando, FL

341. Y. Liu and K.K. Parhi, "Lattice FIR Digital Filters using Stochastic Computing," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1027-1031, Brisbane, Australia, April 2015
342. G.N.C. Shanmugam, Y. Lao and K.K. Parhi, "An Obfuscated Radix-2 Real FFT Architecture," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1056-1060, Brisbane, Australia, April 2015
343. A. Chinnapalanichamy and K.K. Parhi, "Serial and Interleaved Architectures for Computing Real FFT," *Proc. of 2015 IEEE Int. Conf. Acoustics, Speech and Signal Processing (ICASSP)*, pp. 1066-1070, Brisbane, Australia, April 2015
344. B. Yuan and K.K. Parhi, "Successive Cancellation Decoding of Polar Codes Using Stochastic Computing," *Proc. of 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015
345. R. Parhi, C.H. Kim, and K.K. Parhi, "Fault-Tolerant Ripple-Carry Binary Adder Using Partial Triple Modular Redundancy (PTMR)," *Proc. of 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015
346. B. Yuan and K.K. Parhi, "Reduced-latency LLR-based SC List Decoder for Polar Codes," *Proc. of 2015 ACM Great Lakes Symposium on VLSI*, pp. 107-110, Pittsburgh, May 2015
347. M. Parhi, M.D. Riedel, and K.K. Parhi, "Effect of Bit-Level Correlation in Stochastic Computing," *Proc. 2015 IEEE International Conference on Digital Signal Processing (DSP)*, pp. 463-467, Singapore, July 2015
348. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Markov Chain Computations using Molecular Reactions," *Proc. 2015 IEEE International Conference on Digital Signal Processing (DSP)*, pp. 689-693, Singapore, July 2015
349. S. Roychowdhury, D.D. Koozekanani, M. Reinsbach, K.K. Parhi, "3-D Localization of Diabetic Macular Edema using OCT Thickness Maps," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 4334-4337, Milan, Italy, August 2015
350. Z. Zhang and K.K. Parhi, "Seizure Prediction using Polynomial SVM Classification," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 5748-5751, Milan, Italy, August 2015
351. Z. Zhang and K.K. Parhi, "Seizure Detection using Regression Tree Based Feature Selection and Polynomial SVM Classification," *Proc. of 2015 IEEE Engineering in Medicine and Biology Society Conference (EMBC)*, pp. 6578-6581, Milan, Italy, August 2015
352. Y. Lao and K.K. Parhi, "Canonic Real-Valued Radix-2 FFT Computations," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 441-446, Pacific Grove, CA, Nov. 2015

353. Z. Zhang, T.R. Henry and K.K. Parhi, "Seizure Prediction using Cross-Correlation and Classification," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 775-779, Pacific Grove, CA, Nov. 2015
354. Y. Liu and K.K. Parhi, "Architectures for Stochastic Normalized and Modified Lattice IIR Filters," *Proc. 2015 Asilomar Conference on Signals, Systems and Computers*, pp. 1351-1358, Pacific Grove, CA, Nov. 2015 *Invited Talk*
355. S. Koteswara, C.H. Kim and K.K. Parhi, "Mode-based Obfuscation using Control-Flow Modifications," *Proc. of Third Workshop on Cryptography and Security in Computing Systems (CS2)*, pp. 19-24, Prague, Jan. 20, 2016
356. S.V.S. Avvaru, C. Zhou, S. Satapathy, Y. Lao, C. Kim and K.K. Parhi, "Estimating Delay Differences of Arbiter PUFs Using Silicon Data," *Proc. of 2016 Design, Automation, Test in Europe (DATE)*, pp. 543-546, March 2016, Dresden
357. B. Yuan and K.K. Parhi, "Belief Propagation Decoding of Polar Codes using Stochastic Computing," *Proc. of 2016 Int. Symp. on Circuits and Systems*, Montreal, May 2016
358. Y. Liu and K.K. Parhi, "Computing Complex Functions using Factorization in Unipolar Stochastic Logic," *Proc. of 2016 ACM Great Lakes Symposium on VLSI*, Boston, MA, May 2016
359. C. Zhou, S. Satapathy, Y. Lao, K.K. Parhi and C.H. Kim, "oft Response Generation and Thresholding Strategies for Linear and Feed-Forward MUX PUFs," *Proc. of 2016 ACM/IEEE International Symposium on Low Power Electronics and Design*, pp. 124-129, San Francisco, Aug. 2016
360. S. Roychowdhury, D.D. Koozekanani, and K.K. Parhi, "Automated Detection of Neovascularization for Proliferative Diabetic Retinopathy Screening," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 1300-1303, Orlando, FL, August 2016
361. V. Vijayakumar, D.D. Koozekanani, S. Roychowdhury and K.K. Parhi, "Artery/Vein Classification of Retinal Blood Vessels using Feature Selection," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 1320-1323, Orlando, FL, August 2016
362. B. Sen, G. Bernstein, T. Xu, B. Mueller, M.W. Schreiner, K.R. Cullen, K.K. Parhi, "Classification of Obsessive-Compulsive Disorder from Resting-State fMRI," *Proc. of 38th Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, pp. 3606-3609, Orlando, FL, August 2016
363. Y. Liu, H. Venkataraman, Z. Zhang and K.K. Parhi, "Machine Learning Classifiers using Stochastic Logic," *Proc. 2016 IEEE Int. Conf. on Computer Design*, pp. 408-411, Phoenix, AZ, Oct. 2016

364. Y. Lao and K.K. Parhi, "Data-Canonic Real FFT Flow-Graphs for Composite Lengths," *Proc. 2016 IEEE Workshop on Signal Processing Systems*, pp. 189-194, Dallas, Oct. 2016
365. Y. Liu and K.K. Parhi, "Computing RBF Kernel for SVM Classification using Stochastic Logic," *Proc. 2016 IEEE Workshop on Signal Processing Systems*, pp. 327-332, Dallas, Oct. 2016
366. Y. Liu, M. Parhi and K.K. Parhi, "Synthesis of Correlated Bit Streams for Stochastic Computing," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 167-174, Pacific Grove, CA, Nov. 2016
367. Z. Zhang and K.K. Parhi, "Seizure Prediction using Long-Term Fragmented Intracranial Canine and Human EEG Recordings," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 361-365, Pacific Grove, CA, Nov. 2016
368. Y. Liu and K.K. Parhi, "Computing Hyperbolic Tangent and Sigmoid Functions using Stochastic Logic," *Proc. 2016 Asilomar Conference on Signals, Systems and Computers*, pp. 1580-1585, Pacific Grove, CA, Nov. 2016
369. S.A. Salehi, K.K. Parhi, M.D. Riedel, "Computing Polynomials by Chemical Reaction Networks," *Proc. 2016 IEEE Globecom Symposium*, Washington, D.C., Dec. 2016
370. B. Sen and K.K. Parhi, "Extraction of Common Task Signals and Spatial Maps from Group fMRI using a PARAFAC-Based Tensor Decomposition Technique," *Proc. 2017 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, New Orleans, Louisiana, pp. 1113-1117, March 2017
371. Q. Tang, C. Zhou, W. Choi, G. Kang, J. Park, K. Parhi, and C.H. Kim, "A DRAM based Physical Unclonable Function Capable of Generating $> 10^{32}$ Challenge Response Pairs per 1Kbit Array for Secure Chip Authentication," *Proc. 2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, Texas, April 30-May 3, 2017
372. S.A. Salehi, Y. Liu, M.D. Riedel and K.K. Parhi, "Computing Polynomials with Positive Coefficients using Stochastic Logic by Double-NAND Expansion," *Proc. 2017 ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 471-474, Banff, Canada, May 2017
373. K.K. Parhi, "Analysis of Stochastic Logic Circuits in Unipolar, Bipolar and Hybrid Formats," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017
374. S. Koteswara, A. Das and K.K. Parhi, "FPGA Implementation and Comparison of AES-GCM and Deoxys Authenticated Encryption Schemes," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017

375. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Hierarchical Functional Obfuscation of Integrated Circuits Using a Mode-Based Approach," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017
376. A. Koyily, C. Zhou, C.H. Kim, and K.K. Parhi, "An Entropy Test for Determining Whether a Mux PUF Is Linear or Nonlinear," *Proc. of 2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, Baltimore, Maryland, May 2017
377. C. Zhou, K.K. Parhi, and C.H. Kim, "Secure and Reliable XOR Arbiter PUF Design: An Experimental Study based on 1 Trillion Challenge Response Pair Measurements," *Proc. 2017 Design Automation Conference (DAC)*, Austin, Texas, June 2017
378. M. Liu, C. Zhou, Q. Tang, K.K. Parhi and C.H. Kim, "A Data Remanence based Approach to Generate 100% Stable Keys from an SRAM Physical Unclonable Function," *Proc. of 2017 IEEE International Symposium on Low-Power Electronics and Design (ISLPED)*, Taipei, Taiwan, July 2017
379. S.V. Sandeep Avvaru, C. Zhou, C.H. Kim and K.K. Parhi, "Predicting Hard and Soft-Responses and Identifying Stable Challenges of Mux PUFs Using ANN," *Proc. of 2017 IEEE Midwest Symp. on Circuits and Systems*, Boston, August 2017
380. S.A. Salehi, M.D. Riedel, and K.K. Parhi, "Molecular Computation of Complex Markov Chains with Self-Loop State Transitions," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, Oct. 29-Nov. 1, 2017
381. S. Koteshwara, C.H. Kim, and K.K. Parhi, "Functional Encryption of Integrated Circuits by Key-Based Dynamic Hybrid Obfuscation," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, Oct. 29-Nov. 1, 2017
382. S. Koteshwara, A. Das and K.K. Parhi, "Performance Comparison of AES-GCM-SIV and AES-GCM Algorithms for Authenticated Encryption on FPGA Platforms," *Proc. 2017 Asilomar Conference on Signals, Systems and Computers*, Pacific Grove, CA, Oct. 29-Nov. 1, 2017

Conference Abstracts Without Proceedings

1. H. Jiang, M. Riedel, and K. Parhi, "Signal Processing Functions with Biomolecular Reactions," *International Workshop on Bio-Design Automation*, Anaheim, CA, 2010
2. H. Jiang, M. Riedel, and K. Parhi, "Iterative Computation with Biomolecular Reactions," *Annual Institute of Biological Engineering Conference*, Boston, MA, 2010
3. H. Jiang, M. Riedel, and K. Parhi, "Digital Signal processing with DNA," *International Conference on DNA Computing*, Pasadena, CA, 2011
4. H. Jiang, M. Riedel, and K. Parhi, "Asynchronous Sequential Computation with Molecular Reactions," *International Workshop on Bio-Design Automation*, San Diego, CA, 2011

5. S. Roychowdhury, K.K. Parhi, M.G. Lawrence, and D.D. Koozekanani, "Automated Screening System for Detecting Diabetic Retinopathy: A Classification Approach," Poster presented at 2012 *Association for Research in Vision and Ophthalmology (ARVO) annual meeting*, Fort Lauderdale, May 2012
6. S. Radwan, S. Roychowdhury, J. Tokarev, H.F. Roemhild, K.K. Parhi, and D.D. Koozekanani, "Optical Coherence Tomography Predictors of Visual Outcome in Macular Edema," Poster presented at 2013 *Association for Research in Vision and Ophthalmology (ARVO) Annual Meeting*, Seattle, May 2013
7. S. Roychowdhury, D.D. Koozekanani, S. Radwan, and K.K. Parhi, "Automated Detection and Location Analysis of Diabetic Cysts in Retinal OCT Images: An Iterative Filtering Approach," Poster presented at 2013 *Association for Research in Vision and Ophthalmology (ARVO) Annual Meeting*, Fort Lauderdale, May 2013
8. K.K. Parhi and Z. Zhang, "Seizure Prediction using Ratio of Spectral Power from Single EEG Electrode," *Proc. of 6th International Workshop on Seizure Prediction (IWSP6)*, p. 39, Nov. 2013, San Diego
9. S. Roychowdhury, K.K. Parhi, M. Reinsbach, and D.D. Koozekanani, "Automated Intra-Retinal Layer Thickness Profile Analysis in Optical Coherence Tomography Images by Iterative High-Pass Filtering," Poster presented at 2014 *Association for Research in Vision and Ophthalmology (ARVO) Annual Meeting*, Orlando, FL, May 2014
10. Y. Wang, B. Yuan, K.K. Parhi and R. Victora, "Two-Dimensional Magnetic Recording using a Rotated Head Array and LDPC Code Decoding," *2014 IEEE International Magnetism Conference (INTERMAG) Digest*, Dresden, Germany, May 2014
11. S. Chu, C. Lenglet and K.K. Parhi, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at 2014 *IEEE EMBS BRAIN Grand Challenges Conference*, Nov. 2014, Washington, D.C.
12. K.K. Parhi, "Simple Features and Simple Classifiers for Cyber-Physical Systems: Applications to Seizure Detection and Prediction," Talk presented at *Workshop on Big Data Analytics in CPS: Enabling the Move from IoT to Real-Time Control*, April 2015, Seattle, Washington
13. S. Chu, K.K. Parhi and C. Lenglet, "Joint Brain Connectivity Estimation from Diffusion and Functional MRI Using a Network Flow Model," Poster presented at the *24th Annual Meeting of the International Society for Magnetic Resonance in Medicine (ISMRM)*, May 30-June 5, 2015, Toronto, Canada
14. Z. Zhang and K.K. Parhi, "Seizure Prediction using Polynomial Support Vector Machine Classification," Poster presented at the *7th International Workshop on Seizure Prediction*, August 3-6, 2015, Melbourne, Australia
15. S.A. Salehi, K.K. Parhi and M.D. Riedel, "Markov Chain Computations using Molecular Reactions," Poster Presented at the *21st International Conference on DNA Computing and Molecular Programming (DNA21)*, August 17-21, 2015, Cambridge, MA

16. K.K. Parhi, "Simple Features and Simple Classifiers for Cyber-Physical Systems: Applications to Seizure Detection and Prediction," *Talk at Workshop on Big Data Analytics in CPS: Enabling the Move From IoT to Real-Time Control*, Seattle, Washington, April 13, 2015, held in conjunction with CPS Week 2015 (*Invited Talk*)
17. Y. Wang, B. Yuan, K.K. Parhi, and B. Kumar, "Increased Data Throughput and BER Performance with Rotated Head Array in the Two Dimensional Magnetic Recording," *2016 joint MMM-IEEE International Magnetism Conference (INTERMAG)*, San Diego, Jan. 2016
18. K.K. Parhi, "Network Analysis of Functional Brain Connectivity in Borderline Personality Disorder Using Resting-State fMRI," *2016 Information Theory and Applications (ITA)*, San Diego, Jan. 2016 (*Invited Talk*)
19. A. Rashno, K.K. Parhi, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Intra-Retinal, Sub-Retinal and Sub-RPE Cyst Regions Segmentation in Age-Related Macular Degeneration (AMD) Subjects," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017
20. J. Kohler, A. Rashno, K.K. Parhi, P. Drayna, S. Radwan, and D.D. Koozekanani, "Correlation Between Initial Vision and Vision Improvement with Automatically Calculated Retinal Cyst Volume in Treated DME after Resolution," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017
21. K.K. Parhi, A. Rashno, B. Nazari, S. Sadri, H. Rabbani, P. Drayna, and D.D. Koozekanani, "Automated Fluid/Cyst Segmentation: A Quantitative Assessment of Diabetic Macular Edema," *Annual Meeting of the Association for Research in Vision and Ophthalmology (ARVO)*, Baltimore, MD, May 2017

Technical Society Activities: Organizational

1. Member, Board of Governors, IEEE Circuits and Systems Society (2005, 2006, 2007)
2. Member, IEEE CAS Society Fellow Selection Committee (2003, 2004, 2008)
3. Chair, VLSI Systems and Applications Technical Committee, IEEE Circuits and Systems Society (2002-2004)
4. Member, IEEE CASS Outstanding Young Author Award Committee (2003)
5. Member, IEEE Darlington and Guillemin-Cauer Prize Paper Committee (2004, 2005)
6. Chair, ASEE Frederick Emmons Terman Award Selection Committee (2005)
7. Judge, IEEE Fellow Committee, 1998, 1999
8. Judge, ASP-DAC Best Paper Selection Committee (1998)
9. Member, IEEE VLSI Trans. EIC Selection Committee (2002)
10. Editor-in-Chief, IEEE Trans. on Circuits and Systems, Part-I: Regular Papers, Jan. 2004-Dec. 2005
11. NSF Panel, 1993, Feb. 2002, Apr. 2003, Dec. 2004, March 2010, Oct. 2011, May 2012, May 2014, June 2014, May 2015, 2017
12. (Biomedical Imaging/Engineering) NIH R43/44 Panel, March 2011, March 2012
13. Judge, Davidson Fellowship Selection, 2011, 2012
14. Associate Editor, IEEE Trans. on Circuits and Systems (1990-1991)
15. Associate Editor, IEEE Transactions on Signal Processing (1993-1995)
16. Associate Editor, IEEE Circuits and Systems Trans., Part II: Analog and Digital Signal Processing, 1995-1997
17. Associate Editor, IEEE Trans. on VLSI Systems, 1997-9
18. Associate Editor, IEEE Signal Processing Letters, 1997-1999
19. Editor, Journal of VLSI Signal Processing, 1993-
20. Guest Editor, Special Issue on 1995 IEEE VLSI Signal Processing Wksp. for the Journal of VLSI Signal Processing, Vol. 16(1), May 1997
21. Guest Coeditor, Special Issue on "Theory and Application of Filter Banks and Wavelets", IEEE Trans. on Signal Processing, April 1998
22. Guest Editor, Special Issue on ASAP Conf. 1996 for the Journal of VLSI Signal Processing, Vol. 19(2), June 1998

23. Guest Co-Editor, Special Issue on Interconnect for the Journal of Analog Circuits and Signal Processing, Vol. 31, No. 3, June 2002
24. Guest Co-Editor, Special Issue on SIPS-2002 for the Journal of VLSI Signal Processing
25. Guest Co-Editor, Special Issue on Signal Processing for Broadband Access Systems: Techniques and Implementations for the EURASIP Journal on Applied Signal Processing (Dec. 2003)
26. Associate Editor, IEEE Trans. on Circuits and Systems, Part-II: Analog and Digital Signal Processing, 2002-2003
27. Member, Editorial Board, IEEE Signal Processing Magazine (2003-2006)
28. General Chair, IEEE Signal Processing Systems (SiPS): Design and Implementation Workshop, Oct. 2002
29. International Coordination Chair of IEEE APCCAS 2004, Tainan, Taipei
30. Technical Program Cochair, IEEE VLSI Signal Processing Workshop, Oct. 1995
31. Technical Program Cochair, Applications Specific Array Processors, Sept. 1996
32. Track Chair, Parallel Processing Track, IEEE ISCAS - 1993
33. Track Chair, DSP Processing Track, IEEE ISCAS - 1995
34. Track Chair, VLSI Track, IEEE ISCAS - 2002, 2003
35. Track Chair, VLSI Track, Midwest Symp. on VLSI, 2004
36. Technical Program Committee, IEEE HOST, 2016, 2017
37. Technical Program Committee: IEEE VLSI SP Workshop, 1990 - 96
38. Technical Program Committee: IEEE SiPS Workshop, 1997 - 2004, 2010, 2012
39. Technical Program Committee: IEEE ICASSP 1991 - 2004
40. Technical Program Committee, European Signal Processing Conference (EUSIPCO), 2008
41. Technical Program Committee: IEEE ISCAS 1992 - 93, 1995 - 2002, 2010, 2012 [Track-Chair: 1993 (Parallel Processing), 1995 (DSP), 2002, 2003 (VLSI)]
42. Technical Program Committee, Int. Workshop on System-on-Chip (2003, 2004, 2005)
43. Technical Program Committee, Int. Symp. on System-on-Chip (2003, 2004)
44. Technical Program Committee: IEEE Symp. on Computer Arithmetic, 1997, 2016
45. Technical Program Committee: IEEE ASP-DAC Conference, 1998, 2000

46. Technical Program Committee: ASAP Conf., 1992 - 96, 2002, 2004
47. Technical Program Committee: Great Lakes Symp. on VLSI, 1996, 1999, 2000, 2001, 2003, 2004, 2005, 2006
48. Technical Program Committee: Int. Conf. Electronics, Circuits and Systems (IECS), Rhodes (Greece), 1996
49. Technical Program Committee: Int. Workshop on Image and Signal Processing, Advances in Computational Intelligence, 1996
50. Technical Program Committee: IEEE Wksp. on VLSI for Communications, 1993
51. Technical Program Committee: Workshop on CORDIC-related Paradigm to Signal Processing Problems, 1998
52. Technical Program Committee: INDICON-2004 (Kharagpur, India)
53. Registration Chair, 1993 IEEE ICASSP Conference (Minneapolis)
54. Advisory Board, 2014 International Conference on VLSI and Signal Processing, Jan. 2014, IIT Kharagpur, India
55. Advisory Board, 1st International Conference on Automation, Control, Energy and Systems, Feb. 2014, Hooghly, India
56. Session Chair, IEEE EMBC Conference, 2012, 2015
57. Session Chair, Asilomar Conference - 1998, 2001, 2012
58. Session Chair, IEEE ICASSP 91, 96, 99, 00, 2015
59. Session Chair, IEEE ISCAS 1992, ISCAS 1993, 1995, 1996, 1997, 1998, 2001, 2002
60. Session Chair, IEEE VLSI Signal Processing Workshop, 1992, 1993, 1995, 1996
61. Session Chair, IEEE SiPS Workshop, 1997, 2001
62. Session Chair, IEEE Workshop on VLSI in Communications, 1993
63. Session Chair, 3rd Int. Conf. on Image and Signal Processing, 1995
64. Session Chair, ASAP Conf., Aug. 1994, 1996
65. Session Chair, IEEE ASP-DAC Conf., Jan. 2000

Tutorials, Panels, Invited Keynote Talks

1. Co-Presenter, Tutorial Workshop on "VLSI DSP Synthesis" at IEEE ICASSP 92 (also available as an *IEEE Video Tutorial*)
2. Presenter, Tutorial on DSP Architectures and Synthesis at VLSI'95
3. Organizer and Copresenter, Tutorial on DSP Architectures and Synthesis at IEEE ISCAS 95
4. Organizer and Copresenter, Tutorial on Design of High-Performance DSP Systems at IEEE ISCAS 96
5. Organizer and Copresenter, Tutorial on High-Performance Video DSP Systems at IEEE ISCAS 97
6. Organizer and Copresenter, Tutorial on Low-Power Multimedia DSP Systems at IEEE ICASSP98
7. Presenter, Tutorial on VLSI Architectures for Video and Data Communications at IEEE ISCAS98
8. Copresenter, Tutorial on Design Methodologies for Low Power Signal Processing, IEEE Int. Symp. on Low Power Electronics and Design, Monterey, Aug. 1998
9. Organizer and presenter, Tutorial on Design of Low-Power Multimedia DSP Systems at IEEE ISCAS 1999
10. Panelist, Future of Digital Signal Processing, ISCAS'96
11. Plenary Talk Speaker, ICVC-97
12. Invited Speaker, IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
13. Panelist, "Single Chip or Multiple Chips", IEEE CAS/COM Workshop on ADSL, Princeton, July 1999
14. Keynote Talk Speaker, 2001 IEEE SiPS Workshop (Antwerp, Belgium)
15. Invited Speaker, 2001 System-on-Chip Conference (Tampere, Finland)
16. Panlist, 2001 System-on-Chip Conference (Tampere, Finland)
17. Invited Speaker, 2003 IEEE SiPS Workshop, Seoul, Korea (August 2003)
18. Tutorial Copresenter, IEEE Portable 2007 Conf.
19. Tutorial Copresenter, IEEE ISCAS 2007 Conf.

20. Keynote Talk, ACM Great Lakes Symposium on VLSI, 2014
21. Tutorial Presentation on Hardware Security, IEEE ISCAS, 2017
22. Keynote Speaker, Workshop on Processing for Communication and Intelligent Information (PCII), Fudan University, Shanghai, June 2017

Technical Society Activities: Reviews

1. Ph.D. Thesis Committee, Univ. of Grenoble, France, Feb. 1995
2. Ph.D. Thesis Committee, I.I.T. Bombay, India, Feb. 1998
3. , Ph.D. Thesis Committee, KJIST Univ., Korea (2003)
4. Ph.D. Thesis Committee, Linkoping Univ., Sweden (2003)
5. Ph.D. Thesis Committee, Univ. of Toronto (2003)
6. Ph.D. Thesis Opponent, Linkoping University, Sweden (2004)
7. Ph.D. Thesis Opponent, Lund University, Sweden (2012)
8. Ph.D. Thesis Examiner, Univ. Canterbury, New Zeland, 2015
9. Ph.D. Thesis Examiner and Committee, Univ. Calgary, Canada, 2015
10. Book Reviewer, Kluwer Academic Press, 1990-, McGraw Hill, 1992-, IEEE Press, 1993-, IEEE Comp. Society Press (1994-)
11. Reviewer Swiss National Science Foundation (2013)
12. Italian Research Assessment Exercise VQR 2004-2010 (2013)
13. Reviewer, NSF Proposals (1989-), ARO Proposals (1992-), UK EPSRC
14. Reviewer, IEEE Proceedings, 1986-
15. Reviewer, IEEE Transactions on Circuits and Systems, 1986-
16. Reviewer, IEEE Transactions on Circuits and Systems, Part II, 1993-
17. Reviewer, IEEE Transactions on Circuits and Systems, Part I, 1996-
18. Reviewer, IEEE Transactions on Computers, 1987-
19. Reviewer, IEEE Journal of Solid State Circuits, 1990-
20. Reviewer, IEEE Trans. on Acoustics, Speech, and Signal Processing, 1989-
21. Reviewer, IEEE Trans. on Parallel and Distributed Systems, 1991-
22. Reviewer, IEEE Trans. on Circuits and Systems for Video Technology, 1991-
23. Reviewer, IEEE Trans. on VLSI Systems, 1993-
24. Reviewer, IEEE Trans. on Image Processing, 1994-
25. Reviewer, IEEE Trans. on Speech and Audio Processing, 1997-

26. Reviewer, IEEE Trans. on Vehicular Technology, 1996-
27. Reviewer, IEEE Signal Processing Letters, 1995-
28. Reviewer, IEEE Signal Processing Magazine, 1997-
29. Reviewer, IEEE Trans. on Communications, 1996-
30. Reviewer, IEEE Journal of Selected Areas in Communications, 1999-
31. Reviewer, IEEE Trans. on Computer Aided Design, 1999-
32. Reviewer, IEEE Trans. Medical Imaging, 2013-
33. Reviewer, IEEE Trans. Biomedical Engineering, 2014-
34. Reviewer, Nature Pediatrics, 2015
35. Reviewer, PLOS One, 2015
36. Reviewer, NeuroImage, 2016
37. Reviewer, IEEE Trans. NanoBio Science, 2017-
38. Reviewer, Royal Society Interface, 2015
39. Reviewer, Clinical EEG and Neuroscience, Sage, 2014-
40. Reviewer, EURASIP Journal on Advances in Signal Processing, 2014-
41. Reviewer: IEICE
42. Reviewer, Elsevier Signal Processing, 2012
43. Reviewer, ACM TODAES, 1996-
44. Reviewer, Journal of Parallel and Distributed Computing, 1988-
45. Reviewer, Journal of VLSI Signal Processing (Kluwer Academic), 1988-
46. Reviewer, Journal of System Integration (Kluwer Academic), 1991-
47. Reviewer, Multidimensional Systems and Signal Processing (Kluwer), 1994-
48. Reviewer, The Computer Journal, 1993-
49. Reviewer, Applied Mathematics Letters, 2002-
50. Reviewer, Int. Journal of Circuits, Systems and Computers, 1997
51. Reviewer, IEE Proceedings, Circuits, Devices and Systems, 1994-
52. Reviewer, IEEE International Symposium on Circuits and Systems, 1986-

53. Reviewer, Int. J. of Computers and Mathematics, 2001-
54. Reviewer, IEEE Int. Conf. on Acoustics, Speech, and Signal Processing, 1990-
55. Reviewer, IEEE Int. Symposium on Computer Architecture, 1990-
56. Reviewer, IEEE Workshop on VLSI Signal Processing, 1990-
57. Reviewer, IEEE International Parallel Processing Symposium, 1991-
58. Reviewer, IEEE Asia Pacific Conference on Circuits and Systems, 1992 -
59. Reviewer, ACM/IEEE Design Automation Conference, 1991-
60. Reviewer, IEEE Int. Conf. on Image Processing, 1995-
61. Reviewer, International Conference on Parallel Processing, 1988-
62. Reviewer, Int. Conference on Applications Specific Array Processors, 1990-
63. Reviewer, Hawaii International Conference on System Sciences, 1991
64. Reviewer, European Conf. on Circuit Theory and Design, 1993-
65. Reviewer, Midwest Symp. on Circuits and Systems, 1995-
66. Reviewer, Int. Conf. on VLSI Design, 1994-
67. Reviewer, European Signal Processing Conference (EUSIPCO), 1998
68. Reviewer, IEEE Globecom Conf., 2001, 2003
69. Reviewer, Percom 2004
70. Reviewer, VTC-2004
71. Reiewer, IEEE ECCTD 2009
72. Reviewer, IEEEE SiPS Workshop -2009, 2012

Technical Society Activities: Membership

1. Fellow of IEEE – Circuits and Systems Society
2. Fellow , IEEE – Signal Processing Society
3. Fellow, IEEE – Computer Society
4. Member, Technical Committee on VLSI Systems and Applications, IEEE CAS Society (Chair-Elect: 2000-2002, Chair: 2002-2004)
5. Member, Tech. Cmt. on Visual Signal Processing and Communications, IEEE CAS Society
6. Member, Tech. Cmt. on Digital Signal Processing, IEEE CAS Society
7. Founding Member, Tech. Cmt. on Nanoelectronics and Gigascale Integration, IEEE CAS society
8. Member, Technical Committee on Design and Implementation of SP Systems, IEEE Signal Processing Society (1990-)
9. Member, Technical Committee on VLSI, IEEE Computer Society

University Activities

1. Director of Graduate Studies (2008-2011)
2. MN Future Proposal Review Panel (2013)
3. Graduate Teaching Award Selection Committee (2014, 2015, 2016)
4. Dossdall Fellowship Evaluation Committee (2012)
5. Member, Graduate Education Committee, Graduate School (2012)
6. Chair, Graduate Standards Committee (2007-2008)
7. Member, Graduate Standards and Program Committee, Electrical Eng. Dept. (1989-90) (1997-98) (2003-2004)
8. Member, Faculty Recruiting Committee of Electrical Eng. Dept. (1990-95) (1998-99)(2002-03)(2004-2005)(2005-2006) (2011-2012) (2012-2013)
9. Member, Faculty Promotion and Tenure Committee of Electrical Eng. Dept. (1995-96) (1998-99) (2013-14)
10. Member, Ph.D. Written Qual. Exam. Committee (1989, 1990, 1998, 2002-3, 2004-5, 2009-10, 2012-13) (2015)

11. Member, Space Committee (2014-2016)
12. Instructor for Oral Presentation Training (1990)
13. Member, *Adhoc* Committee on Ph.D. Written Examination, 1993
14. Chair-Systems and Hardware Track for Univ. Digital Summit (1997)

Post Doctoral Fellows and Visitors Supervised

1. Kazuhito Ito, Currently Professor, University of Saitama, Japan (1992-1993)
2. Ching-Yi Wang, Currently with Boston Scientific (1993-1996)
3. Luis Montalvo, Currently with Technicolor, France (1995-1996)
4. Michael Zervakis, Currently Professor at Technical Univ. of Crete, Chania, Crete, Greece (1996)
5. Steve Summerfield, Formerly with Univ. of Warwick, Coventry, U.K., Currently with Huawei, London (1997)
6. Hiroshi Suzuki, Curretly Senior Manager at Broadcom Limited, Irvine, CA (1997-1999)
7. Javier Valls, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
8. Trini Sansaloni, Currently Professor at Universidad Politecnica de Valencia, Valencia, Spain (1999)
9. Yuke Wang, Currently Patent Lawyer (Dallas, Texas) (1999)
10. Jin-Gyun Chung, Currently Dean of Engineering, Chonbuk National Univ., Korea (2001)
11. Chester Park, Currently Asst. Prof. at Konkuk University, Korea (2005)
12. Chunlei Xia (Shanghai, China, 2006)
13. Mario Garrido, Currently Asst. Professor at Linkping University, Sweden (2007)
14. Hemant Patil, Currently Assoc. prof. at DA-IICT, Gandhinagar, India (2009)
15. Xiaoping Li, Nanjing Univ, China (2010)
16. Sayed Ahmad Salehi, Currently PhD student at UMN (2011-12)
17. Yun-Nan Chang, Currently Professor at National Sun Yat-Sen Univ., Taiwan (2012)
18. Mojtaba Bandarabadi, Currently with Inselspital Bern, Switzerland (2012) (coadvised by Dr. Tay Netoff)
19. Abdolreza Rashno, Predoctoral Visitor from Isfahan University of Technology, Iran, 2016-2017

Ph.D. Theses Supervised

1. Lori E. Lucke, "Applying Parallel Processing Techniques to Digital Signal Processing Algorithms and Architectures for High Level VLSI Synthesis", December 1992

[Currently Fellow, Minnetronix Corp, St. Paul]
2. Ching-Yi Wang, "MARS: A High-Level Synthesis Tool for Digital Signal Processing Architecture Design", December 1992

[Currently with Boston Scientific, St. Paul]
3. Naresh R. Shanbhag, "Design of Pipelined VLSI Adaptive Digital Filters with Relaxed Look-Ahead", July 1993

[Currently Jack Kilby Professor at Univ. of Illinois at Urbana]
4. H.R. Srinivas, "Floating Point Computer Arithmetic Architectures", September 1994

[Currently Senior Manager, Broadcom limited, Irvine, CA]
5. K.J. Raghunath, "Pipelined STAR RLS Adaptive Filters", October 1994

[Currently Principal Architect, Ikanos Communications, NJ]
6. Jin-Gyun Chung, "Pipelined IIR Lattice and Wave Digital Filters", November 1994

[Currently Professor at Chonbuk National University, Chonju, South Korea]
7. Tracy C. Denk, "Retiming, Folding and Register Minimization", July 1996
8. Janardhan H. Satyanarayana, "Design of Low-Power DSP Systems", March 1998

[Currently with Intel, PA]
9. Ahmed Shalash, "Architecture and System Design for Digital Subscriber Loop Communications", June 1998

[Currently Professor at Cairo University, Egypt]
10. Leilei Song, "Low-Power VLSI Architectures for Finite-Field Applications", June 1999

[Currently at Intel, CA]

11. Yun-Nan Chang, "Low-Power Bit-Serial and Digit-Serial DSP Systems", June 1999
[Currently Professor at National Sun Yat-Sen University, Kaohsiung, Taiwan]
12. Jun Ma, "Pipelined RLS Adaptive Filters", July 1999
13. Martin Kuhlmann, "High-Performance Low-Power Arithmetic, Architectures and Circuits", Dec. 1999
[Currently Director at MaxLinear, Irvine, CA]
14. Vijay Sundararajan, "Performance Optimization Methodologies for Design of Digital VLSI Systems", Jan. 2000
[Currently Associate Technical Director at Broadcom Inc., San Jose, CA]
15. Zhongfeng Wang, "High-Performance and Low-Cost VLSI Design of Turbo Decoders", Aug. 2000
[Currently Full Professor at Nanjing University, China]
16. Robert A. Freking, "Structural Strategies for High-Performance Undelimited-Codeword Source Coding", October 2000
[Currently with MIT Lincoln Laboratories]
17. William L. Freking, "Algorithms and Architectures for High-Performance Public-Key Cryptography Systems", October 2000
[Currently with MIT Lincoln Laboratories]
18. Lijun Gao, "Architecture Design and Mapping of DSP Systems", Feb. 2001
[Currently with Analog Devices, Boston]
19. Zhipei Chi, "High Performance, High Speed VLSI Architectures for Wireless Communication Applications", June 2001
[Currently with Marvell Technology Group, San Jose, CA]
20. Tong Zhang, "Efficient VLSI Architectures for Error Correction Coding", June 2002
[Currently Full Professor of ECSE Dept., R.P.I., Troy, NY]
21. Yanni Chen, "Low-Complexity High-Speed VLSI Architectures for Error-Correction Decoders", June 2003
[Currently at Apple, CA]
22. Junjin Kong, "Classical and Quantum Convolutional Codes: Design and Implementation", Feb. 2005
[Currently a "Master" at Samsung, S. Korea]

23. Xinmiao Zhang, "Architectures for Error Control Coders and Cryptography Systems", June 2005
[Tenured Assoc. Prof. at Ohio State Univ.]
24. Yongru Gu, "VLSI Architectures for High-Speed Transceivers", July 2005
[Currently at Inplay Tech, Irvine]
25. Jun Tang, "Architectures for OFDM Based Ultra Wideband Systems", July 2006
[Currently with Broadcom, Irvine, CA]
26. Sangmin Kim, "Efficient VLSI Architectures for Error Control Coders", Oct. 2006
[Currently with Qualcomm, San Diego]
27. Jianhung Lin, "Algorithm and Architectures for Next Generation Multimedia Systems", Jan. 2007
[Currently with Maxlinear, Irvine]
28. Yuping Zhang, "VLSI Architectures for Turbo Code Decoder, LDPC Code Decoder and List Sphere Decoder", May 2007
[Currently with Marvell Technology Group, CA]
29. Chao Cheng, "High-Speed Low-Cost VLSI DSP Algorithms Based on Novel Fast Convolutions and Look-Ahead Pipelining Structures", May 2007
[Currently with Qualcomm, San Jose, CA]
30. Aaron E. Cohen, "Architectures for Cryptography Accelerators" September 2007
[Currently with Naval Research Lab, Washington, DC]
31. Daesun Oh, "Low Complexity VLSI Architectures for LDPC Decoders", May 2008
[Currently with Samsung, S. Korea]
32. Jie Chen, "Efficient VLSI Architectures for High-Speed Ethernet Transceivers", Aug. 2008
[Currently Manager at Marvell Technology Group, San Jose, CA]
33. Renfei Liu, "Error Control Algorithms and Architectures for Reliable DSP Systems", Nov. 2010
[Currently with Broadcom Corp., Irvine, CA]
34. Yun Sang Park, "Reduced-Complexity Epileptic Seizure Prediction with EEG," Jan. 2012 (Coadvised by Prof. Theoden I. Netoff)
[Currently with Samsung, S. Korea]

35. Hua Jiang, "Digital Logic and Signal Processing Computations with Molecular Reactions," May 2012 (Coadvised by Prof. Marc D. Riedel)
[Currently with Netflix, CA]
36. Manohar Ayinala, "Low-Power Architectures for Signal Processing and Classification Systems," July 2012
[Currently with Intel, Allentown, PA]
37. Chuan Zhang, "Low-Latency Low-Complexity Channel Decoder Architectures for Modern Communication Systems," December 2012
[Currently Associate Prof. with Southeast University, China]
38. Te-Lung Kung, "Synchronization and Coding in Wireless Communication Systems," September 2013
39. Sohini Roychowdhury, "Automated Segmentation and Pathology Detection in Ophthalmic Images," July 2014
[Currently with Volvo, Mountain View, CA]
40. Yingjie Lao, "Authentication and Obfuscation of Digital Signal Processing Integrated Circuits," July 2015
[Currently Assistant Professor at Clemson University, South Carolina]
41. Bo Yuan, "Algorithm and Architecture for Polar Codes Decoder," July 2015
[Currently Assistant Professor at City University of New York]
42. Tingting Xu, "Biomarkers for Mental Disorders from Neuroimaging Data," December 2016
[Currently with Ad Colony, Seattle]
43. Yin Liu, "Digital Signal Processing and Machine Learning System Design using Stochastic Logic," July 2017
[Currently with Microsoft, Redmond, WA]
44. Sayed Ahmad Salehi, "A Framework for Computing Discrete-Time Systems and Functions using DNA," July 2017 (Coadvised by Prof. Marc D. Riedel)
[Currently with Utah Valley University]
45. Zisheng Zhang, "Approaches to Feature Identification and Feature Selection for Binary and Multi-Class Classification," July 2017
[Currently with irhythm, San Francisco]

M.S. Projects Supervised

1. Gregory S. Munson, "Finite Precision Effects in Scattered and Clustered Look-Ahead Pipelined Recursive Digital Filter Implementations", June 1989
[Currently with JAMF Software, Eau Claire, WI]
2. Jim Malaney, "Design of a Programmable Digital Filter", November 1989
[Manager at GE Healthcare, Madison, Wisconsin]
3. Lai Q. Pham, "Roundoff Error in Digital Filters using Redundant Numbers", November 1989
4. Syed Babar Raza, "Reduction of Hardware Overhead in Recursive Filters by Interleaving", January 1991
5. Joo-Sang Lee, "A New Approach For Design Of Data Format Converter Architectures Using Register Allocation", May 1991
[Currently with Micron Technology, Dallas, TX]
6. H.R. Srinivas, "High-Speed VLSI Arithmetic Processor Architectures Using Hybrid Number Representation", July 1991
[Currently Senior Manager at Broadcom, Irvine, CA]
7. N. Iyer, "iSchematic: An Automatic Schematic Generator for OCT 5.0 Data Base", September 1991
8. Andrew P. Brown, "Applications of Circuit Retiming to DSP Architecture Design", October 1991
[Currently with MBA Engineering, MN]
9. J.-G. Chung, "Synthesis of Pipelined Lattice IIR Digital Filter", November 1991
[Currently Dean of Engineering, Chonbuk National Univ., S. Korea]
10. Gireesh Shrimali, "Fast Arithmetic Coder Architectures", June 1993
11. Wayne C. Amendola, Jr., "VLSI Implementation of a 200 MHz 16X16 Redundant Digit Multiplier and a 125 MHz 16X16 Booth-Encoded Redundant Digit Multiplier", June 1993
[Currently Data Analyst, Capital One, CA]
12. Bin Fu, "VLSI Design Advances in Arithmetic Coding", May 1995
13. Santosh Misra, "CDMA Based Mobile Communication Systems", May 1995
[Indian Administrative Service (IAS), Officer, Govt. of Chhattisgarh, India]

14. Darren Pearson, "Low Power Strategies for VLSI Implementation of Digital Filters", May 1995
[Currently Instructor at St. Paul College, MN]
15. Surendra Jain, "Efficient VLSI Architectures for Finite Field Arithmetic", June 1995
[Currently Venture Capitalist, Bengaluru, India]
16. Yun-Nan Chang, "High-Level DSP Synthesis using Heterogeneous Functional Units", June 1995
[Currently Professor at National Sun Yat-Sen University, Taiwan]
17. Yuet Li, "STAR Adaptive Lattice Recursive Least Square Filters", February 1996
[Currently Associate Technical Director at Broadcom, Fremont, CA]
18. Chong Xu, "Power-Speed Reconfigurable FIR Filters", February 1996
[Currently with Intel, CA]
19. David A. Parker, "Low-Area/Power Parallel FIR Filters", May 1996
[Currently Director at Altera, CA]
20. Mayukh Majumdar, "Low-Area Data Format Converters", June 1996
21. Leilei Song, "Efficient Bit-Serial Finite Field Multipliers", June 1996
[Currently Senior Manager at Marvell]
22. John Bratt, "VHDL Interface for MARS DSP Synthesis System", June 1996
[Currently with AMD, CO]
23. Hojun Kim, "Coefficient Optimization in Pipelined IIR Digital Filters", July 1996
[Currently with Telematics, CA]
24. Mousumi Gayen, "ILP Scheduling with Processor Interconnection", Jan. 1997
25. Nikhil Sarpotdar, "Radix-2 Division and Square Root Algorithms: Study and Implementation", July 1997
26. William Ho, "Power Efficiency of the Carry-Select Adder", August 1997
[Currently with a Startup, CA]
27. Ashish Karandikar, "Low-Power and High-Performance Static Random Access Memory", December 1997
[Currently Vice President, Nvidia]
28. Zhipei Chi, "Pipelined Single and Multi-Channel Lattice RLS Adaptive Filters", Sept. 1998
[Currently with Marvell, CA]

29. Nidish Kamath, "Scheduling of DSP Algorithms for Low-Power Design", Jan. 1999
[Currently Technologist, Bay Area, CA]
30. Dhiraj Kumar, "Performance Tradeoffs of DCT Architectures in Xilinx FPGAs", April 1999
[Currently Senior Director at Paypal, NY; Previously Sales Executive, Facebook]
31. Ziyu Li, "DLMS Adaptive FIR Filter: Bit-Serial Systolic Array VLSI Implementation", July 1999
[Predictive Modeling Analyst at Travelers, MN]
32. Robin Bansal, "Optimized Power and Delay Solutions for Digital CMOS Circuits by Transistor Reordering using HEAT", August 1999
[President and CEO, Bansi Holdings, PA]
33. Ru-Guang Chen, "Double Error Correction on Residue Number System", Feb. 2000
[Currently with Amazon, CA]
34. Bibhudatta Sahoo, "A Low Power Correlator", Aug. 2000
[Currently Associate Professor in Amrita University, Bengaluru, India]
35. Siwei Chen, "Minimal Switching Activity Schedules for Various FIR Filters", Aug. 2000
[Currently with Focaltech, Providence, RI]
36. Wenhao Wu, "VLSI Design and Implementation of Two Viterbi Decoders", Aug. 2000
[Currently with Intel, CA]
37. Karuna Prasad, "Power Analysis of 4-2 and 5-2 Compressors", Jan. 2001
38. Aaron E. Cohen, "VLSI Architectures for RSA," June 2004
[Currently with Naval Research Lab, Washington, DC]
39. Saurabh Jain, "Low-Complexity Pipelined-Parallel Decision Feedback Decoder (PDFD) for 1 Gbps Ethernet", August 2004
[Currently with Marvell, CA]
40. Lina Long, "A VLSI Implementation for Viterbi Decoder in Ultra Wide-band System", March 2005
[Currently with Cisco, CA]
41. Manoj Yadav, "LDPC Decoder for DVB System", May 2005
[Currently Manager at Marvell, CA]

42. Renfei Liu, "VLSI Architectures for Viterbi Decoders," May 2007
[Currently at Broadcom, Irvine, CA]
43. Daesun Oh, "LDPC Decoder Architectures," Feb. 2008
[Currently with Samsung, S. Korea]
44. Jie Chen, "Architectures for 10-Gigabit Ethernet," Feb. 2008
[Currently Manager at Marvell, CA]
45. Priyadharshini Vijayakumar, "Timing Variations in Digital Filters with Supply Voltage Variations", Aug. 2008
[Currently with Intel, CA]
46. Prashant Metkar, "Improved Approach for Calculating Model Parameters in Speaker Recognition using Gaussian Mixture Models", May 2009
[Currently Financial Engineer in Pune, India]
47. Jaime Rivera, "Research for the Development of an Apparatus To Help Prevent Sudden Infant Death", May 2009
[Currently with Eagle Properties, Rochester, MN]
48. Xiaoming Zhu, "Lung Sound Separation by Independent Component Analysis", June 2009
[Currently at Marvell, CA]
49. Yun-Sang Park, "Seizure Prediction by Support Vector Machine Classification," Jan. 2010
[Currently with Brown Univ as Postdoc]
50. Yingbo Hu, "Subthreshold Circuit Design", August 2010
[Currently with Maxim, CA]
51. Manohar Ayinala, "High-Throughput VLSI Architectures for CRC/BCH Encoders and FFT Computations", Nov. 2010
[Currently with Intel, Allentown, PA]
52. Lan Luo, "Postprocessing of Seizure Prediction by Kalman Filter", May 2011
[Currently with Intel, Oregon]
53. Te-Lung Kung, "Frame Start Synchronization in OFDM System," September 2011
54. Michael Brown, "A Low-Complexity Seizure Prediction Algorithm," November 2011
[Currently with Digi Wireless Devices, MN]

55. Chuan Zhang, "Polar Code Decoder Architectures," April 2012
[Currently Associate Prof. at Southeast University, China]
56. Tingting Xu, "Schizophrenia Classification from MEG," May 2013
[Currently PhD Candidate at UMN]
57. Manikandan Palani, "EEG Data Compression," May 2014
[Currently with Qualcomm, Denver, CO]
58. Aravinth Chinnapalanichamy, "Serial and Interleaved FFT Architectures for Real Signals," Jan. 2015
[Currently with Nvidia]
59. Sandhya Koteswara, "Obfuscated FFT Architecture," Feb 2015
[Currently PhD student, UMN]
60. Sayed Ahmad Salehi, "DNA Computing," April 2015
[Currently PhD student, UMN]
61. Yingjie Lao, "Removing Redundancies of Fast Fourier Transform Computations," July 2015
[Currently with Clemson Univ., South Carolina"])
62. Goutham N. C. Shanmugam, "Obfuscated Real FFT Architecture," August 2015
[Currently with ARM, Austin, TX]
63. Vaishnavi Santhapuram, "Timing Induced Error Analysis for Wallace Tree Multipliers," Oct. 2015
[Currently with Intel, CA]
64. Vishal Vijayakumar, "Artery/Vein Classification in Fundus Images," 2016
[Currently Ph.D. student at the University of Minnesota]

Graduate Advisees

I am currently advising following Graduate Students.

1. Shu-Hsien (Dennis) Chu (PhD) (Coadvised by Prof. Christophe Lenglet)
2. Sandhya Koteswara (PhD)
3. Bhaskar Sen (PhD)
4. Satya Venkata Sandeep Avvaru (MS/PhD)
5. Xingyi Liu (Ph.D.)
6. Anoop Koyily (MSEE)
7. Nanda Kumar Unnikrishnan (MSEE)

New Course Development

1. I developed two new classes "VLSI Digital Signal Processing (EE 5329)" and "Digital Signal Processing Structures for VLSI" (EE-5549) in Spring 1989/Spring 1990.
2. I developed and taught the "VLSI Low-Power and Digital Video Systems (EE 8451)" Course in Fall 1997.
3. I developed and taught the "Digital Arithmetic, Error Control Coding and Cryptography Architectures" (EE 5953)" Course in Winter 1999
4. Developed and taught a new class "VLSI Communications Systems" in Spring-2003 (EE-8950)
5. Introduced and Taught "Teaching Experience in EE" class (EE-8920) (2010-11) (Spring 2012) (Spring 2014)
6. Introduced and Taught "Ethics and Professional Conduct in EE" (EE-8925) (Fall-2010) (Spring 2011) (Spring 2013) (Spring 2015)
7. I taught a new graduate course on Digital Signal Processing Applications (Spring 2015). Applications from neuroengineering and biomedical signal analysis were emphasized.

Non-Conference Invited Talks since 1992

1. "Critical Path Reduction by Unfolding and Folding Techniques," NEC Computer & Communication Lab., Japan, April 1992
2. "High-Speed Digital Signal Processors", NEC Computer & Communication Lab., Japan, May 1992
3. "Dedicated VLSI Digital and Signal Processors", Toshiba (Japan), May 1992
4. "Dedicated VLSI Digital and Signal Processors", Tokyo Inst. of Technology (Japan), May 1992
5. "Dedicated VLSI Digital and Signal Processors", NTT Transmission Laboratory (Japan), May 1992
6. "Dedicated VLSI Digital and Signal Processors", Tohoku University, Sendai (Japan), May 1992
7. "VLSI Wavelet Architectures", NEC Computer & Communication Lab., Japan, June 1992
8. "Dedicated VLSI Digital and Signal Processors", Indian Institute of Technology, Delhi (India), July 1992
9. "Dedicated VLSI Digital and Signal Processors", Swiss Federal Institute of Technology, Zurich (Switzerland), August 1992
10. "Register Minimization in DSP Architectures", NCUBE Corporation, Bangalore, India, December 1993
11. "High-Speed Multiplication and Addition", IEEE Section, Bangalore, India, December 1993
12. "Pipelined VLSI IIR and Adaptive Digital Filters", Indian Institute of Science, Bangalore, India, December 1993
13. "High-Level Transformations for DSP Synthesis", Indian Institute of Science, Bangalore, India, December 1993
14. "Pipelined VLSI IIR and Adaptive Digital Filters", Department of Electrical Engineering Seminar, University of California, Davis, August 1994
15. "VLSI Architectures for Approximation Algorithms", Dept. of Electrical Engineering and Computer Sciences, University of California, Berkeley, August 1994
16. "Dedicated VLSI Digital Signal Processors", Department of Electrical and Computer Engineering, University of Iowa, Iowa City, August 1994
17. Lectures on "VLSI Digital Signal Processing," Central Electronics Engineering Research Institute (CEERI), Pilani, India, Dec. 1994

18. Four Lectures on "VLSI Digital Signal Processing," Center for Development of Advanced Computing, Pune, Feb. 1995
19. "High-Performance VLSI Digital Signal Processing," Indian Telephone Industries, Bangalore, March 1996
20. Two Lectures on "VLSI Digital Signal Processing," Indian Institute of Technology, Delhi, March 1996
21. "VLSI Digital Signal Processors", Univ. of Nottingham, U.K. (June 1995)
22. Lectures on "VLSI Digital Signal Processing", Delft Univ. of Technology, March and April 1996
23. "High-Performance VLSI Digital Signal Processing," National Tsing-Hua University, Hsinchu, Taiwan, October 17, 1996
24. "High-Performance VLSI Digital Signal Processing," National Chao-Tung University, Hsinchu, Taiwan, October 18, 1996
25. "High-Performance VLSI Digital Signal Processing," National Taiwan University, Taipei, Taiwan, October 21, 1996
26. "Design and Implementation of Dedicated and Programmable DSP Systems," Univ. of Ryukyus, Okinawa, Jan. 20, 1997
27. "Design and Implementation of Dedicated and Programmable DSP Systems," Kyushu University, Fukuoka, Jan. 21, 1997
28. "Design and Implementation of Dedicated and Programmable DSP Systems," LSI Division, Kawasaki Steel, Makuhari, Feb. 12, 1997
29. "Design and Implementation of Dedicated and Programmable DSP Systems," Technical Group Meeting of IEICE DSP, CAS and CS Groups, March 6, 1997, Hiroshima University
30. "Dedicated and Programmable VLSI Signal Processing Systems," Osaka University, Osaka, Japan, March 31, 1997
31. "Dedicated and Programmable VLSI Signal Processing Systems," Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, April 7, 1997 (IEEE CAS Distinguished Lecture)
32. "Dedicated and Programmable VLSI Signal Processing Systems," K-JIST, Kwanju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)
33. "Dedicated and Programmable VLSI Signal Processing Systems," Chonbuk National University, Chonju, Korea, April 8, 1997 (IEEE CAS Distinguished Lecture)

34. "Dedicated and Programmable VLSI Signal Processing Systems," Seoul National University, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)
35. "Dedicated and Programmable VLSI Signal Processing Systems," Daewoo Center, Seoul, Korea, April 9, 1997 (IEEE CAS Distinguished Lecture)
36. "Dedicated and Programmable VLSI Signal Processing Systems," Tohoku University, Sendai, Japan, April 18, 1997
37. "Dedicated and Programmable VLSI Signal Processing Systems," University of Southern California, Los Angeles, April 21, 1997 (Invited Talk)
38. "Dedicated and Programmable VLSI Signal Processing Systems," Inst. of Electronics, Academia Sinica, Beijing, China, June 2, 1997 (IEEE CAS Distinguished Lecture)
39. "Dedicated and Programmable VLSI Signal Processing Systems," Tsinghua University, Beijing, China, June 3, 1997 (IEEE CAS Distinguished Lecture)
40. "Dedicated and Programmable VLSI Signal Processing Systems," Tokyo Institute of Technology, Tokyo, Japan, June 30, 1997
41. "VLSI Architectures for High-Performance DSP Systems," University of California at Berkeley, Sept. 19, 1997
42. "Low-Power Digital Signal Processing for Multimedia Systems," University of Minnesota (Colloquium Talk), Oct. 9, 1997
43. "Low-Power VLSI Digital Signal Processing for Multimedia Systems," PLENARY TALK, IEEE Biannual Int. Conf. on VLSI Design and CAD, (ICVC), Oct. 12-15, 1997, Seoul, Korea
44. "Low-Power Arithmetic Components," Intel Corporation, Aug. 13, 1998
45. "Low-Power VLSI Digital Signal Processing Systems," Broadcom Corporation, Irvine, California, Aug. 14, 1998
46. "Low-Power Multimedia DSP Systems," ECE Colloq. talk at University of Illinois at Urbana, Sept. 15, 1998
47. "Low-Power Multimedia DSP Systems," Lucent Technologies, Bell Laboratories, Allentown, PA, Sept. 23, 1998
48. "Low-Power DSP Systems for Multimedia Communications," Texas Instruments, Dallas, Oct. 1, 1998
49. "Low-Power Multimedia DSP Systems," EECS Department, Univ. of California, Berkeley, Nov. 2, 1998
50. "Low-Power Multimedia DSP Systems," ECE Dept. Colloq. talk at North Carolina State University, Nov. 30, 1998

51. "Low-Power DSP Components for Multimedia Communications," National Univ. of Singapore, Feb. 22, 1999
52. Lectures on VLSI Signal Processing, Lund University, April-May 1999
53. Lectures on VLSI Signal Processing, KTH Royal Institute of Technology, Stockholm, May 1999
54. "Low-Power DSP Components for Multimedia Communications," IEEE Orange County section, Oct. 23, 2000
55. "Low-Power DSP Components for Multimedia Communications," U.C. Santa Barbara, April 20, 2001
56. "Low-Power DSP Components for Multimedia Communications," U.C.L.A., May 16, 2001
57. "Low-Power DSP Systems," NEC Corp., Japan, July 26, 2001
58. "Low-Power DSP Components for Multimedia Systems," Invited Talk at System-on-Chip Conference, Nov. 2001, Tampere
59. "VLSI Architectures for Digital Signal Processing Systems," Invited Talk at St. Cloud State, April 26, 2002
60. "Architectures for Broadband Communications Systems," Seoul National University, Seoul, Korea
61. "Design of High-Speed DSP Receivers," Lund University, Sweden, Sept. 2003
62. "Design of High-Speed DSP Receivers," Linkoping University, Sweden, Sept. 2003
63. "Architectures for Broadband Communications Systems," National Taiwan University, National Chiao-Tung University, National Cheng-Kung University, Taiwan, Nov. 2003
64. Presented a talk on "Data Fusion" on Dec. 20, 2006 at Medtronic, Inc.
65. Six lectures on DSP, Classification, VLSI Architectures at Medtronic, 2007
66. Presented a talk on "Electricity" to 4th Grade students at Providence Academy
67. Eminent Speakers Series Colloquim at the University of Virginia (Electrical Engineering Dept.) on Feb. 23, 2007
68. Series of 6 talks on Biomedical Signal Processing, Feature Extraction and Classification at Medtronic, April-May 2007
69. "Feature Extraction and Classification of Biomedical Signals," Indian Institute of Technology, Kharagpur, Jan. 3, 2008
70. "Feature Selection and Classification in Heart Sound," Tech Tuneup, UMN, June 2008

71. Talk on Seizure Prediction, U of M Neuroengineering Center, May 2009
72. Talk on EEG Signal Processing, Medtronic, June 2009
73. Talk on EEG Signal Processing, U.C. Berkeley, Aug. 2009
74. Talk on EEG Signal Processing, U of M Neuro Symp., Feb. 2010
75. "Signal Processing Device for Seizure Prediction," Neuroengineering Symp., University of Minnesota, Feb. 2, 2010
76. "Digital Signal Processing with Protein Molecules and DNA Strands," Information Systems Lab (ISL) Colloquium, Stanford, Nov. 9, 2010
77. "Digital Signal Processing with Protein Molecules and DNA Strands", CHESS Seminar, University of California, Berkeley, Nov. 10, 2010
78. "Seizure Prediction and Detection", Neuroengineering Symposium, Univ. of Minnesota, Feb. 9, 2011
79. "Processing Signals from EEG Electrodes and Protein Molecules: Convergence of DSP, Machine Learning, and Digital Design," Broadcom, June 7, 2011
80. "Digital Signal Processing for Embedded Communications and Biomedical Systems at Samsung", Korea, May 23, 2012
81. "Language Understanding of Schizophrenic Patients from MEG Data," Neuroengineering Symposium, Univ. of Minnesota, Feb. 16, 2012
82. "Ethics and Professional Conduct for Electrical Engineers," North Central Electrical Engineering Society (NCEES), Minneapolis, October 15, 2013
83. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Distinguished Speaker Series, ECE Department, University of Arizona, April 24, 2014
84. "VLSI Systems for Neurocomputing and Health Informatics," Proc. of 2014 ACM Great Lakes Symposium on VLSI, pp. 1-2, Houston, May 2014 (Keynote Talk)
85. "VLSI Computing of Digital Signal Processing Functions," University of Alberta, October 16, 2014
86. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders", Electrical Engineering Distinguished Talk, University of Alberta, Oct. 17, 2014
87. "Biomarkers and Brain Connectivity for Neurological and Psychiatric Disorders," Minneapolis VA Center, Sept. 28, 2015
88. "Molecular Machine Learning Systems," Workshop on Coding Techniques for Synthetic Biology at the University of Illinois, Urbana, October 30, 2015

89. "Fundus Image Analysis for Retinopathy using Signal Processing and Machine Learning," Univ. of Calgary, Dec. 14, 2015
90. "Network Analysis of Human Brain Connectivity in Psychiatric Patients and Healthy Humans," Neuroengineering/Neuroimaging Seminar, UMN, Feb. 18, 2016
91. "Architectures for Emerging Industrial Internet of Things: Reducing Energy and Enhancing Security," Invited Talk at 2016 NTU-MediaTek IC Design Workshop, Nanyang Technological University, Singapore, Aug. 10, 2016
92. "Brain, Biomedical, and Biomolecular Informatics: Convergence of Signal Processing, Machine Learning and Computing," ECE Colloquium Talk at University of Washington, Seattle, Oct. 25, 2016
93. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," ECE Colloquium Talk at Cornell, Oct. 31, 2016
94. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," IEEE Student Branch, Indian Institute of Technology, Kharagpur, India, Dec. 26, 2016
95. "Computing Signal Processing and Machine Learning Functions using DNA," Indian Institute of Technology, Bhubaneswar, India, Jan. 4, 2017
96. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," S O A University, Bhubaneswar, India, Jan. 6, 2017
97. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Technology - Madras, Chennai, India, Jan. 9, 2017
98. "Internet of Things: Information Analytics, Energy-Efficiency and Hardware Security," Indian Institute of Science, Bengaluru, India, Jan. 10, 2017
99. "Authentication and Functional Obfuscation of Integrated Circuits," Texas Instruments, Bengaluru, India, Jan. 13, 2017
100. "Internet of Things: Energy-Efficient Machine Learning Classification and Hardware Security," University of Illinois at Chicago, April 21, 2017
101. "Authentication and Functional Obfuscation of Integrated Circuits," Shanghai Jiao Tong University, June 28, 2017