

Figure 2: (a) Multiple measurements of the same device. (b) Repeatability test results. (c) $\sqrt{I_D}$ vs. V_{GS} .

cally to form arrays. The floorplan and die photo are shown in Fig. 1(b). To minimize layout-dependent effects (LDEs), which are acute in FinFET nodes, dummies are added to each DUT, and the neighborhood of each element is matched. The die is split into two parts, X-array (left) and Y-array (right). In the X-array, the distance between consecutive devices in the X-axis is $10\mu\text{m}$ and Y-axis is $25\mu\text{m}$, whereas in the Y-array, it is $13\mu\text{m}$ along the Y-axis, and $30\mu\text{m}$ along the X-axis. Four binary-to-thermometer decoders (2×8 -bit, 1×6 -bit, and 1×5 -bit) on the die are used to select the elements for measurement.

Measurement Setup: The dice are assembled in QFN packages. A test holder is used to measure multiple dice sequentially on the same PCB. A high-gain, low offset OTA, OPA378, is used on the PCB to ensure that the source terminal of the DUT is exactly at 0V . The DUT is measured at 250ms intervals, avoiding settling transients. An FPGA is used to provide inputs to the decoders to sequentially turn on one element after another for measurement. Test currents are fed to the die using a Keithley 2401 Sourcemeter and the output voltage, (V_{GS}), of the DUT is measured using a high impedance Keithley 2010 multimeter. To validate the noise performance of our setup, we measure the same device 15 times with a 250ms gap between measurements. The results in Fig. 2(a) show that the standard deviation, σ , of the measurements is $20\mu\text{V}$, i.e., 40ppm of the measured V_{GS} . We use the median value of the measured V_{GS} in our experiments. Next, to validate repeatability [14], a set of 3472 devices is measured, denoted as Measured Set 1, and the same devices are measured one day later, denoted as Measured Set 2. In Fig. 2(b), we see that the two measured sets have a high correlation of 0.9999, demonstrating temporal repeatability. All measurements are performed at 292K .

III. MEASUREMENT RESULTS

We have measured 19 dice with 9,992 devices each. The foundry lists all dice as being from the TT corner of the wafer

but does not provide their location on the wafer. The I-V characteristic for long-channel diode-connected transistors is:

$$I_D = (\beta/2)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (1)$$

where V_{DS} is the drain-source voltage, and λ is the channel length modulation factor. We validate that this relationship applies to our DUT by measuring V_{GS} versus $\sqrt{I_D}$ as shown in Fig. 2(c) and observe a linear relationship. For each DUT, we measure V_{GS} at four values of input current, I_D , to extract its V_{TH} and β by curve fitting on Eq.(1). We approximate the value of λ from simulations and notice that even if λ changes by 50% after fabrication, the measured ΔV_{TH} and $\Delta\beta$ between any two devices change by $< 1\%$.

Visualizing the ΔV_{TH} Surface on a Die: Fig. 3 shows ΔV_{TH} , which is the difference between the V_{TH} at a location and the mean V_{TH} on the die in a $600\mu\text{m}\times 600\mu\text{m}$ die area. Fig. 3(a) shows the extracted ΔV_{TH} containing both the random and distance-dependent components. To see the distance-dependent component, we low-pass-filter the extracted ΔV_{TH} surface to remove the random component. Fig. 3(b) shows the ΔV_{TH} surface on multiple dice, where the zero in the colorbar corresponds to the lowest value on the die as an artifact of filtering. Additionally, the colorbar range of ΔV_{TH} in Fig. 3(a) is about $4\times$ larger than that in Fig. 3(b), indicating that the distance-dependent component is a small fraction of the random component, even for our large device. Note that the ΔV_{TH} surfaces in Fig. 3(b) have spatially correlated regions (same color) and are different on each die.

Next, we find the distribution of ΔV_{TH} for all device pairs on the die separated by distance, D , and show its histogram in Fig. 4(a) and Fig. 4(b) for $D = 10\mu\text{m}$ and $D = 250\mu\text{m}$, respectively. There are 5520 transistor pairs on each die separated by $D = 10\mu\text{m}$ and 4560 pairs separated by $D = 250\mu\text{m}$. From the figure, it can be seen that the distribution is Gaussian at both distances. At minimum D , $D = 10\mu\text{m}$, the mean, $\mu(\Delta V_{TH}) \approx 0$, and the standard deviation, $\sigma(\Delta V_{TH}) = 2.10\text{mV}$, which is similar to that simulated using Monte Carlo models in the PDK (which only capture distance-independent random variations), and is also similar to published data [15]. This is consistent with the fact that at $D = 10\mu\text{m}$, variations in V_{TH} are mainly due to the random component. At $D = 250\mu\text{m}$, both μ and the σ change due to distance-dependent variations. The values of $\mu(\Delta V_{TH})$ and $\sigma(\Delta V_{TH})$ of the distributions at different D are shown in Fig. 4(c). Here, we see a shift in the μ and σ due to distance-

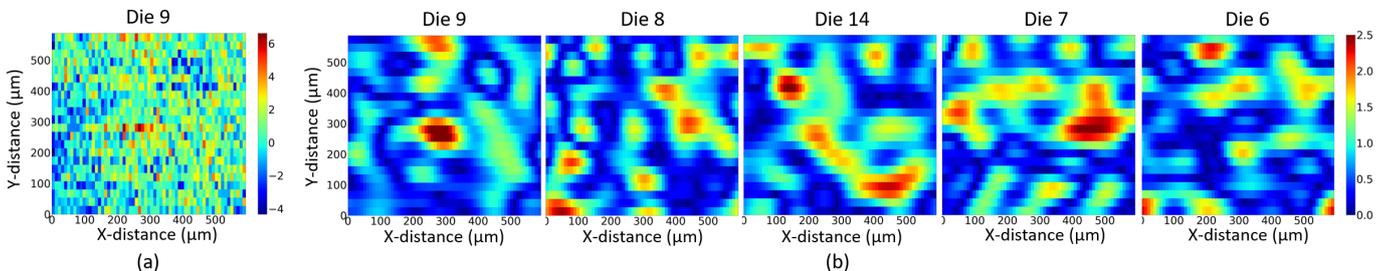


Figure 3: (a) ΔV_{TH} surface on a die before filtering. (b) ΔV_{TH} surface on multiple dice after low-pass filtering. Note that the colorbar range for (b) is $4\times$ smaller than for (a) for visual clarity.

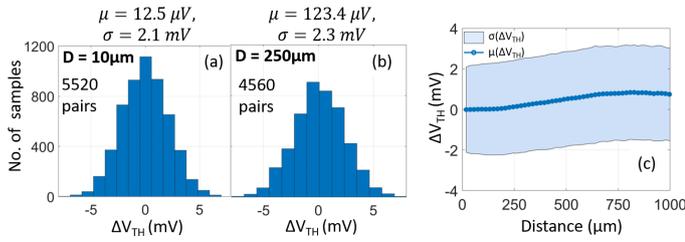


Figure 4: ΔV_{TH} distribution at (a) $D = 10 \mu\text{m}$, and (b) $D = 250 \mu\text{m}$. (c) $\mu(\Delta V_{TH})$ and $\sigma(\Delta V_{TH})$ vs. D .

dependent variations, although the shift is small compared to the random variations measured at minimum D .

Devices Arranged in NonCC and CC: We now infer the currents of each DUT by substituting the extracted V_{TH} and β values from measurement, along with a constant V_{GS} value, into Eq.(1). Here, V_{GS} is chosen such that the overdrive voltage, $V_{GS} - V_{TH}$ is around 0.25V (often used in current mirrors [16]). We use this method to infer device currents because, during measurement, we keep the device current constant for all DUT while allowing their V_{GS} to change whereas in a current mirror the V_{GS} is the same for the device pairs while the output current changes based on device V_{TH} and β . We then find the current mismatch, $\Delta I/I$, between device pairs arranged in NonCC and CC as shown in Fig. 5(a). We infer the currents of each unit cell individually, and then combine them during data processing to result in NonCC and CC arrangements, instead of adding them on chip as is common in DACs [10], [16]. We do this since our DUTs cannot be switched on simultaneously. We consider two different device sizes, Size 2x, and Size 4x having 2, and 4 unit cells, respectively, each of size $W/L = 1.15 \mu/0.28 \mu$.

We plot the mean, $\mu(\Delta I/I)$, and variance, $\sigma^2(\Delta I/I)$, of the $\Delta I/I$ distribution in Fig. 5(b) for both device sizes in NonCC (left) and CC (right) on one of the measured die. From the figure, we see that the mean is virtually independent of the device size and its magnitude is small when compared to $\sigma(\Delta I/I)$ of the Size 2x device even though it has a larger area. Moreover, since the devices arranged in the CC pattern cancel linear variations, a non-zero mean, as seen in Fig. 5(b)

(Top-Right), indicates nonlinear variations.

As expected from [1], [2], we see that the $\sigma^2(\Delta I/I) \propto 1/(WL)$ at minimum D since the random component dominates at this spacing. The distance-dependent component of $\sigma^2(\Delta I/I)$, however, remains the same for the different sizes as the curves show the same trend as D increases (also observed in [2]). This change in $\sigma^2(\Delta I/I)$ with distance in both CC and NonCC is a result of correlated spatial variations.

We now show how NonCC and CC formats are affected by variations on multiple dice for Size 2x devices, in Fig. 5(c). Here, we see that CC has a lower $\mu(\Delta I/I)$ and $\sigma^2(\Delta I/I)$ than NonCC since it cancels linear distance-dependent components. However, at short distances, the distance-dependent component itself is a small fraction of the random variations, that affect both NonCC and CC, hence its impact is less. In summary, (a) within-die distance-dependent variations have nonlinear and spatially correlated components that affect both NonCC and CC, (b) the distance-dependent component is a small fraction of the random component even for large device sizes. Therefore, at short distances, CC may provide little advantage over NonCC as random variations dominate.

IV. MODELING AND IMPACT ON ANALOG DESIGN

We now find the combined distribution of $\Delta I/I$ of a minimum of 11,006 device pairs from 19 dice, at each distance D . We then extract the distance-dependent mean, $\mu(\Delta I/I)_D$, and variance, $\sigma^2(\Delta I/I)_D$ by subtracting out the random component (variations at $D = 10 \mu\text{m}$) and plot them for both NonCC and CC patterns in Fig. 6. Clearly, both patterns are affected by these variations. But as noted earlier, the reduction in $\mu(\Delta I/I)_D$, and variance, $\sigma^2(\Delta I/I)_D$ for CC patterns is due to the cancellation of the linear components. Before applying this understanding to unary current-steering DACs we discuss the area difference between NonCC and CC layouts.

NonCC vs. CC Layout Area: In Fig. 7, we see example layouts of a current mirror circuit in 12nm FinFET showing a NonCC and a CC pattern. Here, devices A and B have the same size (W/L) with 2 unit cells and their source, and gate connections (not shown) are the same in both layouts. The drain connections, however, require more area in CC (one

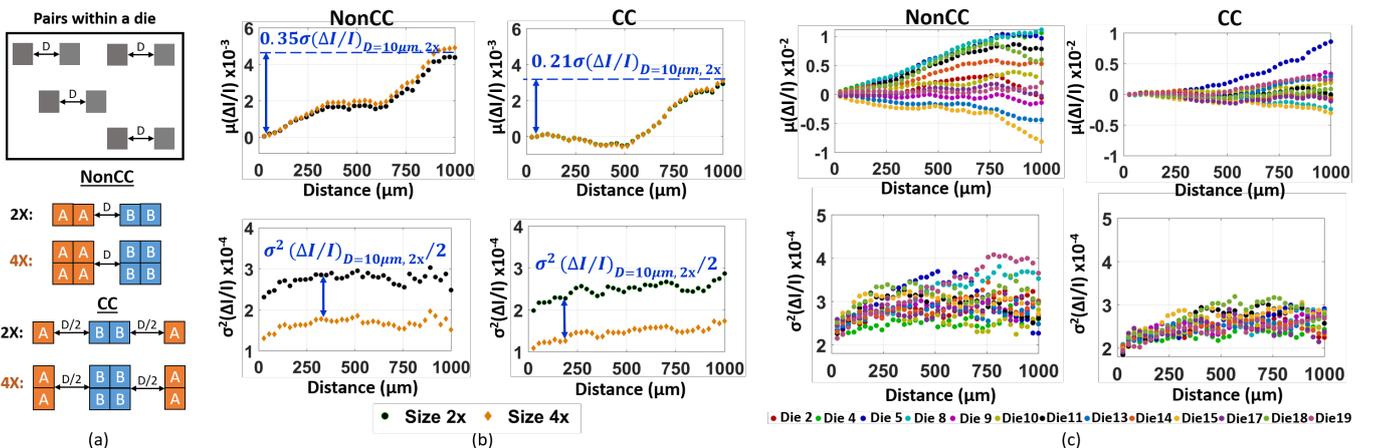


Figure 5: (a) NonCC and CC patterns used to find $\Delta I/I$. (b) μ and σ of $\Delta I/I$ distribution of devices arranged in NonCC and CC and separated by distance, D . (c) μ and σ of $\Delta I/I$ distribution of devices of Size 2x on multiple dice.

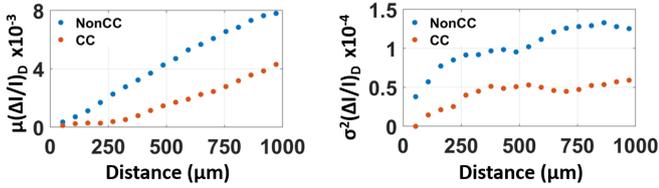


Figure 6: Average distance-dependent variations from multiple dice.

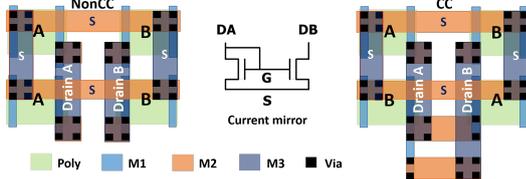


Figure 7: Example NonCC and CC layouts of a 2-device (4 unit) current mirror (NonCC area < CC area)

additional horizontal track), as shown in Fig. 7, because of the cross-coupled connection. Furthermore, the number of extra routing tracks in CC increases linearly with the number of devices in a row, resulting in larger area and parasitics.

Designing Current-Steering DACs: Here, we apply our findings to unary DAC designs. First, we find the current mismatch specification, $\sigma^2(\Delta I/I)_{spec}$ for a 99.7% yield [10]. This total mismatch specification has two components, i.e., the random mismatch, $\sigma^2(\Delta I/I)_R$, and the distance-dependent mismatch, $\sigma^2(\Delta I/I)_D$, as shown in Eq.(2).

$$\sigma^2(\Delta I/I)_{spec} = \sigma^2(\Delta I/I)_R + \sigma^2(\Delta I/I)_D \quad (2)$$

Next, we follow the procedure below to size the devices.

- 1) Find the approximate area assuming $\sigma^2(\Delta I/I)_D = 0$.
- 2) Find $\sigma^2(\Delta I/I)_D$ for the estimated layout area.
- 3) Find new $\sigma^2(\Delta I/I)_R$ using the estimated $\sigma^2(\Delta I/I)_D$.
- 4) Find the device size (WL) using $\sigma^2(\Delta I/I)_R$ [3].
- 5) Estimate layout area for NonCC and CC (using double CC pattern [10]) and iterate steps 2 to 5 as necessary.

6- and 8-bit DACs: In the 6-bit DAC with 63 devices, the distance-dependent mismatch is a small fraction ($\leq 5\%$) of the mismatch specification for NonCC and CC, and the required device size (WL) is similar for both as shown in Table I. However, the estimated layout area is higher in CC owing to the extra routing area required for drain connections as explained in Fig. 7. In the 8-bit DAC, with 255 devices, the distance-dependent mismatch is 30% and 10% of the mismatch specification for NonCC and CC, respectively, and NonCC requires a larger device size than CC to meet the specifications. Even with this increase in device size, NonCC has a lower layout area when compared to CC. Here, we neglect the $\mu(\Delta I/I)$ since it is small compared to $\sigma(\Delta I/I)$. Therefore, in both these cases, NonCC is more advantageous than CC while meeting specifications and these finding can be extended to small devices in OTAs and lower-resolution DACs.

10-bit DAC: For the 10-bit DAC with 1023 devices, it is not possible to meet the mismatch specification with NonCC as shown in Table I, and hence CC is required. Also, for the double CC pattern used here the distance between devices closer to the center and the edge is high, the distance-dependent mismatch is $\geq 50\%$ of the total mismatch and the device size is

Table I: Comparing NonCC and CC unary current-steering DACs

	6-bit DAC		8-bit DAC		10-bit DAC	
	NonCC	CC	NonCC	CC	NonCC	CC
$\sigma^2(\Delta I/I)_{spec}(10^{-4})$	8.87		2.22		0.55	
$\sigma^2(\Delta I/I)_D(10^{-4})$	0.4	0	0.6	0.2	0.9	0.3
$\sigma^2(\Delta I/I)_R(10^{-4})$	8.47	8.87	1.62	2.02	-	0.25
Device $W \times L$ (μm^2)	0.162	0.155	0.849	0.680	-	5.50
Total layout area (μm^2)	230	306	2958	3418	-	80800

very large, hence, this is not an optimal CC pattern, and other CC patterns with less distance between devices can be used. Since distance-dependent variations are often not included in Foundry-provided models our measurement-based findings can be used by a designer to improve their layout quality.

V. CONCLUSION

In this work, we measure and quantify distance-dependent variations on 19 dice with 9,992 devices each, in a 12nm FinFET technology. We then use chip measurements to create a model that estimates mismatch and area overheads for NonCC and CC placement patterns. Our findings are summarized:

- For small devices (6-bit, 8-bit DACs, OTAs), random variations dominate, and NonCC and CC layouts have similar mismatch while NonCC reduces layout area.
- For larger devices (10-bit DACs and higher), the distance-dependent component cannot be ignored even for CC patterns and must be considered during design.

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REFERENCES

- [1] K. Lakshmikumar, *et al.*, "Characterisation and modeling of mismatch in MOS transistors for precision analog design," *IEEE J. Solid-St. Circ.*, vol. 21, no. 6, pp. 1057–1066, 1986.
- [2] M. Pelgrom, *et al.*, "Matching properties of MOS transistors," *IEEE J. Solid-St. Circ.*, vol. 24, no. 5, pp. 1433–1439, 1989.
- [3] P. Kinget, "Device mismatch and tradeoffs in the design of analog circuits," *IEEE J. Solid-St. Circ.*, vol. 40, no. 6, pp. 1212–1224, 2005.
- [4] H. Tuinhout, "Design of matching test structures [IC components]," in *Proc. ICMTS*, pp. 21–27, 1994.
- [5] U. Schaper, *et al.*, "Precise characterization of long-distance mismatch of CMOS devices," *IEEE T. Semicond. M.*, vol. 14, pp. 311–317, 2001.
- [6] M. J. M. Pelgrom, *Analog to Digital Conversion*. Cham, Switzerland: Springer, 4th ed., 2022.
- [7] P. Friedberg, *et al.*, "Modeling within-die spatial correlation effects for process-design co-optimization," in *Proc. ISQED*, pp. 516–521, 2005.
- [8] J. Xiong, *et al.*, "Robust extraction of spatial correlation," *IEEE T. Comput. Aid. D.*, vol. 26, no. 4, pp. 619–631, 2007.
- [9] H. Elzinga, "On the impact of spatial parametric variations on MOS transistor mismatch," in *Proc. ICMTS*, pp. 173–177, 1996.
- [10] A. van den Bosch, *et al.*, "A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter," *IEEE J. Solid-St. Circ.*, vol. 36, no. 3, pp. 315–324, 2001.
- [11] P. M. Ferreira, *et al.*, "Surface versus performance trade-offs: A review of layout techniques," *J. Int. Circuits Syst.*, vol. 1, pp. 1–16, 2022.
- [12] A. K. Sharma, *et al.*, "Common-centroid layouts for analog circuits: Advantages and limitations," in *Proc. DATE*, pp. 1224–1229, 2021.
- [13] A. L. S. Loke, *et al.*, "Analog/mixed-signal design challenges in 7-nm CMOS and beyond," in *Proc. CICC*, pp. 1–8, 2018.
- [14] J. A. Croon, *et al.*, *Matching Properties of Deep Sub-micron MOS Transistors*. Dordrecht, The Netherlands: Springer, 2005.
- [15] M. D. Giles, *et al.*, "High sigma measurement of random threshold voltage variation in 14nm logic FinFET technology," in *Proc. IEEE Symp. VLSI Tech.*, pp. T150–T151, 2015.
- [16] B. Razavi, "The current-steering DAC [a circuit for all seasons]," *IEEE Solid-St. Circ.*, vol. 10, no. 1, pp. 11–15, 2018.