

# The Impact of Electromigration in Copper Interconnects on Power Grid Integrity

Vivek Mishra and Sachin S. Sapatnekar

ECE Department, University of Minnesota, Minneapolis, MN

**Abstract**—Electromigration (EM), a growing problem in on-chip interconnects, can cause wire resistances in a circuit to increase under stress, to the point of creating open circuits. Classical circuit-level EM models have two drawbacks: first, they do not accurately capture the physics of degradation in copper dual-damascene (CuDD) metallization, and second, they fail to model the inherent resilience in a circuit that keeps it functioning even after a wire fails. This work overcomes both limitations. For a single wire, our probabilistic analysis encapsulates known realities about CuDD wires, e.g., that some regions of these wires are more susceptible to EM than others, and that void formation/growth show statistical behavior. We apply these ideas to the analysis of on-chip power grids and demonstrate the inherent robustness of these grids that maintains supply integrity under some EM failures.

**Keywords:** Electromigration, process variation, robustness, power grid

## I. INTRODUCTION

Electromigration (EM) in interconnects occurs due to the movement of metal atoms, activated by momentum transfer from collisions with free electrons [1]. When bounded by a blocking boundary such as a barrier layer, this movement causes a depletion of atoms at the cathode end and a surplus at the anode; this depletion eventually leads to void nucleation and subsequent growth [2]. Since the critical stress for void nucleation is very small for copper dual damascene (CuDD) structures, voids can form early in the lifetime of a design [3].

There is a large gap between what is known about the physics of EM in CuDD wires and the knowledge used at the circuit level. Traditional EM analysis is based on failure criteria measured under accelerated aging. An interconnect whose resistance crosses a predetermined threshold under stress is deemed to have failed, and the time-to-failure parameters are extrapolated to normal operating conditions using Black's equation [4]. This analysis, supplemented with the Blech-length thresholding criterion [5] that defines wires that are immortal under EM, is used by circuit designers to derive maximum current density limit rules on individual wires.

There are several problems with such an approach. First, in a real circuit, the impact of such failures is context-dependent. In some cases, a large failure may be tolerated due to the inherent resilience in the circuit, e.g., due to redundancy in a power grid, where the failure of one wire may be compensated by current flow through other paths. Therefore, the use of a single threshold for the resistance change may either be excessively conservative, or not conservative enough, depending on how the threshold is chosen and how robust the circuit is. Second, for CuDD interconnects, previous work [3] has shown that the Blech-length approach, where wires with a sufficiently small  $jL$  product ( $j$  is the current density,  $L$  is the length) can be considered immortal, is invalid, and it has been observed that some lines fail *probabilistically* even if they satisfy the Blech criterion on their  $jL$  value. The root cause of this difference is that the critical stress for void nucleation in Cu is  $10\times$  lower than that for Al, implying that it is

possible for voids to nucleate soon, before providing the opportunity for opposing back-stresses to build up to balance them. Third, there are known effects such as the current divergence effect (discussed in Section III-D) that are not widely considered at the circuit level.

These peculiarities for CuDD metallization indicate the need to develop models for EM to enable probabilistic circuit analysis in a context-sensitive way. The probabilistic viewpoint reflects both the fact that mechanisms for EM are stochastic, and that the number of interconnects on a chip is large enough that such statistical effects may show up in different parts of the chip. There have been few prior works in this direction: the work in [6] built up on [7] to consider some EM issues beyond the conventional Black's equation, but was based on the problematic Blech length criterion.

In this work, we first present an analytical model to predict the distribution of void growth and consequently, the resistance change in a wire. Next, we demonstrate how this affects the probabilistic distribution of voltage drops in standard power grid benchmarks.

## II. DETERMINISTIC EM MODELS FOR CU INTERCONNECTS

The fundamental phenomenon of EM consists of forces that drive atoms from the cathode to the anode. This produces regions of uneven concentration, i.e., depletion and accumulation, which lead to diffusion through various possible mechanisms: grain boundary, volume, surface, and/or interface diffusion.

EM failure occurs in Cu interconnects in two phases:

- *Void nucleation:* After a wire has been stressed, the depletion of atoms at the cathode creates a tensile stress. Once a critical stress threshold value has been crossed, the void nucleates.
- *Void growth:* After nucleation, further movement of metal atoms from the void results in void growth. This results in increased wire resistance due to the effectively reduced cross-section. If the void grows large enough, it may result in a break in the wire, resulting in either an open circuit or a vastly increased resistance, in cases where the current through the wire can flow through the higher-resistivity barrier layer of the CuDD interconnect.

We begin by introducing deterministic models for the void nucleation and growth phases. The foundation for modern models for EM, incorporating the impact of stress, is based on the stress evolution model in [8], which details a set of differential equations describing the interplay between electron wind force and back stresses in the interconnect. To model void nucleation, we use this stress evolution model, extended to incorporate thermal stress effects using the formulation as presented in [9]. The time,  $t_n$ , at which a void nucleates is given by

$$t_n = \frac{K_{t_n}}{D_{eff}} \quad (1)$$
$$\text{where } K_{t_n} = \frac{\pi}{4} \left( \frac{(\sigma_c - \sigma_{th})^2 \Omega k_B T}{(eZ_{eff}^* \rho j)^2 B} \right)$$

The symbol  $K_{t_n}$  groups together a number of terms to reflect the dependency of  $t_n$  on the effective diffusivity,  $D_{eff}$ . In the detailed expression for  $K_{t_n}$ ,  $\sigma_c$  is the effective critical stress for void nucleation;  $\sigma_{th}$  is a term that accounts for the effects of thermal

stresses;  $\Omega$  is atomic volume;  $k_B$  is Boltzmann's constant;  $T$  is the temperature;  $q^* = eZ_{eff}^*$  is the effective charge, where  $e$  is the elementary charge on an electron and  $Z_{eff}^*$  is the apparent effective charge number;  $E = \rho j$  is the electric field, where  $\rho$  is the resistivity of copper and  $j$  is the current density in the wire;  $B$  is the effective bulk modulus for the Cu–dielectric system.

In a CuDD process, a trench is first etched into the interlayer dielectric, and a Ta-based liner is deposited therein to prevent Cu from diffusing through. Next, the Cu used to construct the interconnect is deposited, and finally, the lines are capped above. The diffusivity,  $D_{eff}$ , for EM can be considered as a sum of contributions of atomic transport along various diffusion paths: the Cu capping interface  $I$  between Cu and the Ta liner, the surface  $S$ , the grain boundaries  $GB$ , and the bulk  $B$ . The product of effective diffusivity and the effective atomic number along a CuDD interconnect can be written as [10]:

$$Z_{eff}^* D_{eff} = Z_I^* D_I \left( \frac{\delta_I}{h} \right) + Z_S^* D_S \delta_S \left( \frac{1}{h} \right) + Z_{GB}^* D_{GB} \delta_{GB} \left( \frac{1}{d} - \frac{1}{w} \right) + n_B D_B$$

where  $\delta_I$ ,  $\delta_S$ ,  $\delta_{GB}$ , and  $\delta_B$  denote the width of the capping interface, surface, grain boundary, and bulk, respectively,  $h$  is the line height,  $d$  is the grain size, and  $n_B$  is the fraction of atoms diffusing through the bulk. For thin copper interconnects at nanometer-scale geometries, which are the subject of this work, the primary diffusion paths for void nucleation is along the surface [10]–[13] and grain boundaries play a significant role only in much wider wires that show polycrystalline grain structures. However, once the void nucleates the surface of the void which is an open copper surface acts as a fast diffusion path [12]. Accordingly, we consider only the dominant surface diffusivity term for each stage and neglect the other terms.

After nucleation at time  $t_n$ , given by (1), the void starts to grow. Various void growth kinetics have been observed in CuDD structures, depending on the direction of the current. The scenario where the electron flow is downwards, shown in Fig. 1(a), corresponds to the via-above case, and results in potential void formations at the via or in the wire, as illustrated in the figure. For the case where the electron flow is upwards, illustrated in Fig. 1(b), an upstream void is potentially formed in the upper wire, typically at a corner of the wire or within the wire, as shown. The mechanics of void formation in each case – *span growth* (for both the via-above and via-below cases), when the void spans the entire interconnect, and *slit growth*, where it forms along the via (for the via-above case) – is different and necessitates a different model.

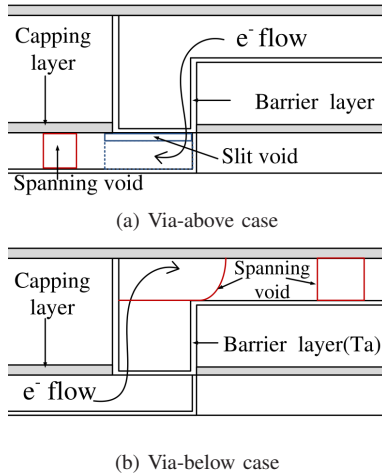


Fig. 1. Mechanisms of void evolution for the via-above and via-below cases.

In either case, once a void is formed, the primary mechanism of increase in the void size is due to drift with a constant drift velocity  $v_d$  [2], [14], which is related to the effective mobility and the driving force expressed as the Nernst-Einstein relation given by:

$$v_d = \left( \frac{D_{eff}}{k_B T} \right) e Z_{eff}^* \rho j \quad (2)$$

If the void nucleates at time  $t_n$ , then at an observation time  $t_o$ , the void has been growing for a length of time,  $t_o - t_n$ . The length of the void increases due to drift, as given by:

$$L_{void}(t_o) = v_d \cdot (t_o - t_n) = \left( \frac{D_{eff}}{k_B T} \right) e Z_{eff}^* \rho j (t_o - t_n) \quad (3)$$

### III. PROBABILISTIC MODELING OF EM FAILURE

The conventional explanation of EM in Al interconnects was predicated on the interaction between the electron wind force and the back stress force. For some interconnects, with low current and/or small length, the two forces could be in equilibrium in the steady state, so that critical stress  $\sigma_c$  for void nucleation is never reached, implying that these wires are *immortal* to EM effects. For a wire of length  $L$  with current density  $j$ , it was shown that the criterion for immortality was  $jL \leq (jL)_{crit}$ , where  $(jL)_{crit}$  is a property of the material and the fabrication process. However, as noted in Section I, it has been observed that for CuDD interconnects, the immortality property does not hold, and lines are apt to show probabilistic behavior [3].

#### A. Probabilistic Models for Activation Energy

The diffusivity is related, through an Arrhenius relationship, to temperature  $T$  and the activation energy  $E_a$  as

$$D_{eff} = D_0 \exp \left( - \frac{E_a}{k_B T} \right) \quad (4)$$

where  $D_0$  is a constant. Recent work has observed EM failure is correlated to uncertainties in the microstructure and physical parameters of an interconnect, which relates to the statistical distribution of the normally-distributed activation energy.

Strictly speaking, since the activation energy is a property of the microstructure, it can vary within the wire depending on the grain boundary orientation. For instance EM activation energy can vary between grains depending on the orientation of the grain with respect to each other and with respect to the interfacial layer [25], [26]. However, at a macroscopic level, it is reasonable to assume that the effective activation energy is same for a wire and varies only between the wires [2], [12], [15]–[18]. Therefore, we work with the idea of the “effective activation energy” for each wire, which is an averaged activation energy value for that wire. As observed above, the activation energy is normally distributed, and so we model the effective activation energy,  $E_a$ , for each wire using an independent Gaussian random variable.

#### B. Statistical Models for Void Dimensions

Since effective activation energy,  $E_a$ , for a wire follows a Gaussian distribution, it is obvious from (4) that diffusivity, which contains  $E_a$  in an exponential term, follows a lognormal distribution.

In our discussion below, for a distribution  $Z = N(\mu, \sigma)$  with mean  $\mu$  and standard deviation  $\sigma$ , we denote a lognormal  $X = e^Z$  as  $\text{LogN}(\mu, \sigma)$ . Therefore, if  $E_a = N(\mu, \sigma)$ , then  $D_{eff} = \text{LogN}(\mu_{D_{eff}}, \sigma_{D_{eff}})$ , where

$$\begin{aligned} \mu_{D_{eff}} &= \log D_0 - \frac{\mu}{k_B T} \\ \sigma_{D_{eff}} &= \frac{\sigma}{k_B T} \end{aligned} \quad (5)$$

As discussed in Section II, the mechanisms responsible for  $D_{eff}$  are different in the nucleation and growth phases: interface diffusivity for nucleation, and surface diffusivity for growth. We refer to the effective diffusivity for the nucleation and growth phases as  $D_{eff,n}$  and  $D_{eff,g}$ , respectively.

**Nucleation:** The expression for nucleation time  $t_n$  was provided in Equation (1). From this, it is clear that  $t_n = \text{LogN}(\mu_{t_n}, \sigma_{t_n})$ ,

$$\begin{aligned}\mu_{t_n} &= \log(K_{t_n}) - \mu_{D_{eff,n}} \\ \sigma_{t_n} &= \sigma_{D_{eff,n}}\end{aligned}\quad (6)$$

The proof of this is straightforward, and relies on the observation that the distribution of a reciprocal of a lognormal  $\text{logN}(\mu, \sigma)$  is another lognormal characterized as  $\text{logN}(-\mu, \sigma)$ .

**Growth:** During void growth, the length of a void evolves with time according to Equation (3). Grouping together all deterministic parameters in this equation, if a void nucleates, then its length at observation time  $t_o$  is given by:

$$L_{void}(t_o) = \left( \frac{D_{eff,g}}{k_B T} \right) e Z_{eff}^* \rho_{Cu} j (t_o - t_n) \quad (7)$$

$$= c_1 D_{eff,g} - c_2 t_n D_{eff,g} \quad (8)$$

Here,  $c_1$  and  $c_2$  are deterministic constants. The first term,  $c_1 D_{eff,g}$ , is clearly lognormal since  $D_{eff,g}$  is lognormal; the second term,  $c_2 t_n D_{eff,g}$  is a scaled product of lognormals, which is also a lognormal. Therefore,  $L_{void}$  is a difference of two lognormals,  $c_1 D_{eff,g}$  and  $c_2 t_n D_{eff,g}$ , and it can be approximated by a lognormal using the widely-used Wilkinson approximation [19].

If  $\mu_X, \sigma_X$  ( $\mu_Y, \sigma_Y$ ) are the mean (standard deviation) of the underlying normal distribution for  $c_1 D$  ( $c_2 t_n D$ ), then

$$\mu_X = \log c_1 + \mu_{D_{eff,n}}; \sigma_X = \sigma_{D_{eff,n}}$$

$$\mu_Y = \log c_2 + \mu_{D_{eff,g}} + \mu_{t_n}$$

$$\sigma_Y = \sqrt{\sigma_{D_{eff,g}}^2 + \sigma_{t_n}^2}$$

where  $\mu_{t_n}$  and  $\sigma_{t_n}$  are given by Equation 6. This provides us with an analytical expression for the distribution of the random variable,  $L_{void}(t_o)$ . For this lognormal distribution,  $\text{logN}(\mu_{L_{void}}, \sigma_{L_{void}})$ , we can compute the parameters of the distribution using Wilkinson approximation as follows:

$$u_1 = e^{(\mu_X + \sigma_X^2/2)} - e^{(\mu_Y + \sigma_Y^2/2)}$$

$$u_2 = e^{(2\mu_X + 2\sigma_X^2)} + e^{(2\mu_Y + 2\sigma_Y^2)} - 2e^{(\mu_X + \mu_Y + (\sigma_X^2 + \sigma_Y^2)/2)}$$

$$\mu_{L_{void}} = 2 \log(u_1) - \log(u_2) / 2$$

$$\sigma_{L_{void}}^2 = \log(u_2) - 2 \log(u_1)$$

### C. Probability Distribution of the Resistance Change due to EM

We will now use the void length distribution to evaluate the distribution of resistance change for different scenarios of void growth. Our resistance evolution model considers separately the cases of the *span growth* and *slit growth* mechanisms shown in Fig. 1. For the case of the span void, the change in resistance,  $\Delta R$ , is [14]:

$$\frac{\Delta R}{R_o} = \left( \frac{\rho_{Ta} A_{Cu}}{\rho_{Cu} A_{Ta}} - 1 \right) \frac{L_{void}}{L_{wire}} \quad (9)$$

where  $\rho_{Cu}$  and  $\rho_{Ta}$  are, respectively, the resistivities of copper and Tantalum,  $R_o = \rho_{Cu} L_{wire} / A_{Cu}$  is the resistance of the interconnect wire segment, which is assumed to have length  $L_{wire}$  and cross-sectional area  $A_{Cu}$ , and  $A_{Ta}$  is the cumulative cross-sectional area of the tantalum barrier. Recall that the void length,  $L_{void}$ , was shown in Section III-B to be lognormally distributed after nucleation.

Since all other terms are constants, it can be seen that for span growth voids, for both the via-above and via-below cases,  $\Delta R$  is lognormal with the same  $\sigma$  as  $L_{void}$ , but with a shifted mean.

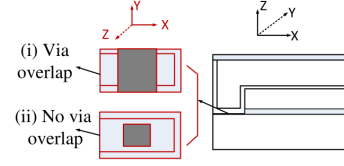


Fig. 2. CuDD via-liner alignment to limit resistance increase under EM [20].

For the slit growth scenario, as shown in Fig. 2, the via size may be chosen so that the via overlaps with the liner (case (i)) or not (case (ii)). As reported in [20], in the former case, the liner provides a conductive path that enables a continued connection, and this may be used to ensure electrical connectivity after a slit void is formed. A derivation similar to that in [14] can be used to show:

$$\frac{\Delta R}{R_o} = \left( \frac{\rho_{Ta} A_{Cu}}{\rho_{Cu} A_{Ta}} - 1 \right) \frac{H_{void}}{L_{wire}} \quad (10)$$

where  $H_{void}$  is the height of the slit void. We use this to ignore the impact of slit growth voids in our evaluation of  $\Delta R$ : although slit voids tend to form earlier than span voids, it is easy to build redundancy into the power grid to guard against slit voids by inserting redundant vias; in fact, this is often done anyway. Therefore, we focus our attention on the impact of span voids.

To write the expressions for the mean and standard deviation of  $\Delta R$  more simply, we introduce the notation

$$k_R = \left( \frac{\rho_{Ta} A_{Cu}}{\rho_{Cu} A_{Ta}} - 1 \right) \frac{1}{L_{wire}} \quad (11)$$

The resistance change distribution can then be expressed as  $\Delta R \text{LogN}(\mu_{\Delta R}, \sigma_{\Delta R})$ , where

$$\mu_{\Delta R} = \mu_{L_{void}} + \log k_R + \log R_o \quad (12)$$

$$\sigma_{\Delta R} = \sigma_{L_{void}} \quad (13)$$

We now summarize the conditions that must be satisfied to achieve a resistance change of  $\Delta R$  at an observation time  $t_o$ . First, a void must nucleate, and then this nucleated void must grow to the point where the wire resistance increases by  $\Delta R$ . Using these notions, we can now determine the probability that a given wire will have a resistance change  $\Delta R$  as:

$$\Pr(\Delta R) = \begin{cases} \Pr(\Delta R | \text{nucleation}) \cdot \Pr(\text{nucleation}) & \Delta R > 0 \\ 1 - \Pr(\text{nucleation}) & \Delta R = 0 \end{cases} \quad (14)$$

For the first case, the first term, for  $\Delta R$  for a nucleated void is given by  $\text{LogN}(\mu_{\Delta R}, \sigma_{\Delta R})$  as derived above, with the mean and standard deviation given by Equation (13). For the second, the nucleation probability is given by  $\text{LogN}(\mu_{t_n}, \sigma_{t_n})$  in Equation (6), and this quantity corresponds to the probability that the nucleation time,  $t_n$ , is less than the observation time,  $t_o$ , i.e., the CDF of  $t_n$  at  $t_o$ . Therefore, the right-hand-side is a lognormal times a constant, i.e., the PDF of  $\Delta R$  has the shape of a lognormal function. The second case corresponds to the scenario where the void does not nucleate, with a probability of  $1 - \text{CDF}(t_n = t_o)$ .

### D. Incorporating the Effect of Current Divergence

The conventional approach to estimating EM failure is based on a current density-based model. Under this model, for two wires of equal length, the one with the larger current density should fail sooner. However, the work in [21] demonstrated experimentally that this is not always the case, by showing test circuit where one wire has twice the current density as another, but experiences consistently later failures. This is consistent with other reported work where the *current*

*divergence* effect comes into play: for example, [22] shows fabricated test structures where the failure rates on a wire segment depends not only on the current density on the segment, but also on those on adjacent segments that share via(s) with this segment.

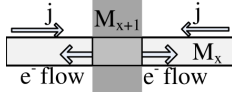


Fig. 3. A via-tree structure where the effective current density is more than the density of current flowing through the wire.

We compute the effective current density on a wire by considering the magnitude and directions of currents in neighboring wires. The effective current density for a wire is computed in terms of the flux-divergence criterion, consistent with [21]. This is illustrated in Figure 3, which shows two wires on metal layers  $M_x$  and  $M_{x+1}$  connected by a via. A via in a CuDD interconnect structure acts as a blocking layer so that metal atoms are not permitted to migrate through it. Therefore, any flux that would have gone to the via is transmitted to a neighboring wire.

In the example shown here, the current on both segments of the wire on layer  $M_x$  flows towards the via, i.e., the direction of electron flow is away from the via for both segments. Assuming equal current densities  $j$  on each of the two segments, this implies that there is an effective divergence, which can eventually lead to void nucleation and growth, equivalent to a current density of  $2j$  on both wires. In other words, as compared to the case where the left-hand segment is missing and the right-hand segment has the same current density of  $j$ , the expected rate of atomic transfer is doubled at this node. Using the via node vector notion [21], an effective current density of  $2j$  is used for this wire instead of the actual current density of  $j$ .

#### E. Monte Carlo Analysis of Power Grids Using Importance Sampling

We now use our probabilistic resistance model to perform Monte Carlo analysis of power grids in the presence of resistance variations. Our PDF for the resistance change, derived in Section III-C builds a simple circuit-level abstraction for complex physical phenomena, facilitating simplified analysis at the circuit level by considering  $\Delta R$  as a random variable. However, given that EM is (and should be) a relatively unlikely event, it is essential for our Monte Carlo analysis to be biased appropriately: a truly random set of samples would probably see no resistance change in most (and possibly, for a small set of samples, no) wires. Most importantly, such an approach would see a large number of samples go to waste as they provide little meaningful information.

To overcome this, we use the notion of importance sampling, which biases the distribution, but “unbiases” it as it interprets the results of sampling. Importance sampling is a Monte Carlo method that computes the expected value of a function  $f(x)$  of a random variable  $x$ , which is specified in terms of a distribution  $p(x)$ . This method is particularly useful when  $p(x)$  is skewed or unevenly distributed, i.e., some values of  $x$  have a low probability of occurrence and are not sampled frequently enough, causing sampling errors. Importance sampling resolves this by sampling according to a function  $q(x)$  that is uniformly distributed over the range of  $x$ , and then correcting the error due to sampling from this different distribution by adding appropriate weights to  $f(x)$ . For example, the expectation of  $f(x)$  under the distribution  $p(x)$ , denoted  $E_p[f(x)]$ , is computed as:

$$\begin{aligned} E_p[f(x)] &= \int f(x)p(x) = \int f(x)p(x) \cdot q(x)/q(x) \\ &= \int w(x)q(x) = E_q[w(x)] \end{aligned}$$

where  $w(x) = f(x)/q(x)$  and  $E_p[f(x)]$  is the expectation of  $f(x)$  under the new distribution  $q(x)$ .

In this work, we use a sampling distribution  $q(x)$ , which is a uniform distribution that stretches from 0 to the tail of the lognormal distribution of  $\Delta R$ : the values of this lognormal go from  $\Delta R = 0$  to the  $(\mu + 3\sigma)$  point of the underlying Gaussian,  $\log(\Delta R)$ . If  $K$  is the span of this distribution, then every point has a uniform probability of  $1/K$ . The method samples points on this uniform distribution, feeds them into a power grid simulator based on DC modified nodal analysis, and determines the voltage distribution at each node. The voltages are then translated back to the original distribution by scaling them by the original lognormal distribution using the  $w(x)$  factor.

## IV. RESULTS

### A. Calibration of Correctness under Accelerated Aging

1) *Failures in a Single Wire:* To calibrate the correctness of our models, we first work under assumptions similar to [2], which computes  $t_g$ , the time at which  $L_{void}$  becomes equal to  $L_{via}$ , i.e., allowing the void to grow until it spans across the length of the via, so that we can compare our predicted values against their published Finite Element Analysis (FEA) simulations. Here, we use the statistical framework derived in Section III under accelerated aging under temperature and current stress.

Parameters for accelerated aging are set to ensure a fair comparison, drawing parameter values from [2] where available. We use  $T = 295^\circ\text{C}$  and  $j = 1.33\text{MA}/\text{cm}^2$  (reflecting temperature and current stress),  $\sigma_c = 41\text{MPa}$ ,  $Z_{eff}^* = 5$ ,  $\rho_{Cu} = 2.5 \times 10^{-8}\Omega\text{m}$ ,  $L_{via} = 0.07\mu\text{m}$ , and  $D_{eff} = 6.7 \times 10^{-9}\text{cm}^2/\text{s}$ . Some parameters that were unavailable were extracted from the literature. Specifically, the mean of  $E_a = 0.47\text{eV}$  [18], the standard deviation for the underlying Gaussian in the lognormal  $E_a$  was extracted from the Arrhenius plot of  $E_a$  vs.  $1/T$  in [12] as  $0.005\text{eV}$ , and  $B = 1\text{GPa}$  [1].

We run a Monte Carlo (MC) simulation to validate our analytical predictions of distribution of  $t_n$  and  $L_{void}$ . Our MC simulation uses  $10^6$  samples on a normal distribution of activation energy. Fig. 4 shows the values obtained from from the analytical model and the MC simulation. As in [2], the PDF for both the nucleation time and growth time is observed to follow a lognormal distribution. The close match that is seen between these curves is expected, since our analytical formulation makes no approximations.

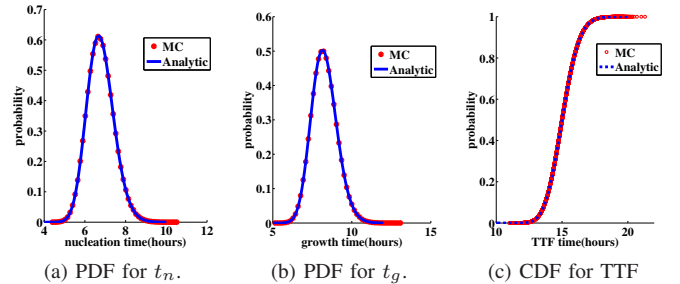


Fig. 4. Comparing analytical vs. MC distributions under accelerated aging.

Table I lists the expected mean and standard deviation for the failure parameters  $t_n$  and  $t_g$  obtained by our model against the FEA-based values mentioned in [2]. The values show a reasonable but not perfect match. The discrepancies could be attributed to factors such as the unavailability of some parameters in [2], and differences in the simulation setup, e.g., explicit consideration of grain size variation on a microstructural level. Clearly, our method is much faster than FEA since it merely involves the evaluation of an analytical expression.



Phase	Nucleation		Growth		
	$\mu, \sigma$	$\mu t_n$	$\sigma t_n$	$\mu t_g$	$\sigma t_g$
From [2]		8.5h	0.38h	8h	0.7h
Analytical		7.27h	0.74h	8.44h	0.86h

TABLE I  
COMPARISON OF OUR ANALYTICAL METHOD WITH [2].

2) *Statistical vs. deterministic approach*: Continuing under the assumptions in [2], where failure is defined as the time when  $L_{void} = L_{via}$ , the time to failure (TTF) is the sum of the nucleation time,  $t_n$ , and the growth time,  $t_g$ . We use the distribution of  $t_n$  and  $t_g$  to plot the distribution of TTF, and this distribution provides insights about the importance of incorporating the statistical behavior when modeling the effect of EM in circuits. From the CDF shown in Fig. 4(c), the time to failure, the 0.27%, 50% percentile and 99.73% points under accelerated aging are 12.73h, 15.68h, and 19.11h, respectively. This has two implications. First, it means that every wire has a nonzero probability of failure, which is not linked to its Blech length of  $jL$ . Indeed, wires that satisfy the Blech length criterion will fail: this has been observed experimentally in many of the references cited in this paper. Second, there is very low probability that the wire will fail in any manufactured part before 12.73h, and a probability that is so small implies that the wire is effectively immortal.

### B. Applying the Single-Wire Model at Normal Operating Conditions

Next, we evaluate the resistance change ratio,  $\Delta R/R$ , of a wire according to our probabilistic formulation in Equation (14). We use a similar setup as described in Section IV-A.1, but we change the temperature to normal operating conditions at 25°C and the current density to 0.5MA/cm<sup>2</sup>, and we return to the assumption that slit voids are not significant since we assume that redundant vias are used. As expected, the use of normal operating conditions for aging analysis results in a reduction in the rate of EM degradation as compared to an accelerated aging case, where TTF is of the order of several hours, to a scenario where the TTF values are of the order of several years.

Using Equation (14), we obtain the probability distribution of the  $\Delta R/R$  at an observation time of 12 years. Fig. 5 compares the CDF of the change in  $\Delta R/R$  as predicted by our formulation against MC simulations. The small mismatch in the two CDFs can be attributed to the error generated by our approximate moment matching method for estimating the difference of two lognormals.

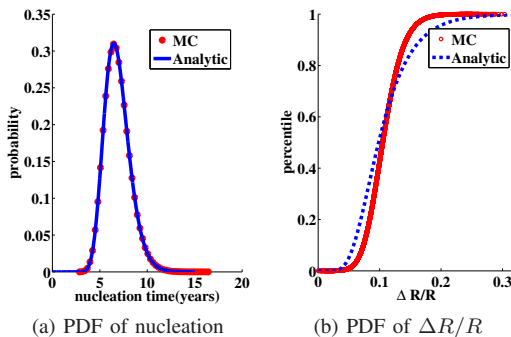


Fig. 5. Distribution of  $t_n$  and  $\Delta R/R$  under normal operation.

### C. Power grid simulation

Having verified our probabilistic resistance change formulation for a single wire against published data due to slit voids, we use our model to analyze the effect of resistance change due to EM at the circuit level. The analysis is based on DC analysis of a

set of power grid benchmarks from [23], enumerated in Table II. To perform a Monte Carlo simulation over the values of  $\Delta R$ , we implement a statistical importance sampling MC approach, described in Section III-E, in C++ and MATLAB. We analyze the interconnects for EM risk in the power grid and simulate the distribution of voltage drops. We run our stochastic MC simulation for 1200 iterations for the benchmarks. Using the runtime per iteration from Table II we can estimate realistic runtimes if a specialized power grid simulator were used; in our implementation, for convenience, we have used the matrix solver from MATLAB. This table indicates that the MC simulation can be carried out in a computationally efficient manner with a better solver.

Name	Total # wires	Runtime [24]	Memory in MB [24]	Expected runtime 1200 iterations
PG1	30027	0.20s	4MB	4min
PG2	208325	1.42s	72MB	29min
PG3	1401572	8.29s	172MB	166min
PG4	1560645	19.35s	606MB	387min
PG5	1076848	9.36s	296MB	187min

TABLE II  
LIST OF P/G BENCHMARKS EVALUATED IN THIS PAPER.

We set the observation time to 2.5 years for PG1–PG4, consistent with the results reported in [6]. For PG5, which shows a low nominal voltage drop after 2.5 years, the observation time is set to 5 years. All circuits are evaluated at a temperature of 105°C.

To compare results of our statistical framework against previous work with deterministic mortality approach, we predict the set of mortal wires using the Blech-length [5] criterion. In the second and third columns of Table III, for each benchmark, we compare the results of the newly formulated statistical approach (“Stat.”) with those from a deterministic Blech-length approach (“Blech”). As stated earlier, for our approach, “mortality” is defined in terms of a  $3\sigma$  deviation from the mean in the underlying normal of the lognormal. From the table, it can be seen that our implementation shows that a larger number of wires must be considered mortal under the probabilistic formulation, as compared to the deterministic Blech-length based approach. This is entirely expected, and makes the case for not using the Blech length criterion for CuDD interconnects.

Next, we evaluate the variation in the IR drop due to the statistical distribution of EM. This distribution is observed to be non-Gaussian, and we compute the spread of the distribution by taking the difference (referred to as  $\Delta V$ ) between the 99.73 and 0.27 percentile points. We characterize the normalized spread by expressing  $\Delta V$  as a fraction of the median (i.e., 50 percentile point) of  $V$ .

The next column of Table III presents the largest realistic normalized resistance change, estimated as the point that is three standard deviations from the mean of the underlying Gaussian of the lognormal  $\Delta R$ . This data indicates the spread in resistance change due to EM. The subsequent columns show the variance in  $\Delta V/V$ , and the corresponding median,  $V_{50\%}$ , for the nodes in the network that have the largest variance and largest median, respectively. In each case, our approach provides a *precise* metric for the impact of EM on the variation in power grid voltage.

Most significantly, this table demonstrates that contrary to the assumptions in many other works on power grid analysis that assume that a failing wire causes a failed circuit, the power grid may continue to work even if a single wire fails. This is exemplified, for example, by PG2, where, in spite of a large spread in the resistance change in the wire, the spread for the IR drop is small.

Finally, we run MC simulations for PG5 at different observation times,  $t_o$ , to analyze how the worst case IR drop varies with time. For three values of  $t_o$ , Fig. 6 shows the CDF of IR drop for the node having largest median IR drop value. For  $t_o = 5$  years, the CDF is to

Ckt	Number of mortal wires		Largest $\Delta R/R$ (in %)	At largest variance node		At largest median node	
	Stat.	Blech		$V_{50\%}$	$\Delta V/V$	$V_{50\%}$	$\Delta V/V$
PG1	16932	13272	218.4	0.73V	15.4%	0.89V	8.2%
PG2	81393	26723	113.6	0.39V	4.7%	0.50V	0.8%
PG3	63231	34998	65.9	0.19V	6.2%	0.24V	0.1%
PG4	140133	79737	36.4	0.006V	7.8%	0.01V	4.7%
PG5	131094	38746	120.4	0.035V	11.5%	0.07V	1.7%

TABLE III  
RESULTS OF MONTE CARLO SIMULATION

the left, and it moves rightwards as the observation time increases. For a given threshold value (e.g., 70mV) on the x-axis, it is clear that the probability of seeing this value of IR drop increases with time, since a larger fraction crosses the threshold value.

Fig. 6 provides further insight about the circuit behaviour with respect to time. If we fix the threshold IR drop as 70mV, there can be many wire failures that result in an increase in the resistance, but almost all samples have IR drop below 70mV at  $t_o = 5$  years. For a slightly higher threshold value of 80mV (off the scale), there is a high probability that the power grid will still be functional, for an even higher observation time of 7.5 years – even though the circuit does see wires that fail within 7.5 years. This indicates that for a given specification, the circuit lifetime, which is characterized by a threshold IR drop, can be longer than the lifetime of the EM-degraded wire, i.e., an individual wire whose resistance exceeds a specific threshold. In other words, the power grid is robust to some EM failures in individual wires.

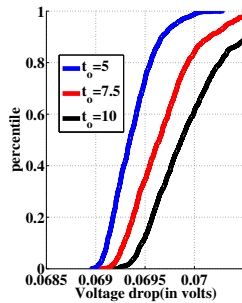


Fig. 6. CDF plots for worst node IR drop at various observation times.

## V. CONCLUSION

We have developed a method for EM analysis of power grids taking into account two effects that were neglected in past work: first, that EM is a probabilistic phenomenon for CuDD interconnects, and second, that the power grid has inherent resilience to EM failures. Our results indicate that both effects are substantial.

## REFERENCES

- [1] C. M. Tan, *Electromigration in ULSI Interconnections*. World Scientific, Dec. 2010.
- [2] R. L. de Orio, H. Ceric, and S. Selberherr, "A compact model for early electromigration failures of copper dual-damascene interconnects," *Microelectronics Reliability*, vol. 59, no. 9–11, pp. 1573–1577, 2011.
- [3] S. P. Hau-Riege, "Probabilistic immortality of Cu damascene interconnects," *Journal of Applied Physics*, vol. 91, no. 4, pp. 2014–2022, 2002.
- [4] J. R. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," *Proceedings of the IEEE*, vol. 57, pp. 1587–1594, Sept. 1969.
- [5] I. A. Blech, "Electromigration in thin aluminum films on titanium nitride," *Journal of Applied Physics*, vol. 47, no. 4, pp. 1203–1208, 1976.
- [6] D. Li and M. Marek-Sadowska, "Variation-aware electromigration analysis of power/ground networks," *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 571–576, Nov. 2011.
- [7] S. M. Alam, C. L. Gan, F. L. Wei, C. V. Thompson, and D. E. Troxel, "Circuit-level reliability requirements for Cu metallization," *IEEE Transactions on Devices and Materials Reliability*, vol. 5, no. 3, pp. 522–531, 2005.

- [8] M. A. Korhonen, P. Borgesen, K. N. Tu, and C. Y. Li, "Stress evolution due to electromigration in confined metal lines," *Journal of Applied Physics*, vol. 73, no. 8, pp. 3790–3799, 1993.
- [9] A. Heryanto, K. L. Pey, Y. K. Lim, W. Liu, N. Raghavan, J. Wei, C. L. Gan, M. K. Lim, and J. B. Tan, "The effect of stress migration on electromigration in dual damascene copper interconnects," *Journal of Applied Physics*, vol. 109, no. 1, pp. 013716–1–013716–9, 2011.
- [10] C. K. Hu, R. Rosenberg, and K. Y. Lee, "Electromigration path in Cu thin-film lines," *Applied Physics Letters*, vol. 74, no. 20, pp. 2945–2947, 1999.
- [11] E. Liniger, L. Gignac, C.-K. Hu, and S. Kaldor, "In situ study of void growth kinetics in electroplated Cu lines," *Journal of Applied Physics*, vol. 92, no. 4, pp. 1803–1810, 2002.
- [12] Z. S. Choi, R. M. Monig, and C. V. Thompson, "Activation energy and prefactor for surface electromigration and void drift in Cu interconnects," *Journal of Applied Physics*, vol. 102, no. 8, pp. 083509–1–083509–9, 2007.
- [13] C. Christiansen, B. Li, M. Angyal, T. Kane, V. M. Y. Y. Wang, and S. Yao, "Electromigration-resistance enhancement with CoWP or CuMn for advanced Cu interconnects," in *IEEE International Reliability Physics Symposium*, pp. 3E.3.1–3E.3.5, 2011.
- [14] M. Hauschildt, M. Gall, S. Thrasher, P. Justison, R. Hernandez, and H. Kawasaki, "Statistical analysis of electromigration lifetimes and void evolution," *Journal of Applied Physics*, vol. 101, no. 4, pp. 682–687, 2007.
- [15] L. Doyen, X. Federspiel, L. Arnaud, F. Terrier, Y. Wouters, and V. Girault, "Electromigration multistress pattern technique for copper drift velocity and black's parameters extraction," in *IEEE International Reliability Workshop Final Report*, pp. 74–78, Oct. 2007.
- [16] V. M. Dwyer, "Modeling the electromigration failure time distribution in short copper interconnects," *Journal of Applied Physics*, vol. 1004, no. 5, pp. 053708–1–053708–6, 2008.
- [17] J. R. Lloyd and J. Kitchin, "The electromigration failure distribution," *Journal of Applied Physics*, vol. 69, no. 4, pp. 2117–2127, 1991.
- [18] B. H. Jo and R. W. Vook, "In-situ ultra-high vacuum studies of electromigration in copper films," *Thin Solid Films*, vol. 262, no. 1–2, pp. 129–134, 1995.
- [19] A. A. Abu-Dayya and N. C. Beaulieu, "Comparison of methods of computing correlated lognormal sum distributions and outages for digital wireless applications," in *IEEE Vehicular Technology Conference*, pp. 175–179, 1994.
- [20] B. Li, T. D. Sullivan, and T. C. Lee, "Line depletion electromigration characterization of Cu interconnects," *IEEE Transactions on Device and Materials Reliability*, vol. 4, pp. 80–85, Mar. 2004.
- [21] Y.-J. Park, P. Jain, and S. Krishnan, "New electromigration validation: Via node vector method dual-damascene Cu interconnect trees," in *IEEE International Reliability Physics Symposium*, pp. 6A.1.1–6A.1.7, 2003.
- [22] C. L. Gan, C. V. Thompson, K. L. Pey, and W. K. Choi, "Experimental characterization and modeling of the reliability of three-terminal dual-damascene Cu interconnect trees," *Journal of Applied Physics*, vol. 94, no. 2, pp. 1222–1228, 2003.
- [23] S. R. Nassif, "Power grid analysis benchmarks," in *Proceedings of the Asia-South Pacific Design Automation Conference*, 2008.
- [24] Z. Zeng, T. Xu, Z. Feng, and P. Li, "Fast static analysis of power-grids: algorithms and implementation," in *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pp. 488–493, 2011.
- [25] Z. S. Choi, R. M. Monig, and C. V. Thompson, "Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects," *Applied Physics Letters*, vol. 102, no. 8, pp. 241913–1–241913–3, 2007.
- [26] R. L. de Orio, H. Ceric, and S. Selberherr, "The effect of copper grain size statistics on the electromigration lifetime distribution," *Simulation of Semiconductor Processes and Devices*, pp. 1–4, 2009.