Enhancement-Mode Buried-Channel $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ MOSFETs With High-κ Gate Dielectrics

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***Abstract*—The operation of long- and short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$-channel MOSFETs with high-κ gate dielectrics are demonstrated for the first time. The devices utilize an undoped buried-channel design. For a gate length of 5 μm, the long-channel devices have $V_t = +0.25$ V, a subthreshold slope of 150 mV/dec, an equivalent oxide thickness of 4.4 +/− 0.3 nm, and a peak effective mobility of 1100 $cm^2/V \cdot s$. For a gate length of 260 nm, the short-channel devices have $V_t = +0.5$ V and a subthreshold slope of 200 mV/dec. Compared with Schottky-gated high-electron-mobility transistor devices, both long- and short-channel MOSFETs have two to four orders of magnitude lower gate leakage.**

***Index Terms*—Buried channel, enhancement mode, high-κ, InGaAs, MOSFET.**

I. Introduction

THE III–V semiconductors are receiving renewed attention for use as channel materials for advanced ultra-large-scale integration (ULSI) digital logic applications due to their high electron mobility [1]. InGaAs HEMTs grown on InP substrates have produced g_m values over 2 S/mm [2], as well as an f_T of 562 GHz [3]. InGaAs-channel Schottky-gated HEMTs have also recently been benchmarked against Si MOSFETs and shown to compare favorably in terms of power-delay product [4]. Despite these promising results, for ULSI logic applications, InGaAs-channel FETs will ultimately need to incorporate high-κ insulating gate dielectrics in order to meet International Technology Roadmap for Semiconductors leakage requirements.

Previous work on InGaAs-channel MOSFETs has mainly focused on surface-channel device geometries [5], but these devices would require the formation of a very high quality semiconductor/dielectric interface in order to preserve low interface-state density near the surface-layer conduction-band edge. For this reason, a buried-channel MOSFET design may be preferable, as shown in Fig. 1, to relax the requirements for low interface-state density near the surface-semiconductor conduction-band edge, as well as improve the carrier mobility. Recently, Passlack *et al.* [6] proposed a buried-channel structure based upon pseudomorphically strained low-In-content InGaAs channels and $Ga_2O_3/(Gd_xGa_{1-x})_2O_3$ dielectrics. In our previous work, we demonstrated the operation of $In_{0.7}Ga_{0.3}As$ buried-channel MOSFETs with HfO_2 gate dielectrics [7]. However, the structure used in that work was not optimal due to its large surface-to-channel distance and δ-doping above the quantum well. In this letter, we report both long- and short-channel enhancement-mode MOSFETs that utilize an undoped-buried-channel design. These devices display good saturation, low leakage, and high ON-state to OFF-state current ratio.

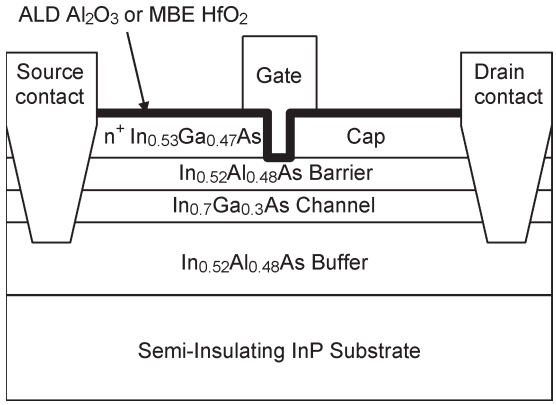

Fig. 1. Schematic cross-sectional diagram of an enhancement-mode $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MOSFET with 7-nm ALD Al_2O_3 (short-channel device) or 10 nm MBE HfO_2 (long-channel device).

II. Device Fabrication

In this letter, an undoped $In_{0.7}Ga_{0.3}As/In_{0.52}Al_{0.48}As$ quantum well layer structure was used, as shown in Fig. 1. The layer structure was grown on a semi-insulating InP substrate by molecular beam epitaxy (MBE) and consisted of a 300-nm $In_{0.52}Al_{0.48}As$ buffer layer, a 10-nm $In_{0.7}Ga_{0.3}As$ strained quantum well, a 10-nm $In_{0.52}Al_{0.48}As$ top barrier layer, and a 25-nm n^+-$In_{0.53}Ga_{0.47}As$ cap layer. Aside from the top $In_{0.53}Ga_{0.47}As$ layer, which was etched away in the gate region, all layers were not intentionally doped.

Manuscript received January 26, 2007; revised March 15, 2007. The review of this letter was arranged by Editor J. del Alamo.

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Digital Object Identifier 10.1109/LED.2007.896813

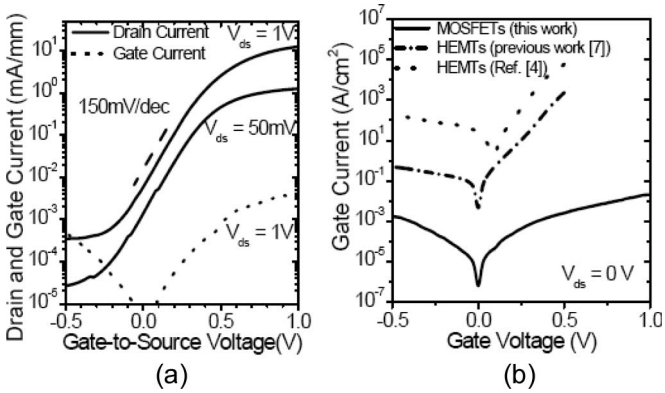

Fig. 2. Long buried-channel $In_{0.70}Ga_{0.30}As/In_{0.52}Al_{0.48}As$ MOSFET with 10 nm MBE HfO_2, $L_g = 5$ μm. (a) Subthreshold characteristics at $V_{\rm ds} = 50$ mV and 1 V, and gate leakage characteristics at $V_{\rm ds} = 1$ V. (b) Gate leakage characteristics at $V_{\rm ds} = 0$ V, with comparison to the previous HEMT devices [4], [7].

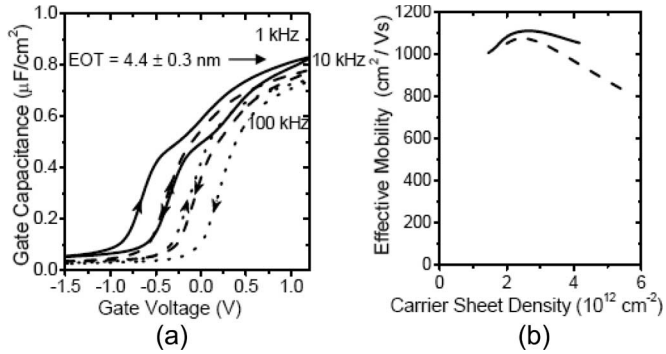

Fig. 3. (a) Gate capacitance versus voltage characteristics of a buried-channel MOSFET with 10 nm MBE HfO_2 at frequencies of 1, 10, and 100 kHz. (b) Effective mobility versus carrier sheet density using 100 kHz C–V data, which were extracted for both (solid line) decreasing and (dashed line) increasing V_g.

Long- and short-channel MOSFETs with metal gates and high-κ dielectrics have been fabricated using the above layer structure. Long-channel ring-shaped MOSFETs were made by patterning the heterostructure using optical lithography followed by selectively etching the InGaAs cap layer to form a gate recess area. The sample was then etched in diluted hydrofluoric acid (HF) before loading into an MBE chamber, where the surface was further cleaned using atomic hydrogen. Following the surface clean, 10 nm HfO_2 was deposited by MBE, and ohmic contacts were then formed by selectively etching the gate dielectric and subsequently depositing and lifting off the Au/Ge/Ni metal, which was then followed by annealing. The gate metal was formed by optical lithography patterning, Al deposition, and subsequent liftoff. The short-channel device fabrication included an additional mesa isolation step before the gate lithography. In addition, the gate recess was patterned by electron-beam lithography, where gate lengths as short as 260 nm were fabricated. After forming Au/Ge/Ni source/drain contacts, the short-channel device was etched in diluted HF and then immediately loaded into an atomic layer deposition (ALD) chamber, where 7 nm Al_2O_3 was deposited at 300 °C. Finally, the gate metal was formed by evaporation and liftoff. Two different work-function materials, Al or Pt, were used as gates to adjust the threshold voltage.

III. Long-Channel MOSFETs

The subthreshold characteristic of a typical buried $In_{0.7}Ga_{0.3}As$-channel MOSFET with $L_g = 5$ μm is shown in Fig. 2(a). The device operates in the enhancement mode and has a threshold voltage of +0.25 V, as determined by linear extrapolation from the peak transconductance at $V_{\rm ds} = +50$ mV. The drain current ON–OFF ratio, which is defined as the ratio between the drain current at ON-state and the drain current at OFF-state, is $\sim 10^4$, and the subthreshold slope is 150 mV/dec. Extrinsic transconductance values as high as 42 mS/mm have been observed at $V_{\rm gs} = +0.95$ V and $V_{\rm ds} = +2$ V. The gate leakage characteristic of the same device is shown in Fig. 2(b), and the results are compared with HEMTs from our previous work [7] and the recent work from Kim *et al.* [4]. The gate leakage current density of the MOSFET is more than two orders of magnitude lower than that of both HEMT devices.

The gate capacitance–voltage results for the MOSFETs are shown in Fig. 3(a). The equivalent oxide thickness (EOT) extracted from the C_g–V_g characteristics at a strong forward bias ($V_g = +1.2$ V) is 4.4 +/− 0.3 nm—a value that agrees fairly well with expectations for the given device dimensions. The C–V hysteresis in Fig. 3(a) also shows on $I_{\rm ds}$ versus $V_{\rm gs}$, which is about 0.2–0.25 V and shifts V_t accordingly. The interface-state density obtained from the conductance method is in the high 10^{12} cm^{-2} eV^{-1} range, and this value could account for the nonideal subthreshold slope in our devices. In addition, despite the long channel length, the device resistance was impacted by an external series resistance, which was measured to be 20 Ω mm. The high value of the extrinsic resistance is due, in part, to the nonoptimized contact formation.

After correcting for the series resistance ($R_{\rm ext}$), the effective drift mobility and the sheet density were calculated from the C_g versus V_g (100 kHz) and linear I_d–V_g characteristics ($V_{\rm ds} = +50$ mV). The resulting mobility versus sheet density plot is shown in Fig. 3(b). The value of extracted mobility shows very little dependence on the V_g sweep direction. A peak mobility of 1100 cm^2/V · s (980 cm^2/V · s without an $R_{\rm ext}$ correction) was determined at a carrier density of 2.6×10^{12} cm^{-2}. The extracted effective channel mobility is the highest reported value for enhancement-mode III–V MOSFETs and is also much higher than that of the Si MOSFET with high-κ gate dielectrics. However, the *effective* channel mobility is much smaller than the reported Hall-effect mobility of $In_{0.7}Ga_{0.3}As$ [3] due to high $D_{\rm it}$ at the dielectric/InAlAs interface. Further improvements should be possible through optimization of the interface properties.

IV. Short-Channel MOSFETs

The dc output characteristics of the short-channel MOSFETs ($L_g = 260$ nm) are shown in Fig. 4(a). The devices show good saturation and pinchoff characteristics, though a significant series resistance was observed. The gate leakage of the

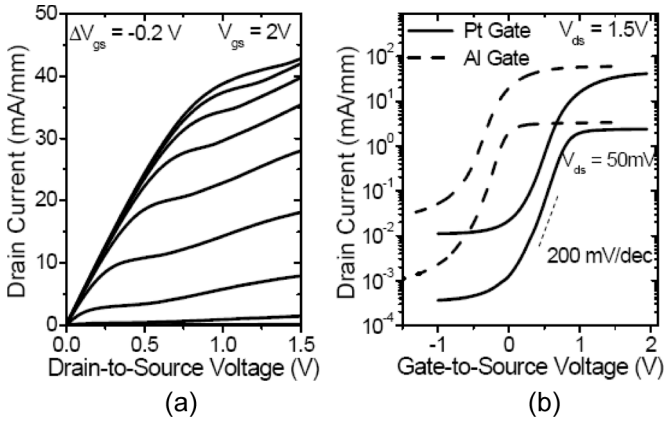

Fig. 4. (a) Output characteristics of a short-channel MOSFET with 7 nm ALD Al_2O_3, $L_g = 260$ nm, and a gate to source/drain contact distance of 2.4 μm. (b) Subthreshold characteristics of an enhancement-mode and a depletion-mode short-channel MOSFET with $L_g = 260$ nm and a gate to source/drain contact distance of 2.4 μm.

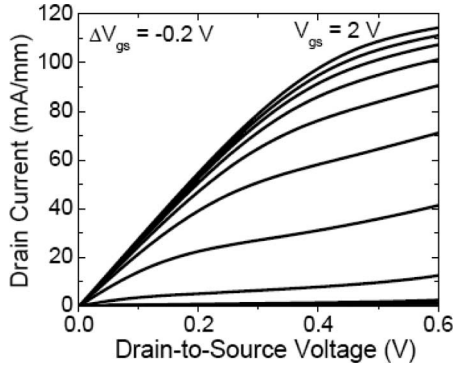

Fig. 5. Output characteristics of a short-channel MOSFET with 7 nm ALD Al_2O_3, $L_g = 260$ nm, and a gate to source/drain contact distance of 0.4 μm.

short-channel devices remains very low and is four orders of magnitude lower than that of the previous HEMT devices [4], [7]. Depending upon the gate metal utilized, the devices can be made to operate in either enhancement mode $(V_t = +0.5\ \text{V})$ by using a high-work-function Pt gate, or depletion mode $(V_t = -0.2\ \text{V})$ by using a low-work-function Al gate, as shown in Fig. 4(b). The difference between the threshold voltage, however, is smaller than the work-function difference between Pt and Al, presumably due to interface traps. The enhancement-mode devices have a current ON–OFF ratio of $\sim 10^3$ and a subthreshold slope of $\sim$200 mV/dec. The large series resistance observed in Fig. 4(a) is primarily due to the nonoptimized source/drain contact formation and the large distance (2.4 μm) between the gate and the Au/Ge/Ni contacts.

A device with the same gate length $(L_g = 260\ \text{nm})$, but with reduced gate to source/drain contact distance (0.4 μm), has three times higher drive current, as shown in Fig. 5. The maximum extrinsic transconductance for this device is 157 mS/mm at $V_{\text{ds}} = +0.6$ V and $V_{\text{gs}} = +0.65$ V. However, the performance is still limited by the parasitic series resistance. Much higher transconductance and drive current are expected with reduced series resistance, as well as further EOT scaling.

V. Discussion and Conclusion

The results are encouraging due to the fact that good modulation of the $In_{0.7}Ga_{0.3}As$ channel with a positive threshold voltage is achieved despite the fact that little optimization of the high-κ dielectric/semiconductor interface was performed. The results support the hypothesis that the buried-channel design is less sensitive to III–V semiconductor/dielectric interface nonidealities because it allows the device to operate in a regime where the surface Fermi level is far from the band edges of the surface semiconductor layer. Furthermore, different from the previous work [6], [7], this layer structure does not have a top-side δ-doping layer, which enhances the vertical scalability in order to approach the EOT values that can be achieved in surface channel devices. The vertical scalability is crucial in order to meet the EOT requirement for the 22 nm and beyond CMOS technology. However, much lower external resistance values will be needed in order to evaluate the dc performance capability of the InGaAs buried-channel MOSFET properly. In addition, further EOT scaling is necessary to determine the degree to which high mobility can be maintained as the top barrier layer thickness is reduced and, ultimately, find the optimum tradeoff between mobility and gate capacitance in these structures.

In conclusion, we have demonstrated long- and short-channel enhancement-mode $In_{0.7}Ga_{0.3}As$ MOSFETs with high-κ gate dielectrics for the first time. The devices show good output and pinchoff characteristics, have two to four orders of magnitude lower gate leakage than Schottky-gated devices, and a peak effective mobility of 1100 $\text{cm}^2/\text{V}\cdot\text{s}$. These results are promising for realizing scalable InGaAs-channel MOSFETs suitable for VLSI applications.

Acknowledgment

The authors would like to thank G. Shahidi for technical guidance and R. Sandstrom for fabrication support.

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