CMOS Inverter

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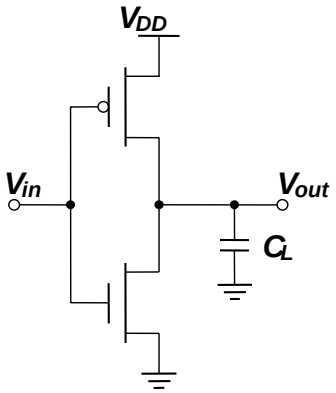
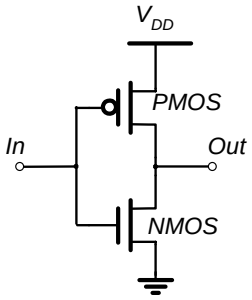
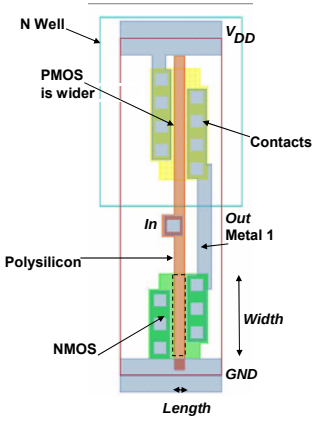
The CMOS Inverter: A First Glance



CMOS Inverter

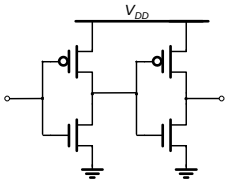


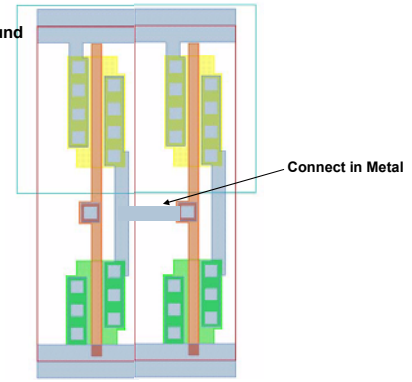


Two Inverters

Share power and ground

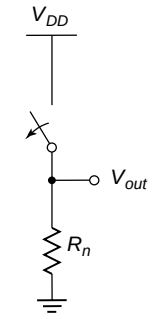
Abut cells



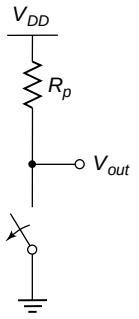


Voltage Transfer Characteristics

CMOS Inverter First-Order DC Analysis



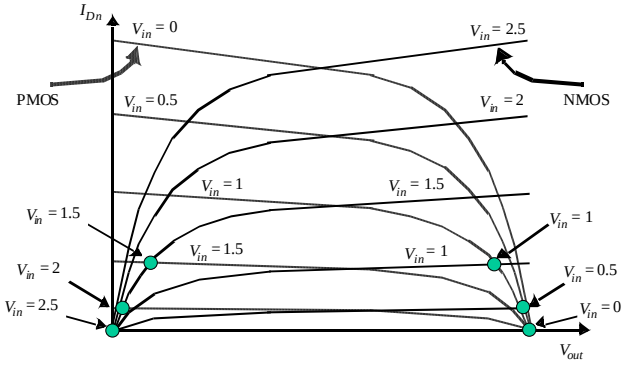
$V_{in} = V_{DD}$



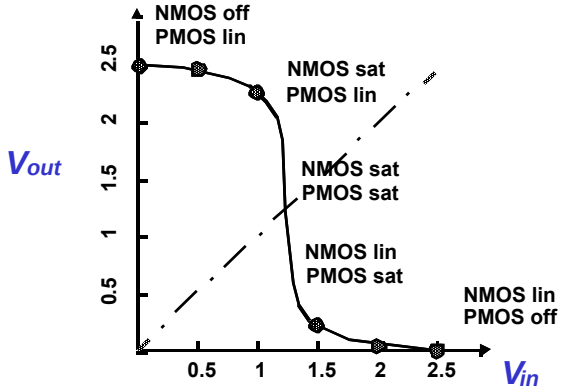
$V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

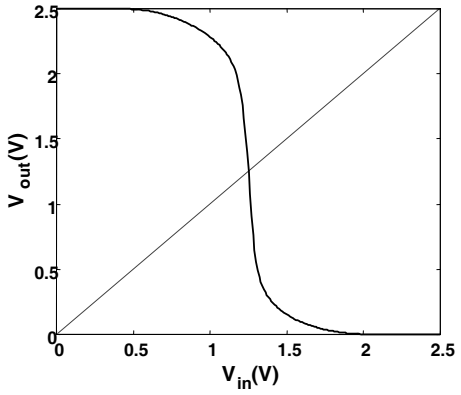
CMOS Inverter Load Characteristics



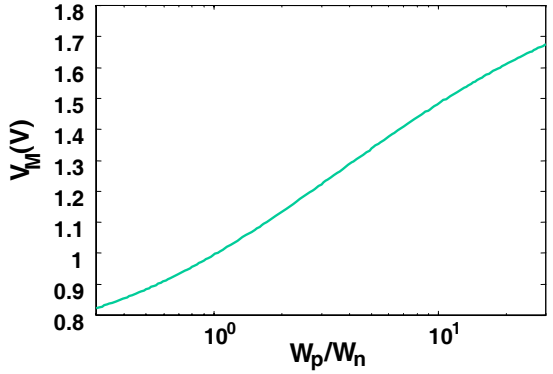
CMOS Inverter VTC



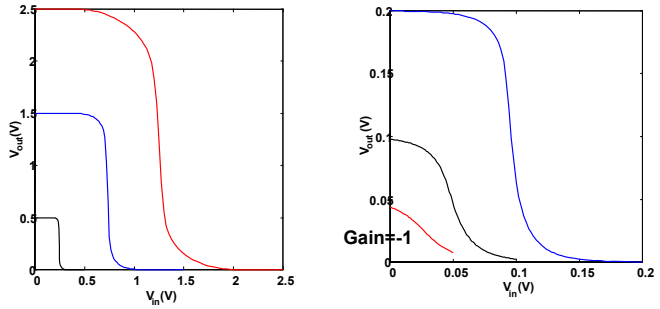
Simulated Inverter VTC (hspice)



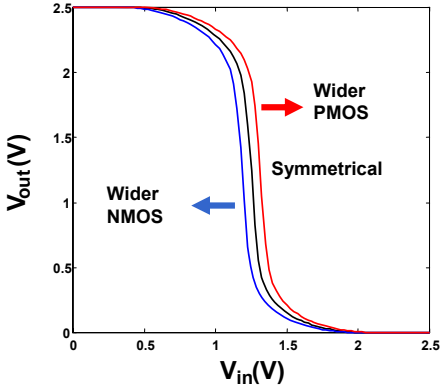
Switching Threshold as a Function of Transistor Ratio



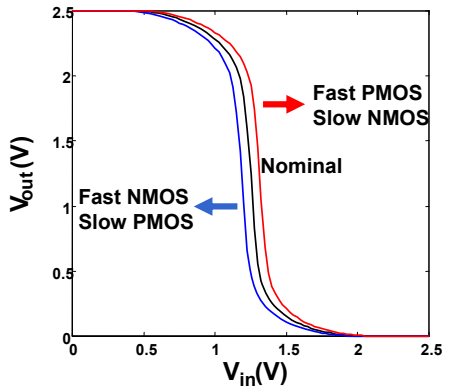
VTC as a function of VDD



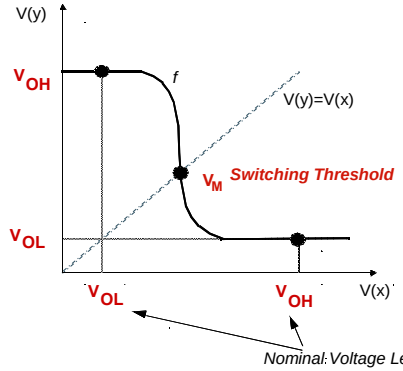
Impact of Sizing



Impact of Process Variations

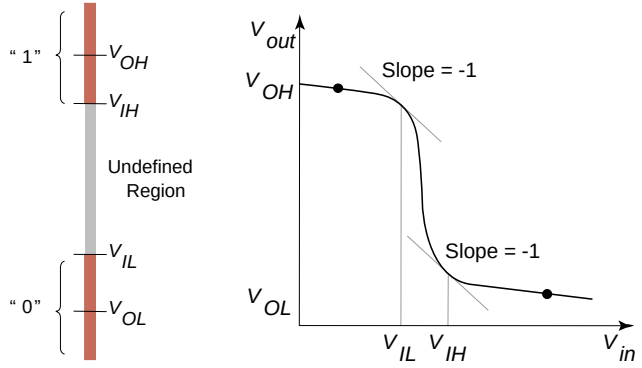


DC Operation
Voltage Transfer Characteristic

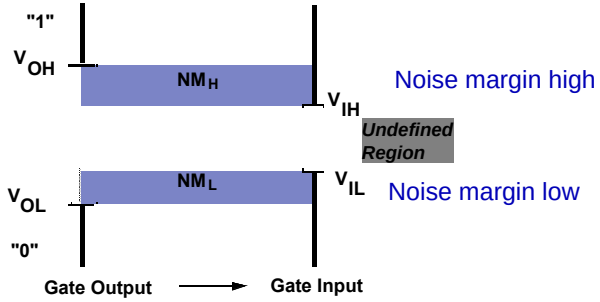


VOH = *f*(VOL)
VOL = *f*(VOH)
VM = *f*(VM)

Mapping between analog and digital signals



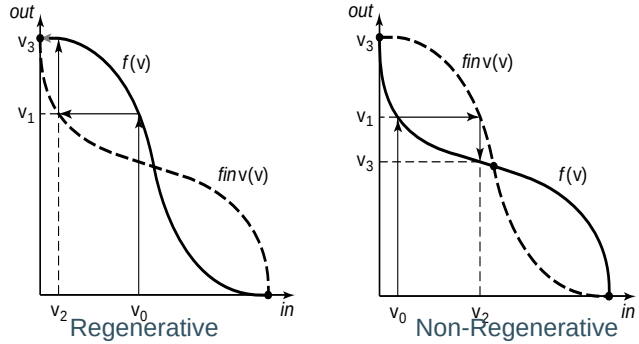
Definition of Noise Margins



Example: CMOS Inverter DC Properties

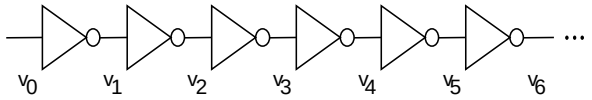
- $V_{OH} = V_{DD} = 2.5V$
- $V_{OL} = 0V$
- $V_{IL} = 1.05V$
- $V_{IH} = 1.45V$
- $N_{MH} = 1.05V$
- $N_{ML} = 1.05V$
- $V_M = 1.2V$

Regenerative Property

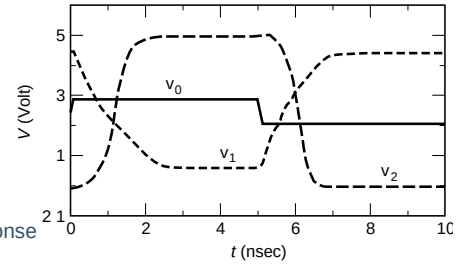


Regenerative Non-Regenerative

Regenerative Property



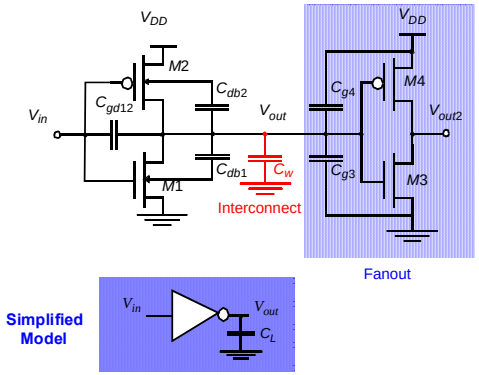
A chain of inverters



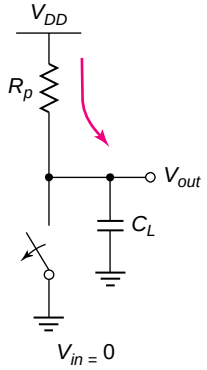
Simulated response

Propagation Delay

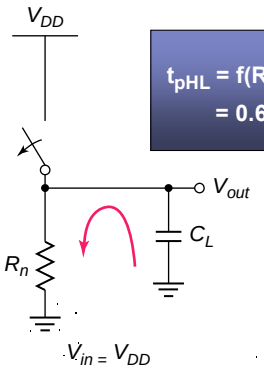
Computing the Capacitances



CMOS Inverter: Transient Response



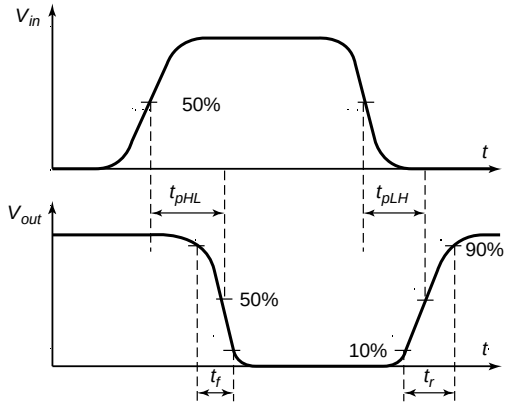
(a) Low-to-high



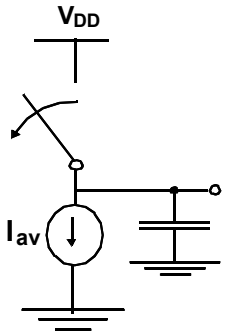
(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

Delay Definitions

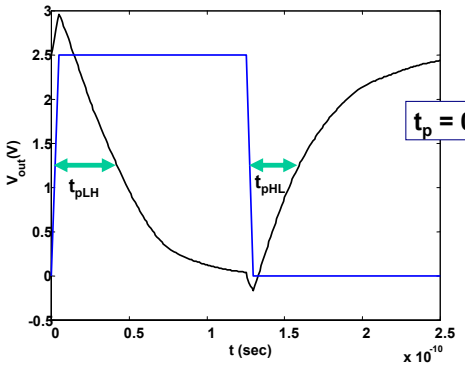


CMOS Inverter Propagation Delay



$$t_{pHL} = \frac{C_L V_{dd}/2}{I_{av}}$$

Transient Response

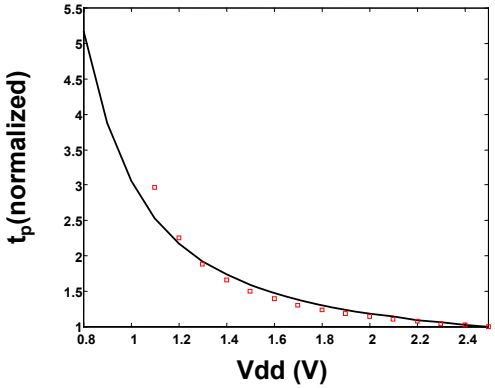


$t_p = 0.69\ C_L\ (R_{eqn}+R_{eqp})/2$

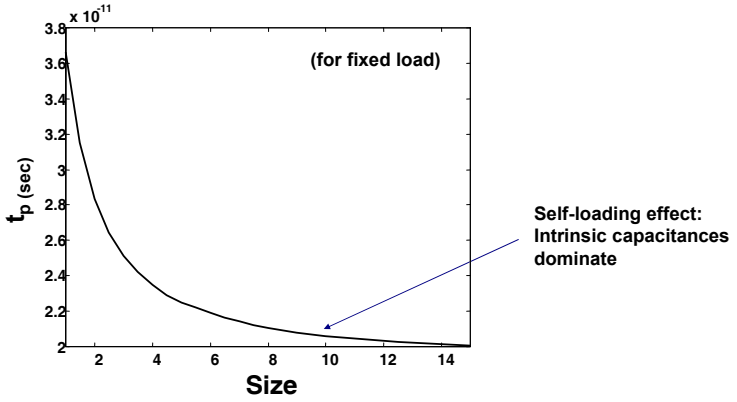
Design for Performance

- Keep capacitances small
- Increase transistor sizes
  - watch out for self-loading!
- Increase V_{DD}

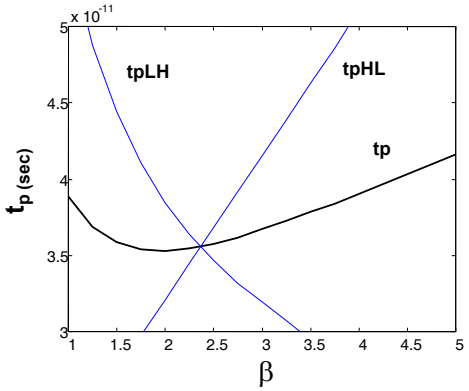
Delay as a function of V_{DD}



Device Sizing

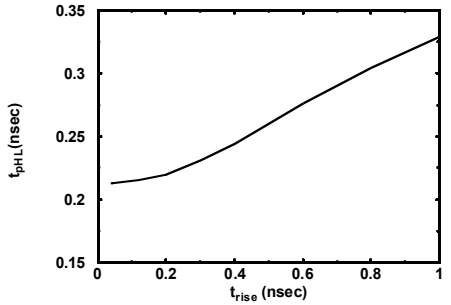


NMOS/PMOS ratio



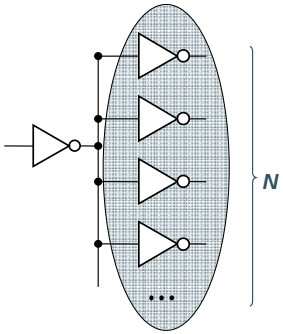
$\beta = W_p/W_n$

Impact of Rise Time on Delay

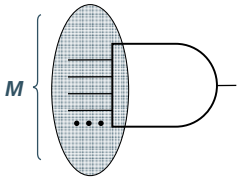


$t_p = t_{step(i)} + ht_{step(i\text{-}1)}$

Fan-in and Fan-out

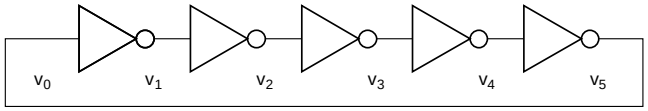


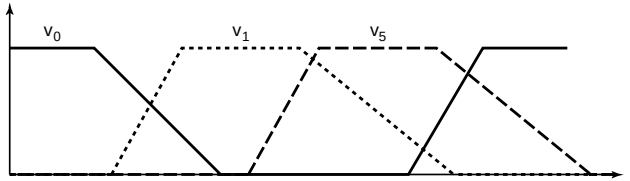
Fan-out *N*



Fan-in *M*

Ring Oscillator





$T = 2 \times t_p \times N$

CMOS Properties

- Full rail-to-rail swing
- Symmetrical VTC
- Propagation delay function of load capacitance and resistance of transistors
- No static power dissipation (ignoring leakage current)
- Direct path current during switching