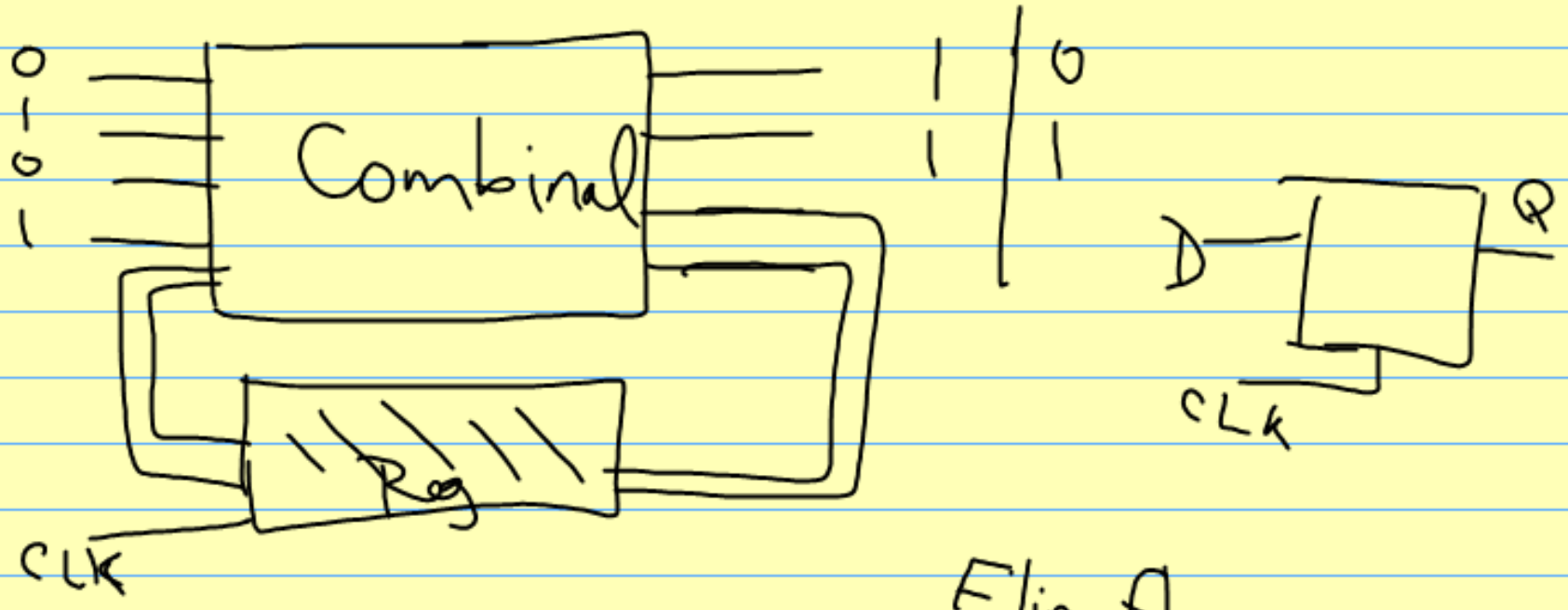
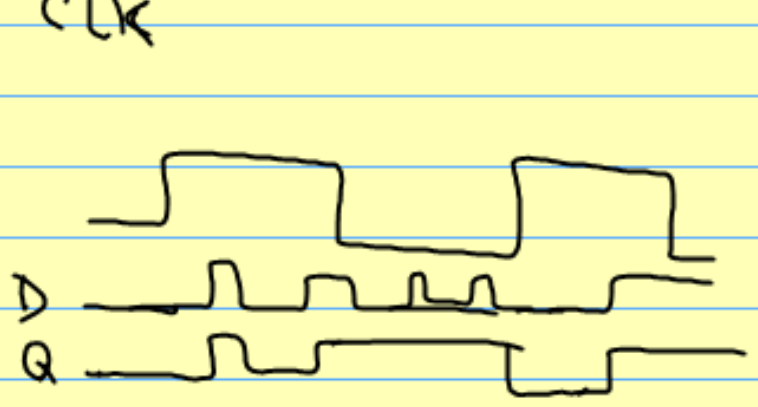
Sequential Logic





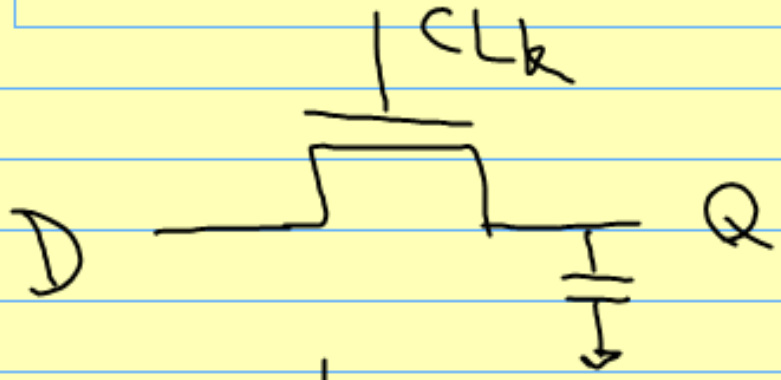
Flip-flop

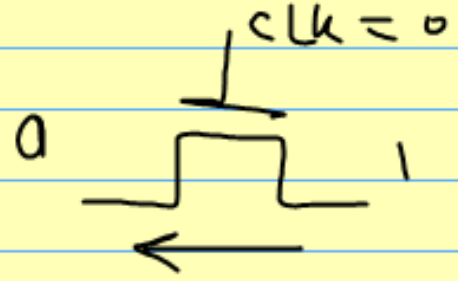
Latch

Reg

Clock edge

Memory Cell





\+ simple

\+ area

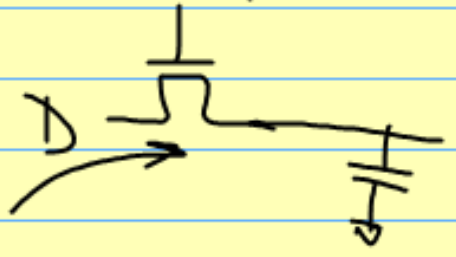
fast?

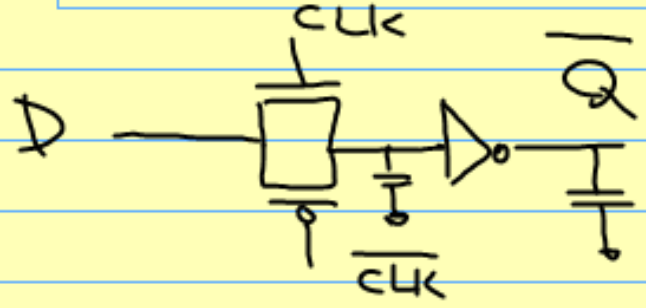
— charge leaks

— Float ⇒ noise

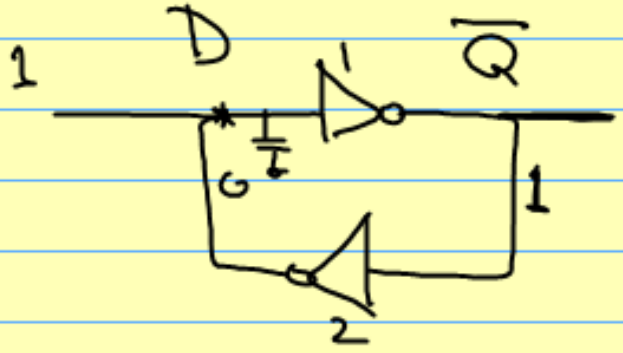
— Diffusion

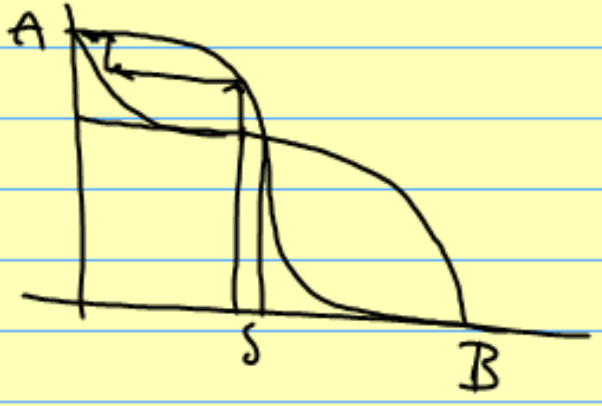
— V_t drop



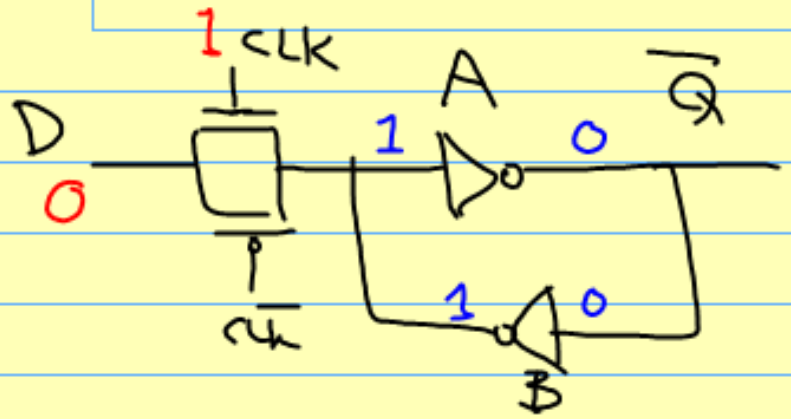


+ Restore weak D
+ Capacitive Coup D
– noise





SRAM cell α-release!



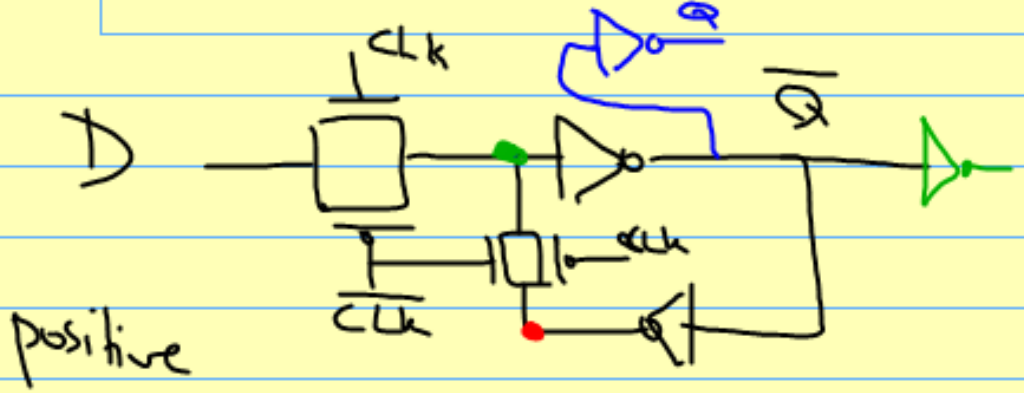
Read: $\overline{Q}$

Write: D ← value

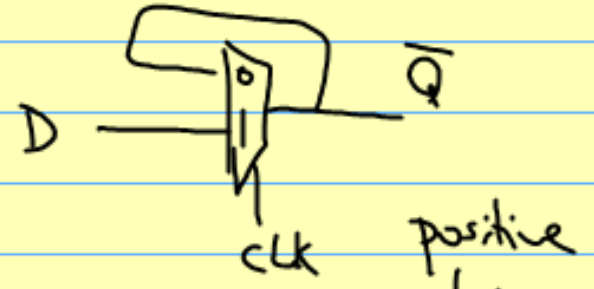
CLK ← 1

- careful sizing (gate B's pmos, nmos vs D)
  - ⇒ clock period
- Delay
- \+ robust

SRAM Cell (Mux-based Latch)



optional path

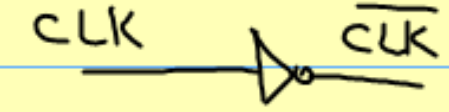


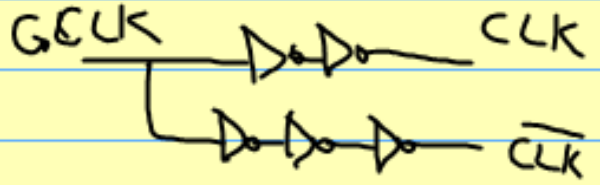
+ Robust++

+ popular

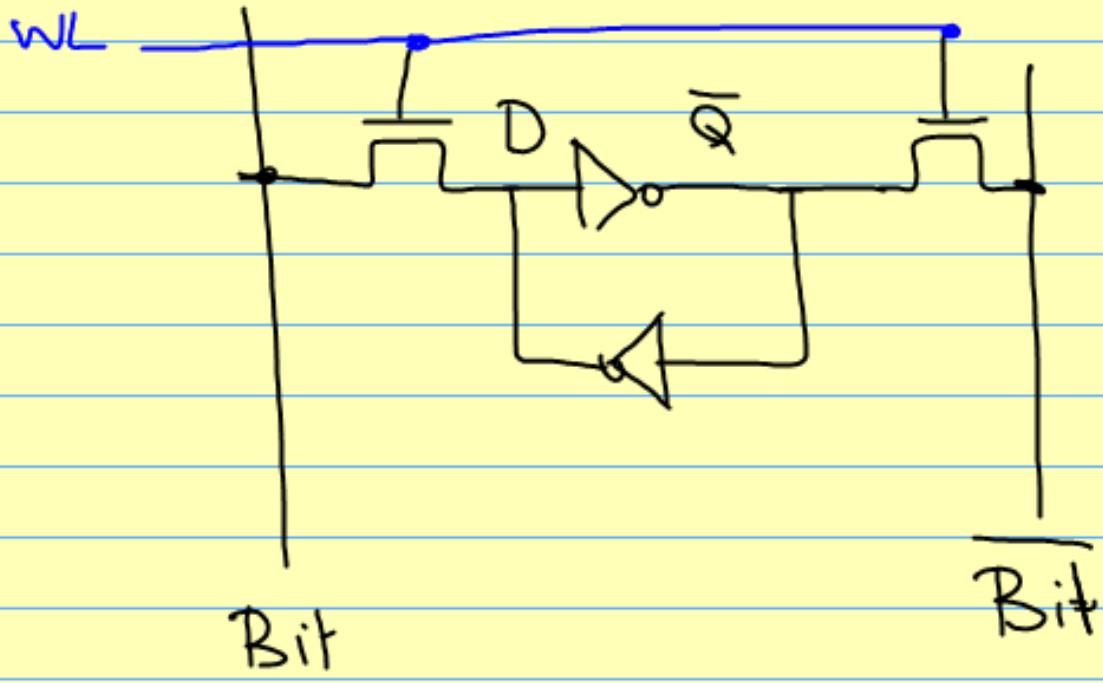
– area

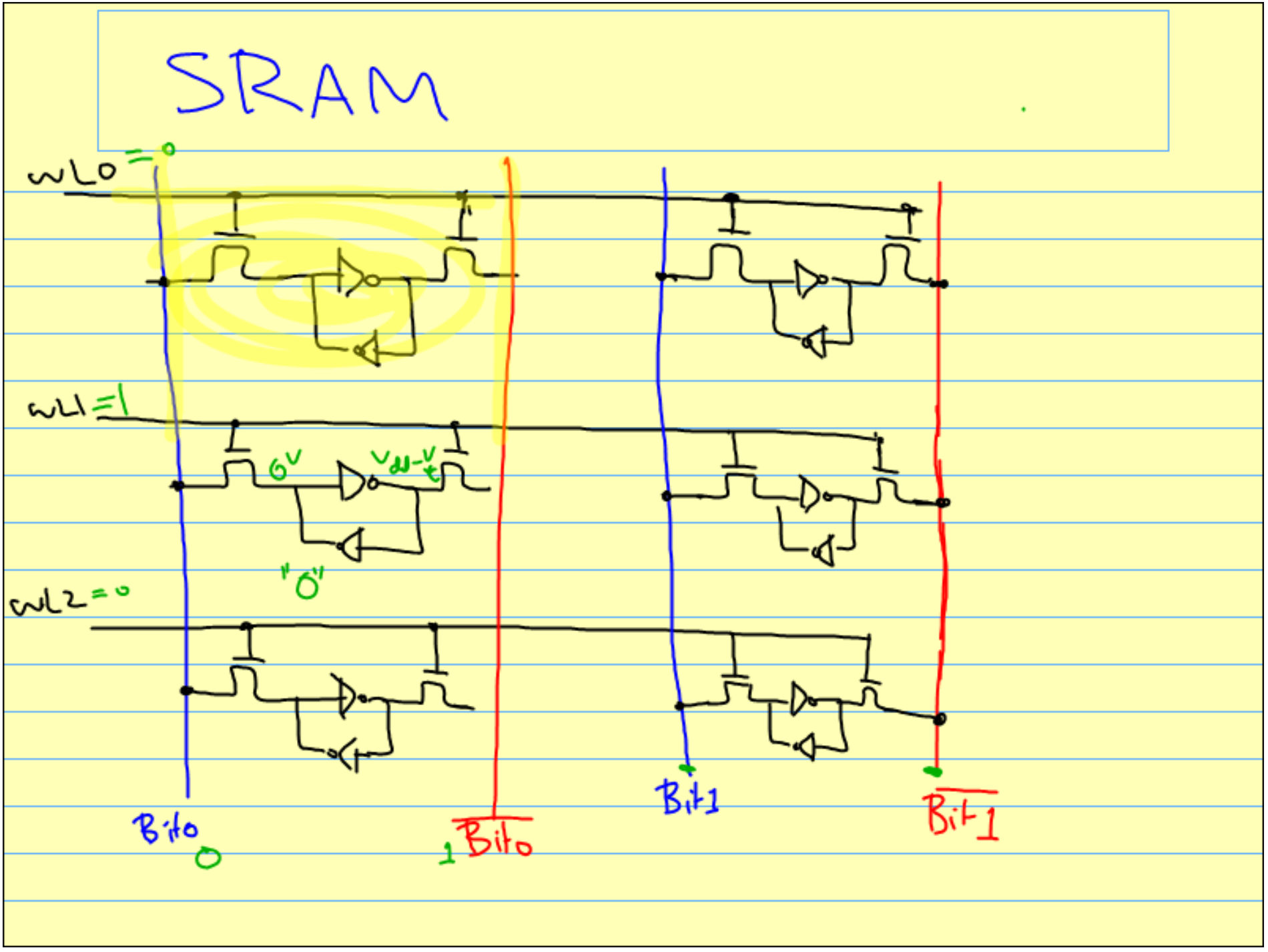
– more load on CLK



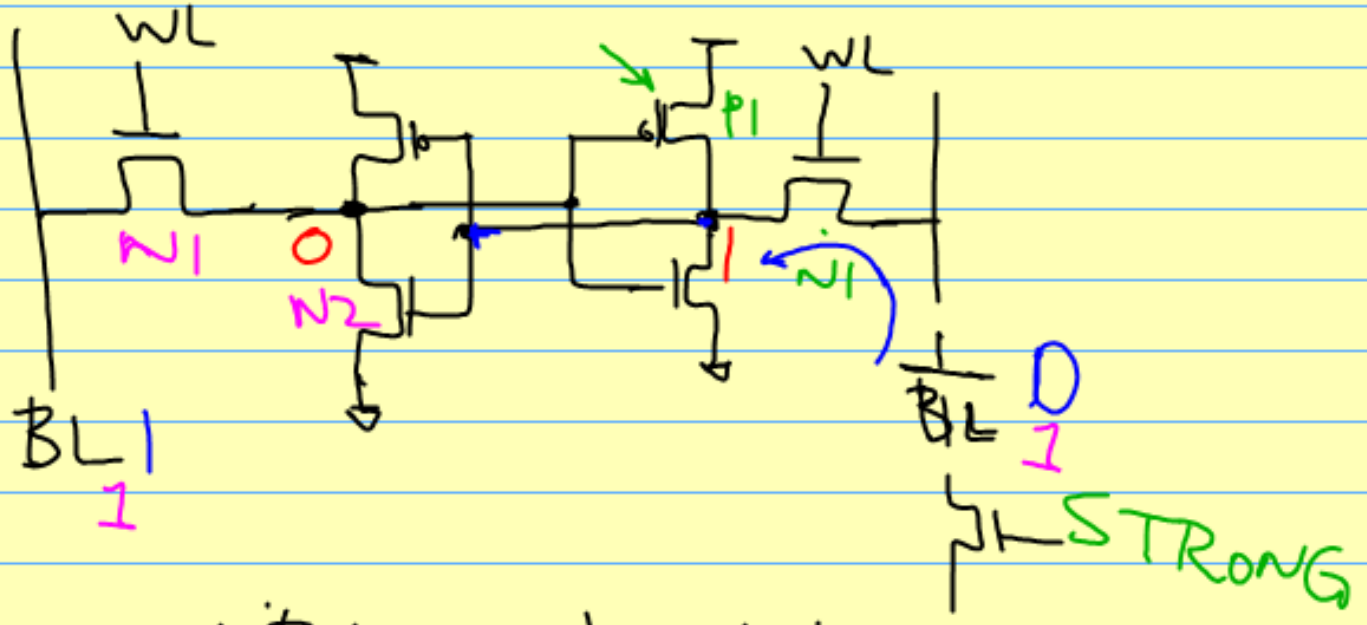


SRAM




SRAM
WL0 = 0
WL1 = 1
0V
$V_{dd}-V_t$
"0"
WL2 = 0
Bit0
0
1
$\overline{Bit_0}$
Bit1
$\overline{Bit_1}$

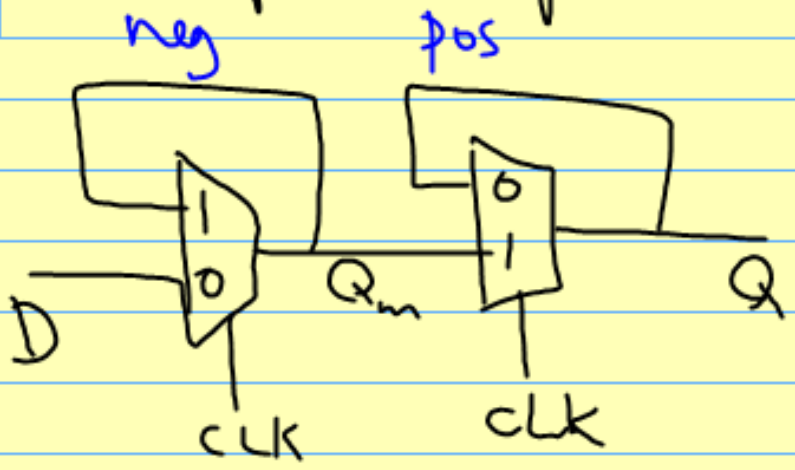
Sizing SRAM cell



Proper write: N1 has to be stronger than P1

proper read: N_2 ~ ~ ~ N_1

Flip-Flops (Edge Triggered)

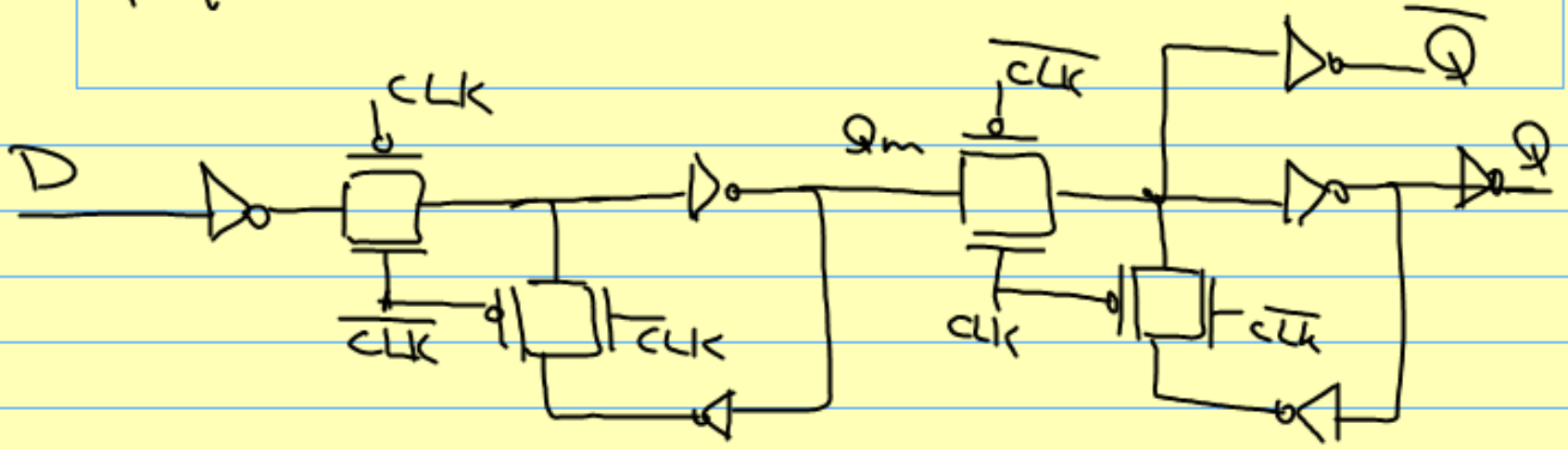


pos pos

CLK $\overline{CLK}$

CLK : 0		D → Qm	Q hold
CLK	↑	DX	Qm hold	Qm → Q
CLK	1	Dx	Q hold	Q follows Qm ⇒ Q hold

FF



Timing Properties