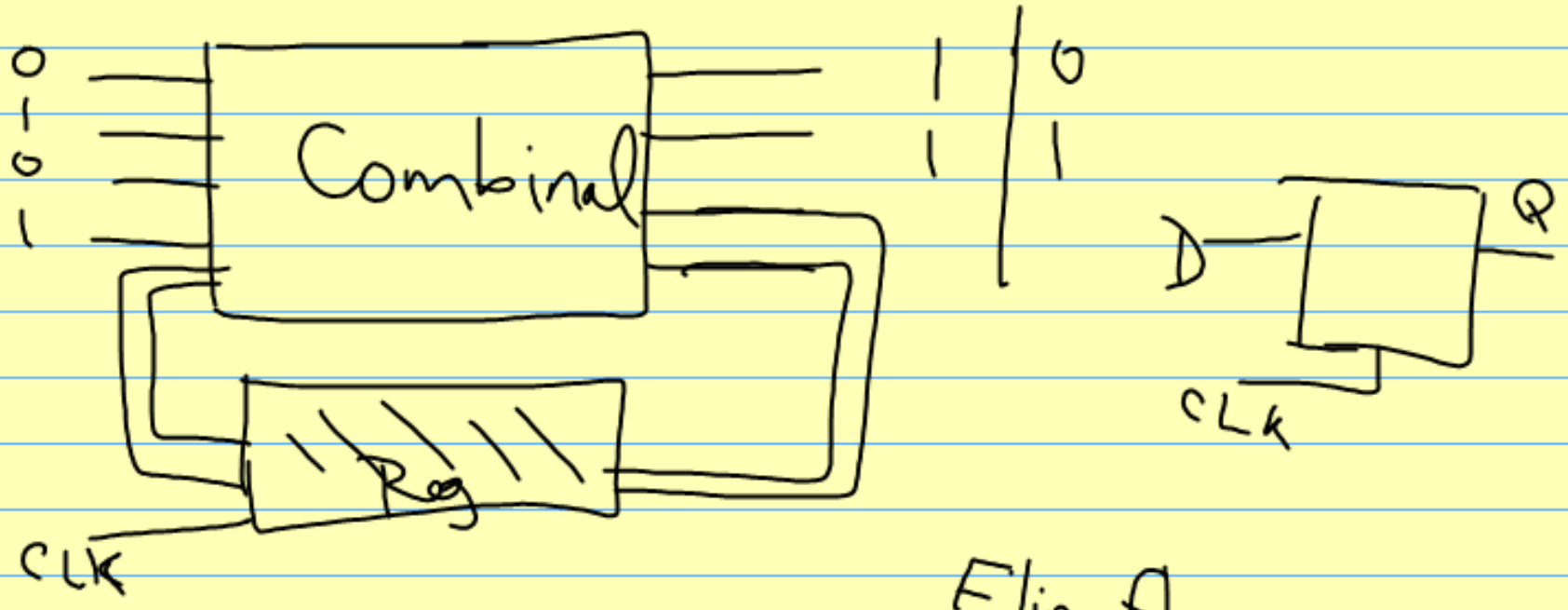
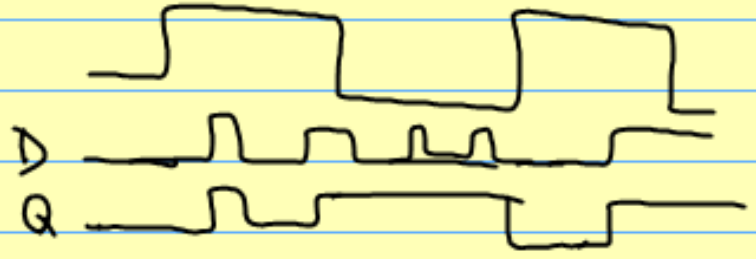
Sequential Logic





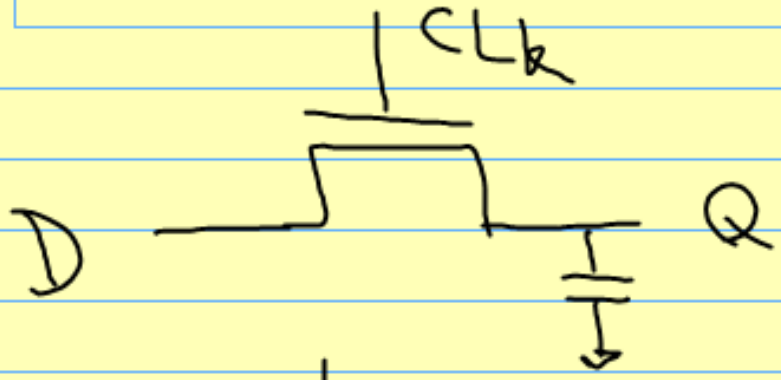
Flip-flop

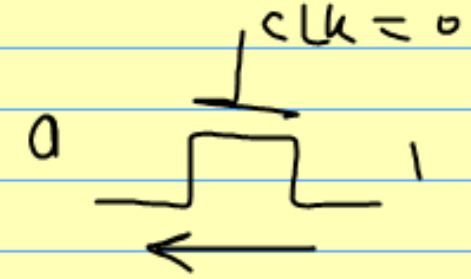
Latch

Reg

clock edge

Memory Cell





\+ simple

\+ area

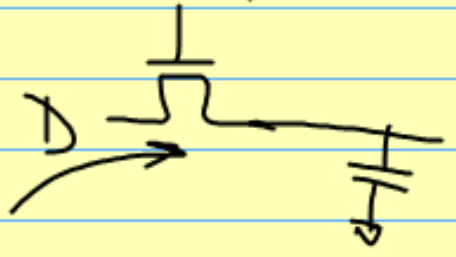
fast?

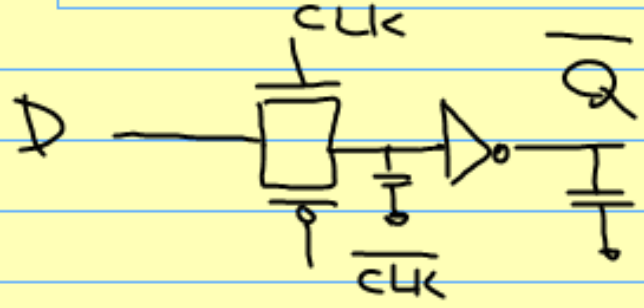
— charge leaks

— Float ⇒ noise

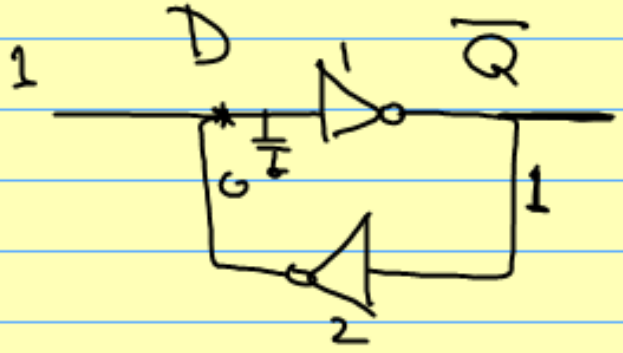
— Diffusion

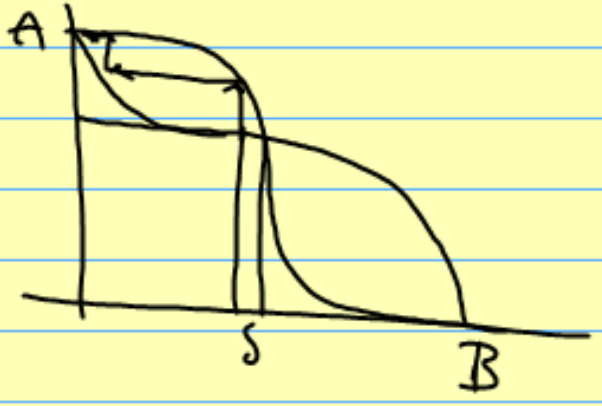
— Vt drop



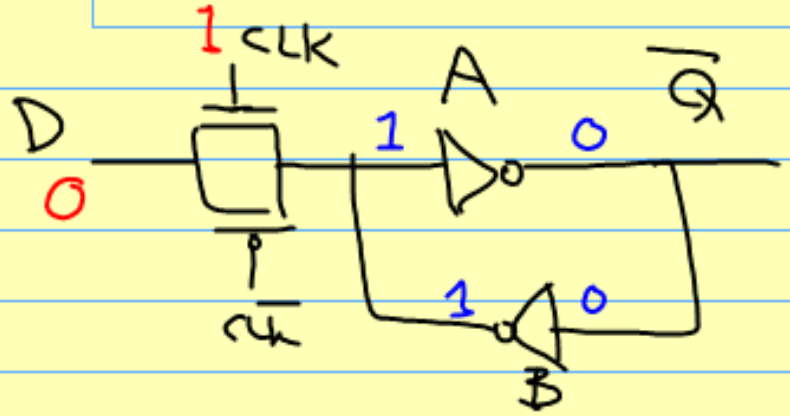


+ Restore weak D
+ Capacitive Coup D
– noise





SRAM cell α-release!



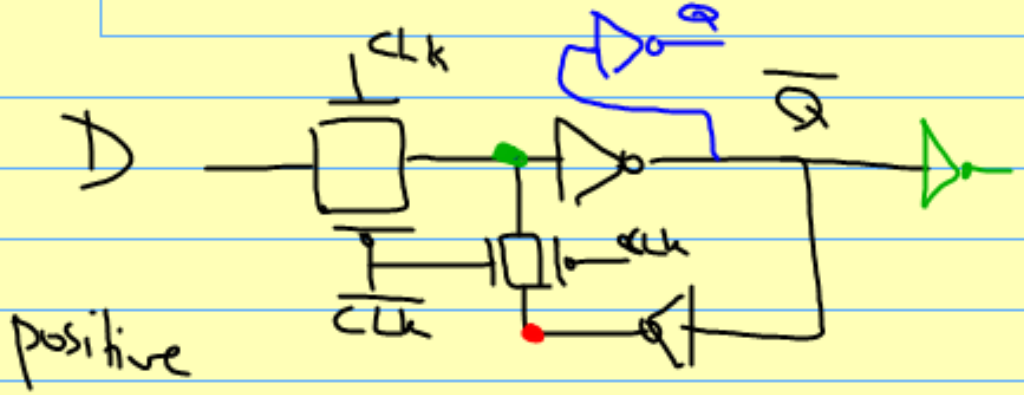
Read: $\overline{Q}$

Write: D ← value

CLK ← 1

- Careful sizing (gate B's pmos, nmos vs D)
  - ⇒ clock period
- Delay
- \+ robust

SRAM Cell (Mux-based Latch)



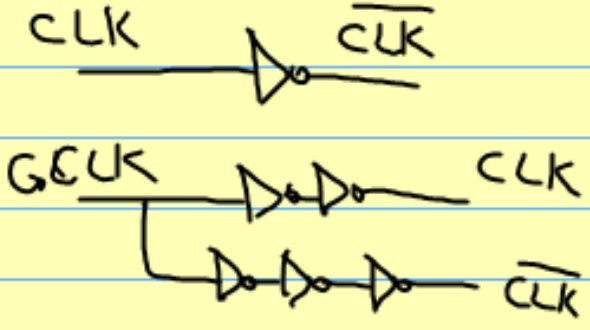
optional path

+ Robust++

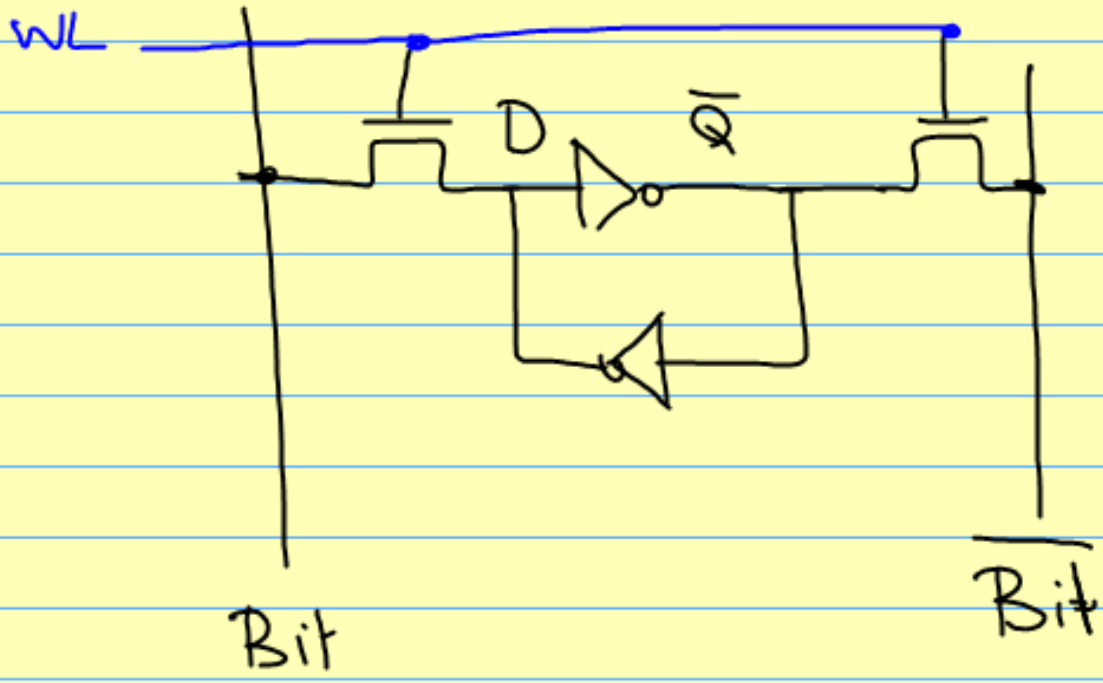
+ popular

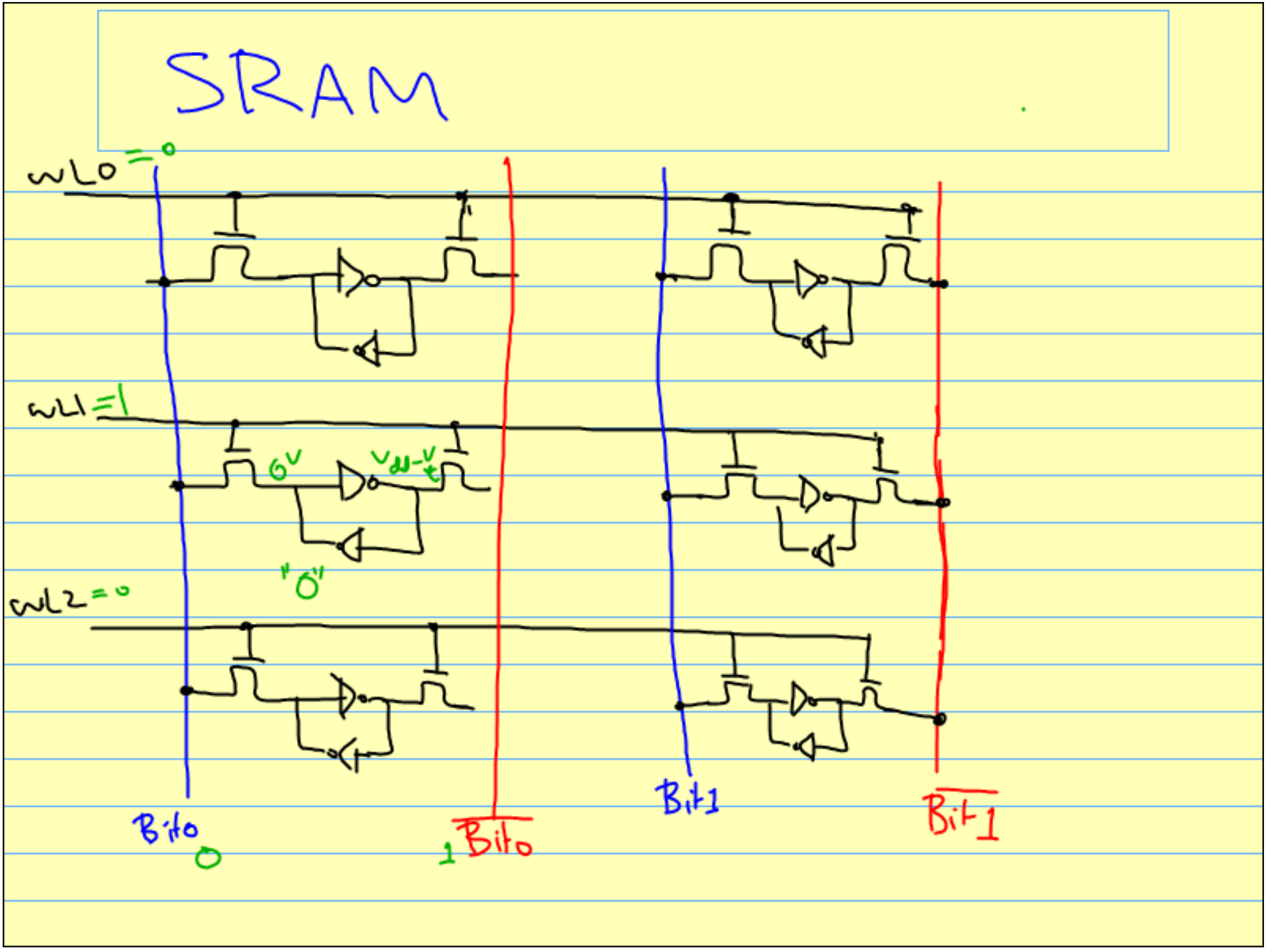
– area

– more load on CLK



SRAM




SRAM
WL0 = 0
WL1 = 1
WL2 = 0
0V
$V_{dd}-V_t$
"0"
Bit0
0
1
$\overline{Bit_0}$
Bit1
$\overline{Bit_1}$