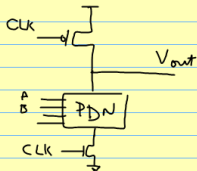
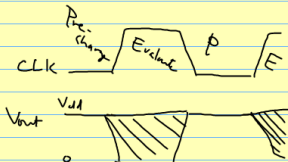


Dynamic Logic



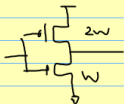
- N+2 devices
- Non-ratioed
- Faster switching *30-40% faster*
- No pass devices
- No short ckt
- $t_{PLH} = 0$



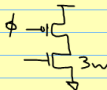
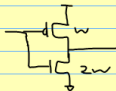
- Large power (Clock) *70%*
- Power large (dynamic)
(even though static $C_{L\downarrow}$)
- ? depend on logic?
- No glitches

Noise Margin (Simplified)

Static CMOS



Shenod logic



Speed

better

better

power

better

robustness

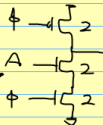
Logical Effort

INV



$$g=1$$

Dynamic (buffer)

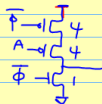


$$g = \frac{2}{3}$$

Dynamic
(no footer)

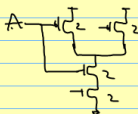
$$g = \frac{1}{3}$$

3x faster

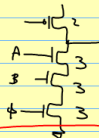


$$g = \frac{4}{3} \quad \times$$

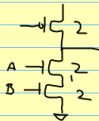
g_{NAND}



$$g = \frac{4}{3}$$

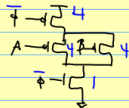


$$g = 1$$

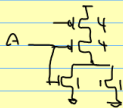


$$g = \frac{2}{3}$$

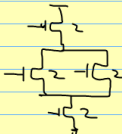
2x Speedup



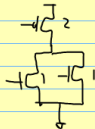
$$g = \frac{4}{3}$$

$$g_{NOR2}$$


$$g = \frac{5}{3}$$

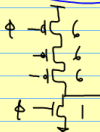


$$g = \frac{2}{3}$$



$$g = \frac{1}{3}$$

5x faster



$$g = 2$$

Signal Integrity

