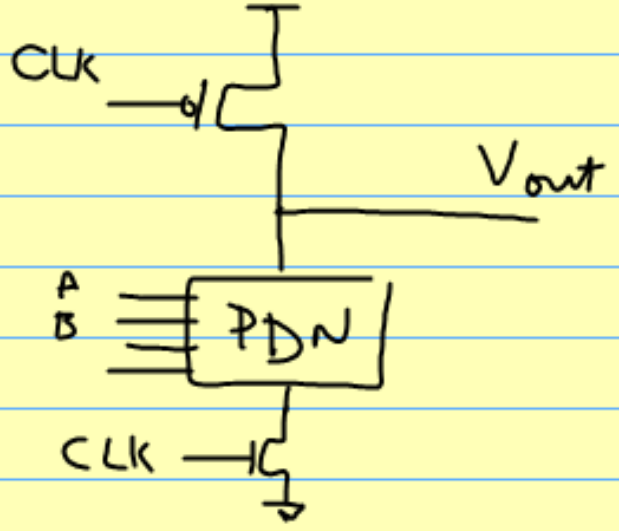
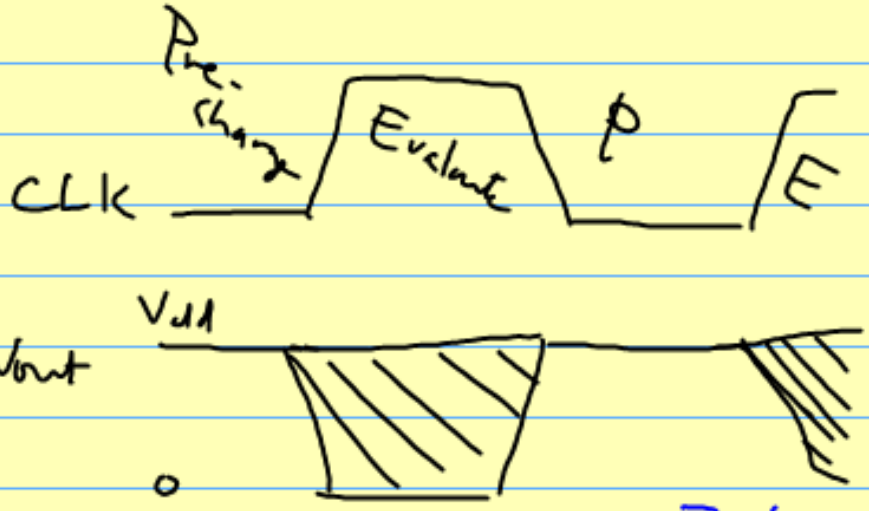
Dynamic Logic

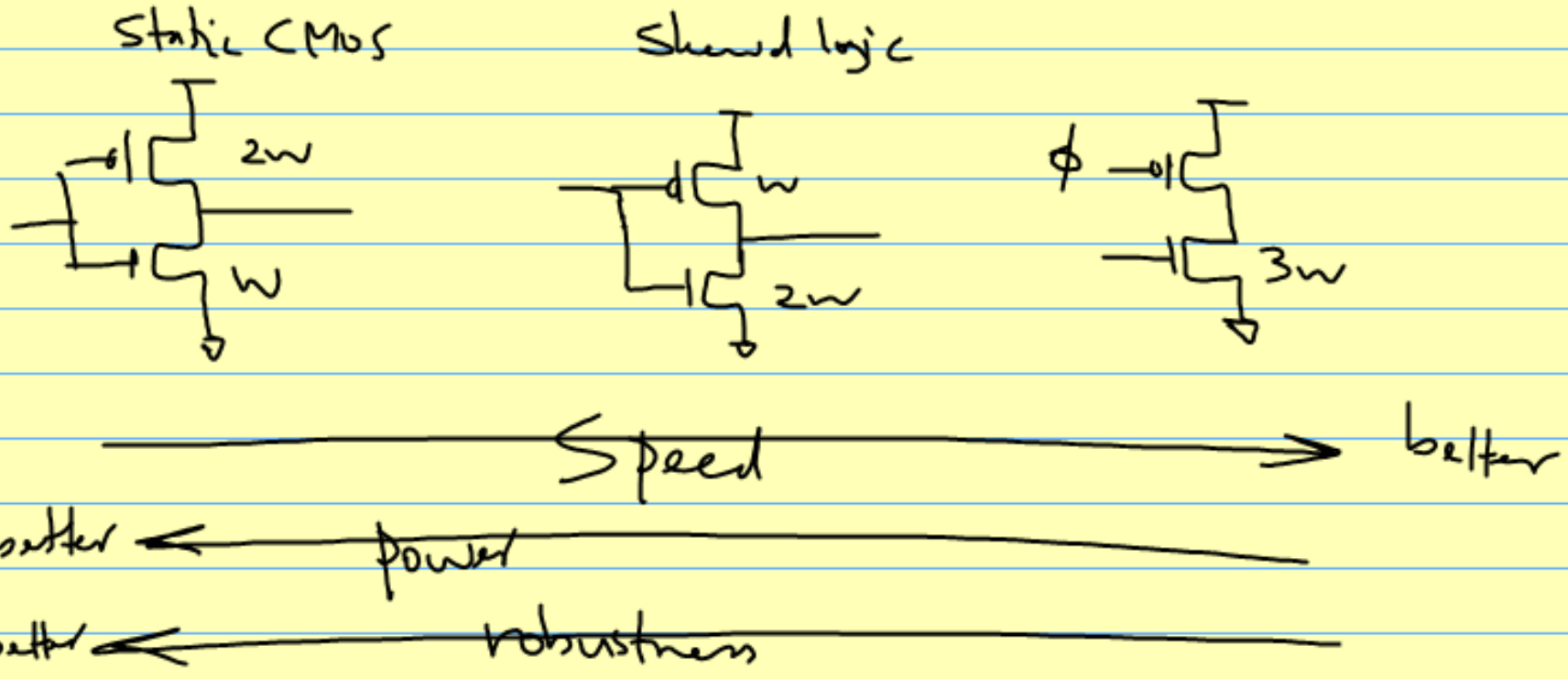




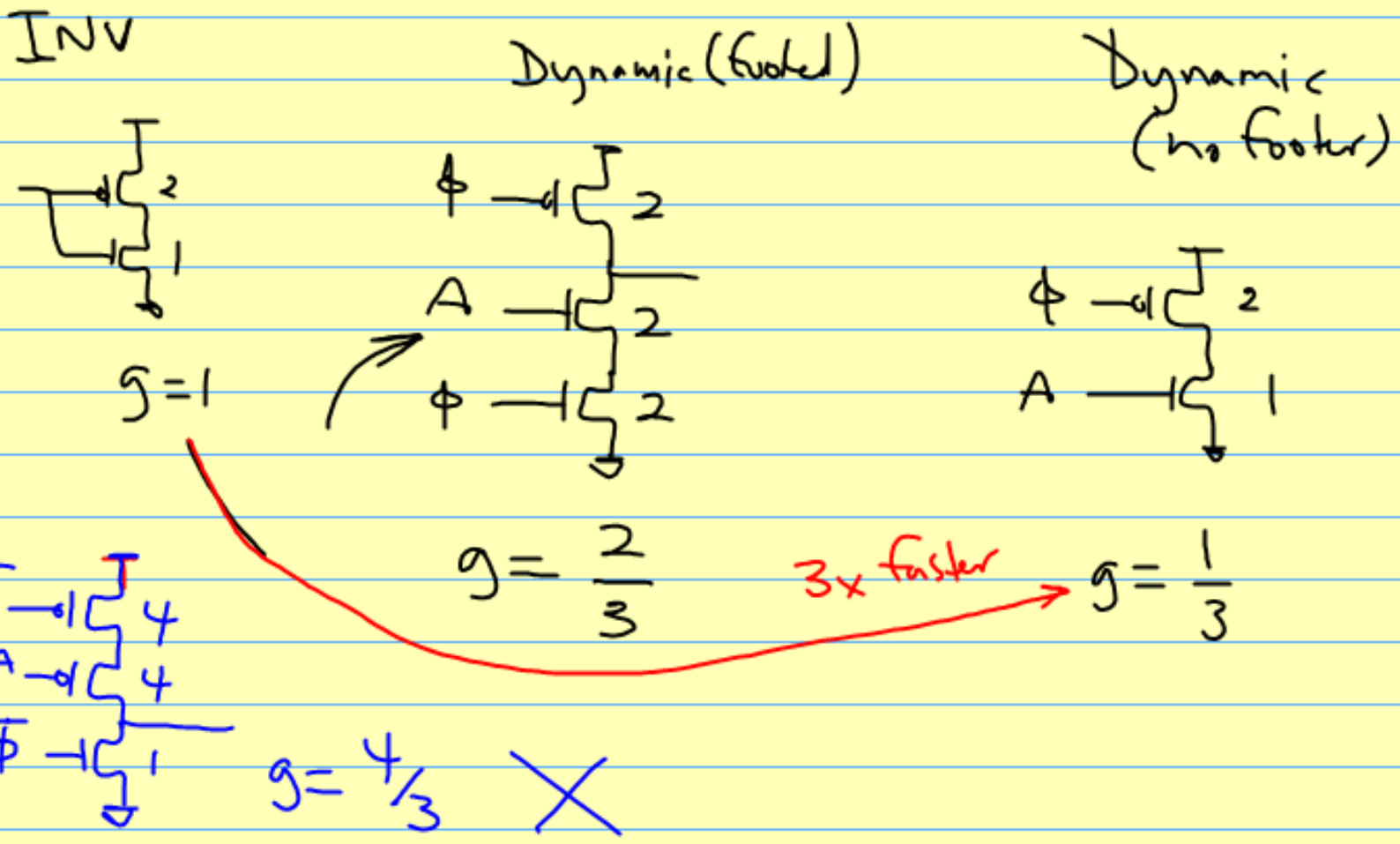
- N+2 devices
- Non-ratioed
- Faster switching 30-40% faster
  - No pmos devices
  - No short ckt
  - $t_{PLH} = 0$

- Large power (Clock) 70%
- power large (dynamic)
  (even though static $C_L \downarrow$)
  ? depend on logic ?
- No glitches

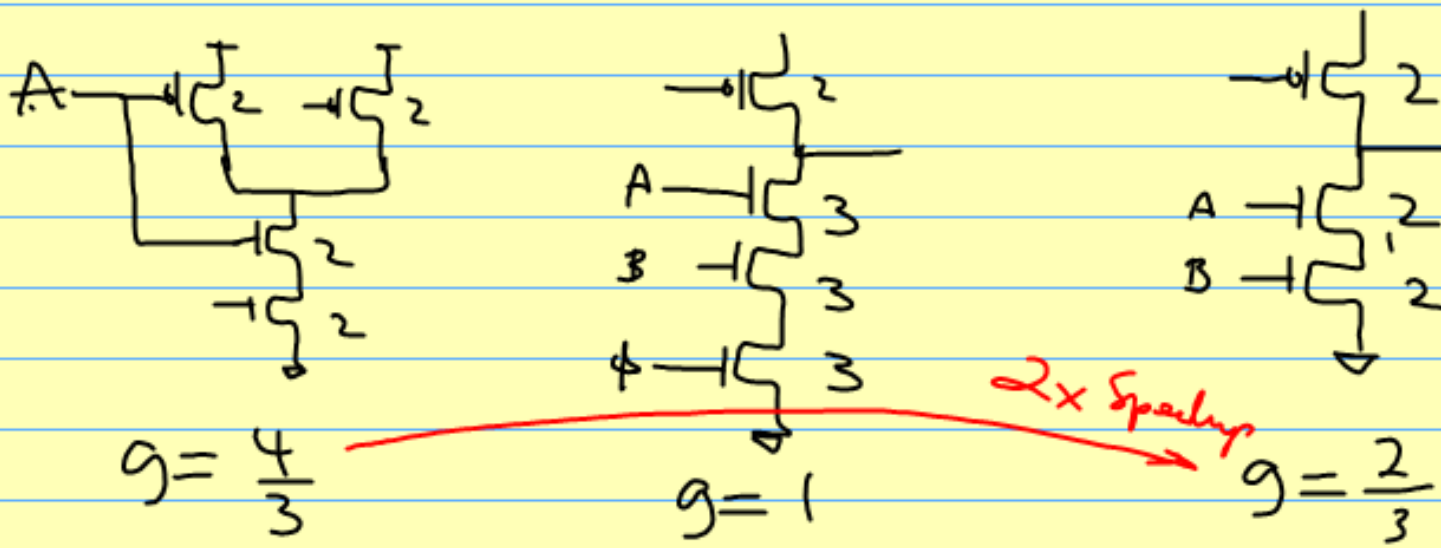
Noise Margin (Simplified)

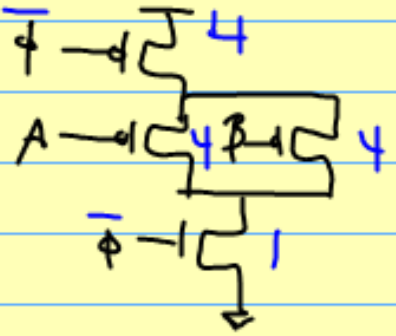


Logical Effort



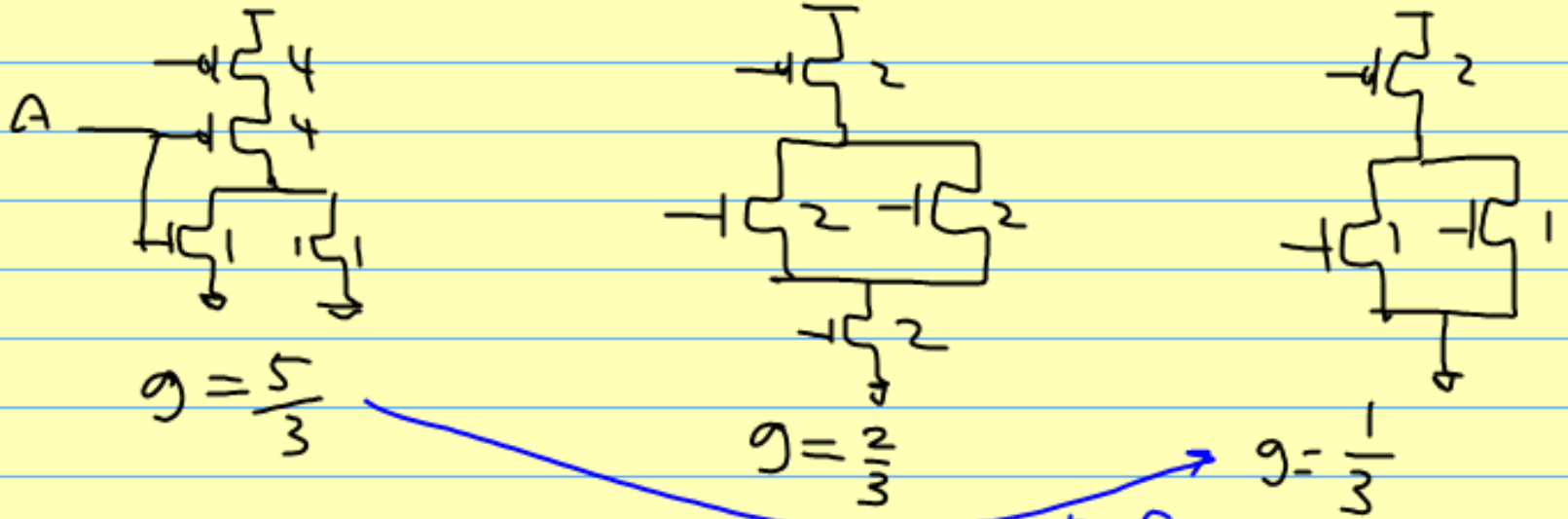
g_{NAND}





$g = \frac{4}{3}$

g_{NOR2}


A
4
4
1
1
$g = \frac{5}{3}$
2
2
2
2
$g = \frac{2}{3}$
2
1
1
$g = \frac{1}{3}$
5x faster
ϕ
6
6
6
ϕ
1
$g = 2$

Signal Integrity