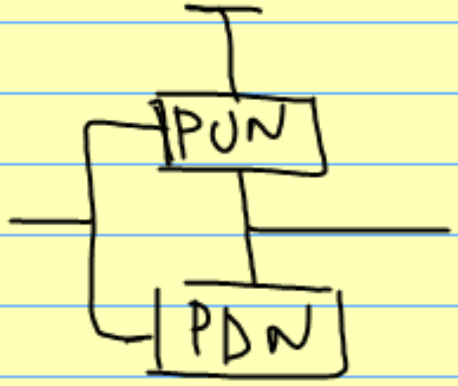
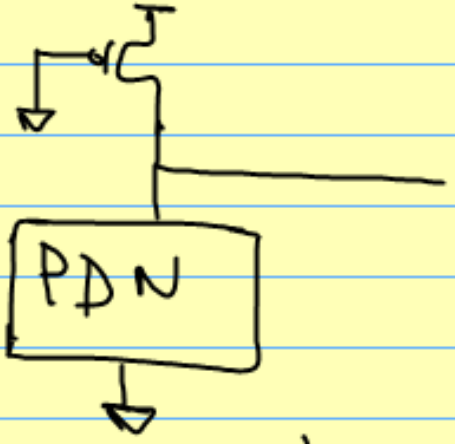
Ratioed Logic (Pseudo_nmos)

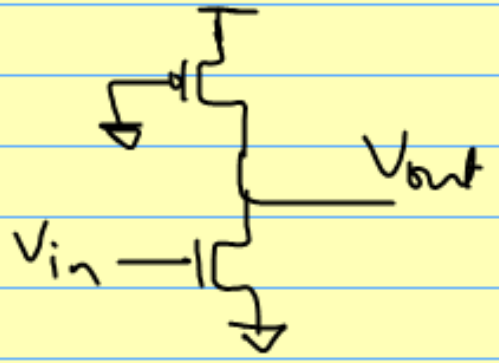
p263



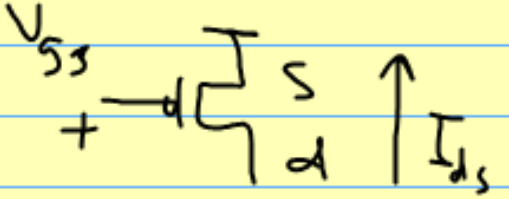


- Robustness X $V_{OL} > 0$
- Static power
+ Reduced # tr
+ Higher performance: cap ↓

Ratioed Logic : sizing W_p



$V_{ol} \sim 0$

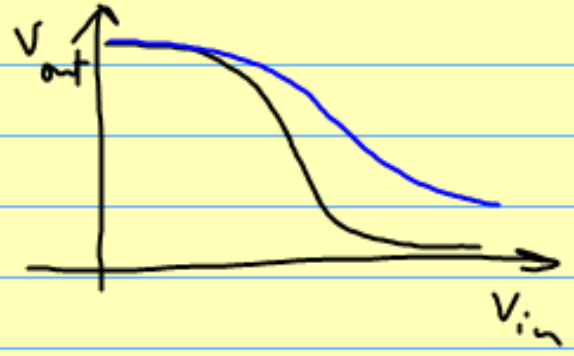


$$k_n\left((V_{dd}-V_{tn})V_{ol}-\frac{1}{2}V_{ol}^2\right)$$

$$=-k_p\left((-V_{dd}-V_{tp})V_{dsatp}-\frac{1}{2}V_{dsatp}^2\right)$$

$$V_{ol} \simeq -\frac{k_p}{k_n}\frac{(-V_{dd}-V_{tp})V_{dsat}}{V_{dd}-V_{tn}}$$

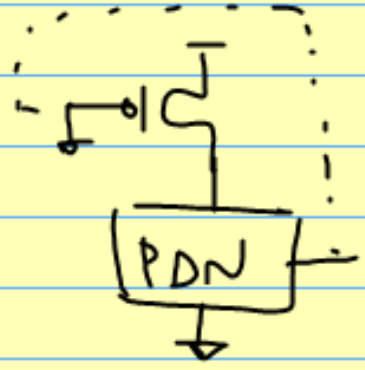
$$V_{ol} \propto -\frac{k_p}{k_n} = \left|\frac{\mu_p W_p}{\mu_n W_n}\right|$$



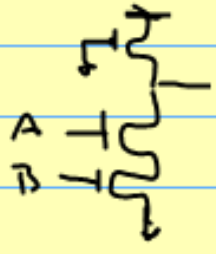
Ratioed Logic: Static Pwr

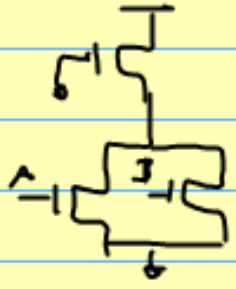
$$P_{static} = V_{dd} \cdot I \Big|_{V_{out}=V_{0l}}$$

$$= V_{dd} \cdot \left| k_p \left(-V_{dd} - V_t\right) V_{dsat_p} - \frac{1}{2} V_{dsat_p}^2 \right|$$

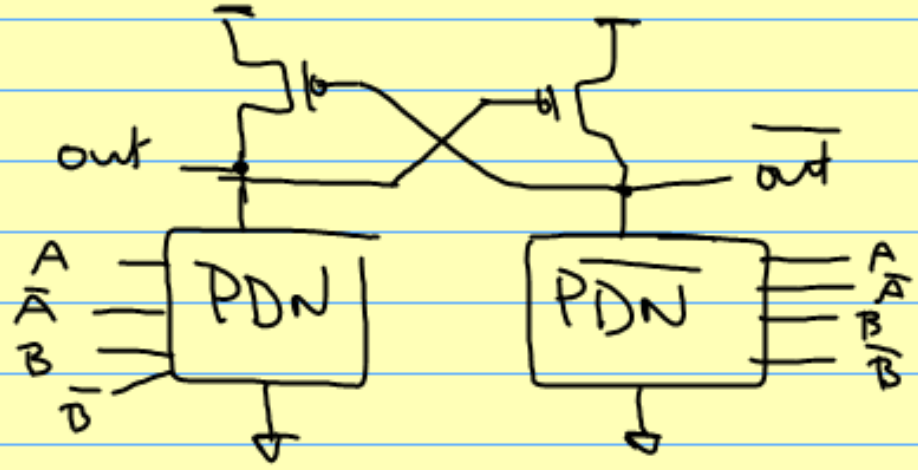


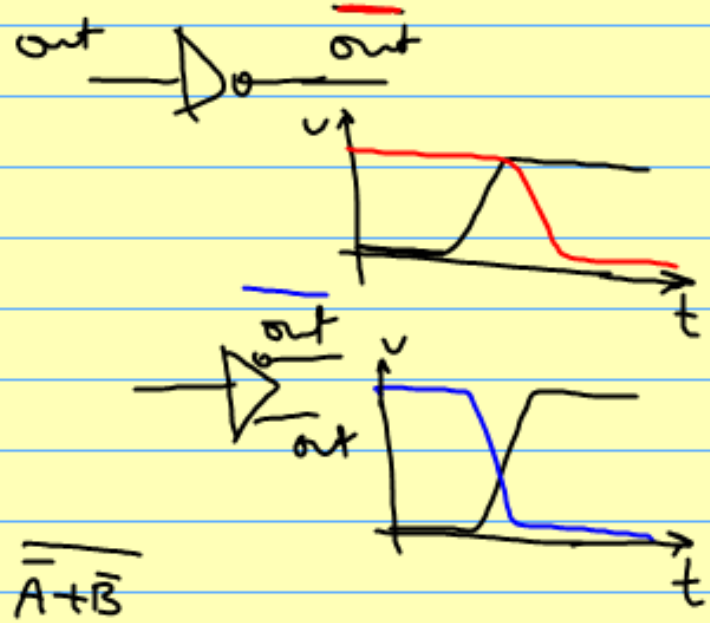
	area	delay/noise
NOR	✓	✓
NAND		



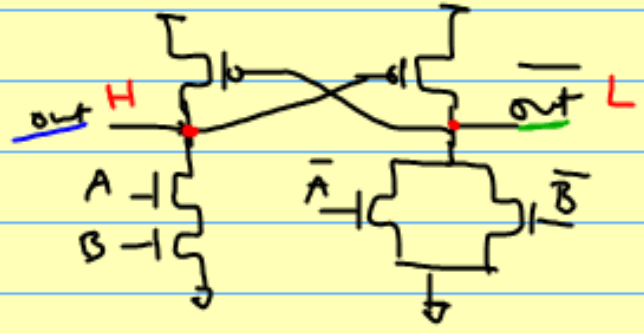


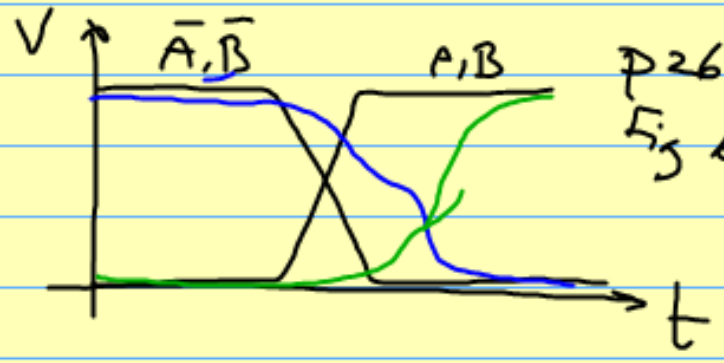
DCVSL : Differential Cascade Voltage Switch Logic





$out = \overline{A \cdot B}$ $\quad \overline{out} = \overline{A \cdot B} = \bar{A} + \bar{B}$





p268
Fig 6-31

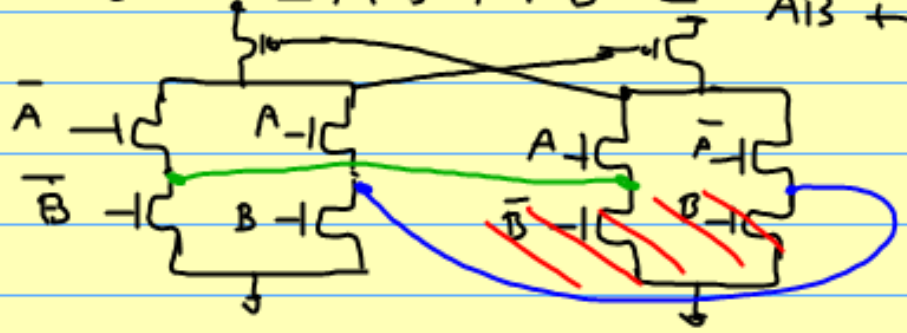
DCVSL

+ Reduces # tr
+ Rail-to-Rail voltage swing
+ No Static pwr
+ differential logic
+ share tr

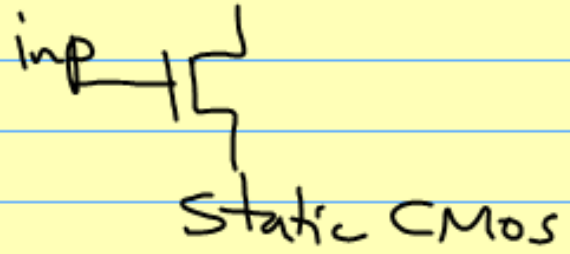
− still ratioed
− Design Complexity

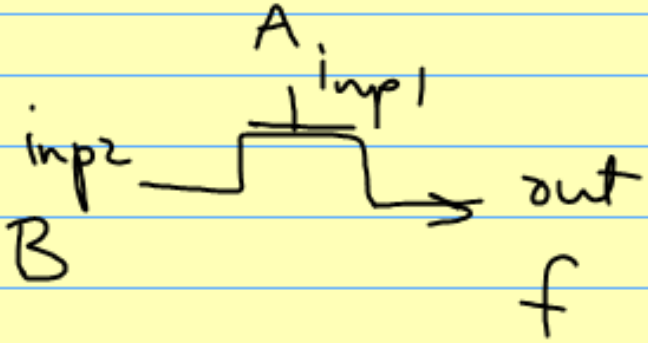
$$out = A\bar{B} + \bar{A}B = \overline{\bar{A}\cdot\bar{B} + AB}$$

$$\overline{out} = \bar{A}\bar{B} + AB = \overline{A\bar{B} + \bar{A}B}$$

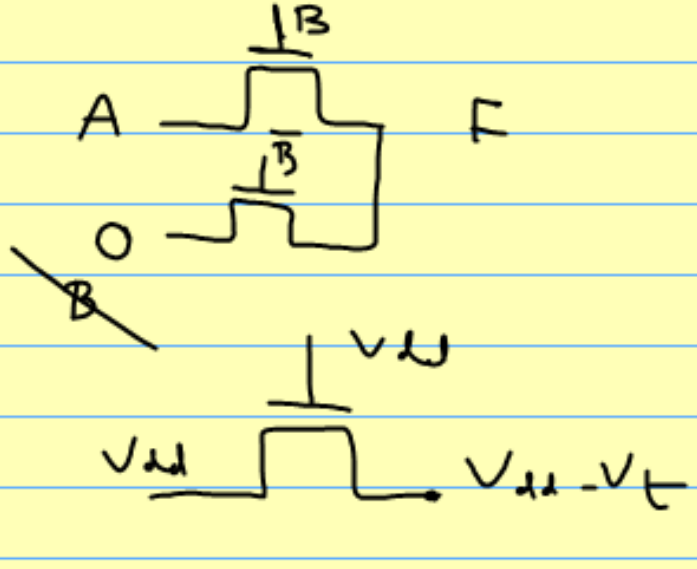


Pass Transistor Logic



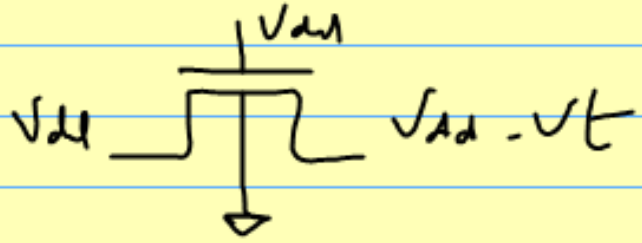


$F = A \cdot B$



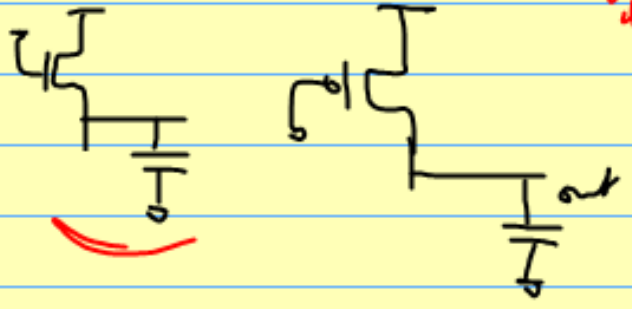
+ Reduce # tr
+ No pmos
+ No static pwr
− Voltage swing
noise margin
− input imp
− delay

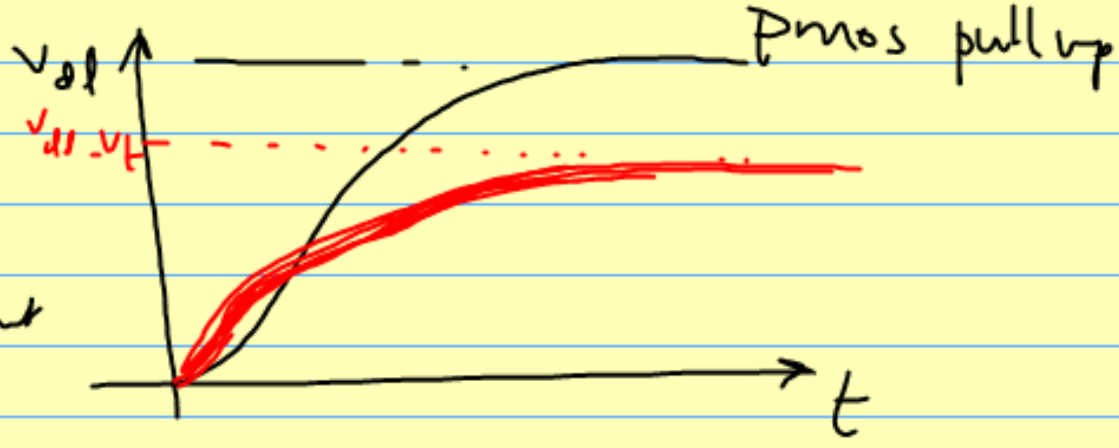
PTL Body Effect



$$V_t = V_{t_0} + \gamma\left(\sqrt{2\gamma_B + (V_{dd} - V_t)} - \sqrt{2\gamma_B}\right)$$

$$V_t > V_{t_0}$$

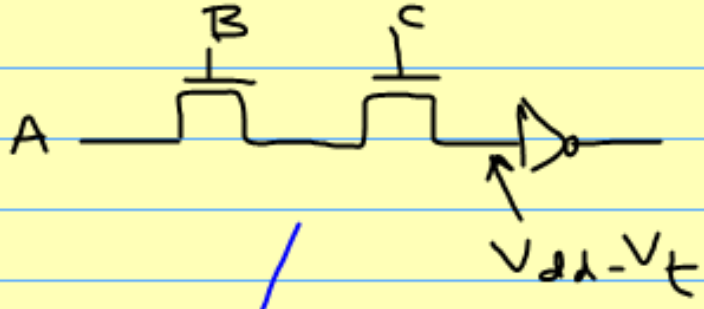


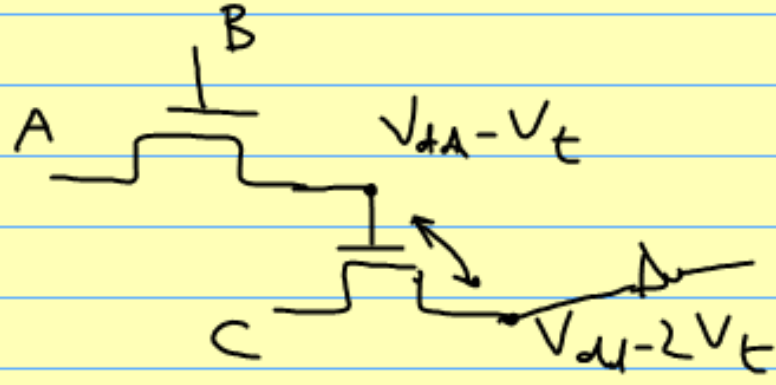


slow: V_t

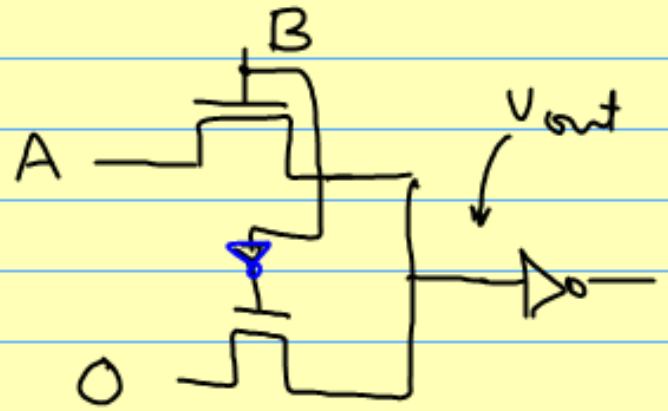
Cascade Pass tr

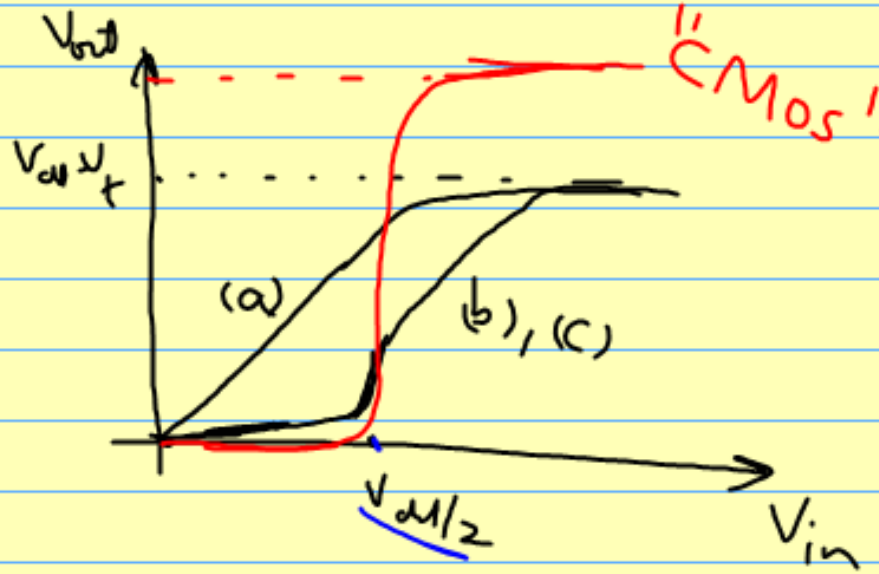
$F = A \cdot B \cdot C$





DC characteristics PTL



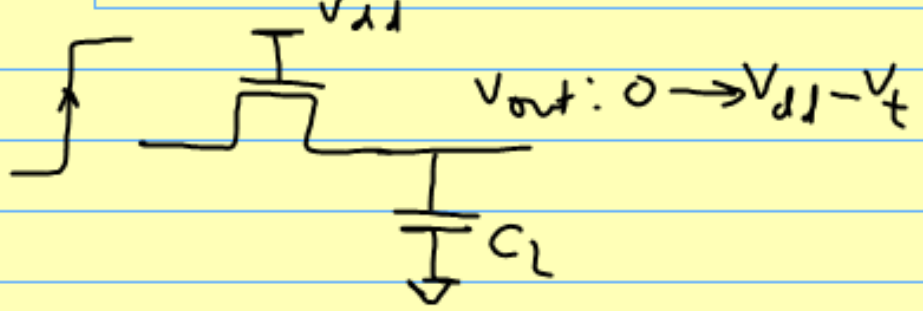


(a) B=1, A: 0 → 1

(b) A=1, B: 0 → 1

(c) A, B : 0 → 1

Power PTL

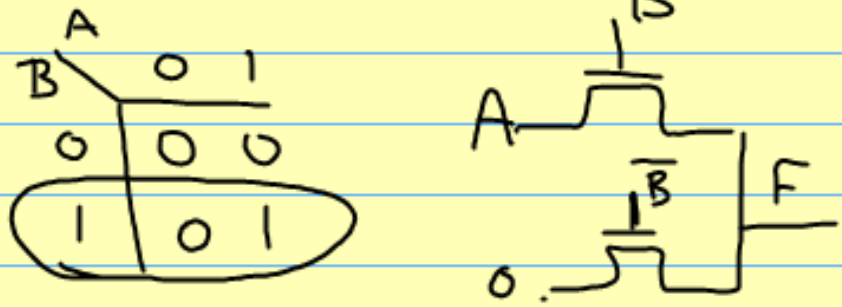


$$E_{0\rightarrow 1} = \int i(t)\, V_{dd}\, dt = \int_{t:0}^{\infty} C_L \frac{dV}{dt} V_{dd}\, dt = \int_0^{V_{dd}-V_t}$$

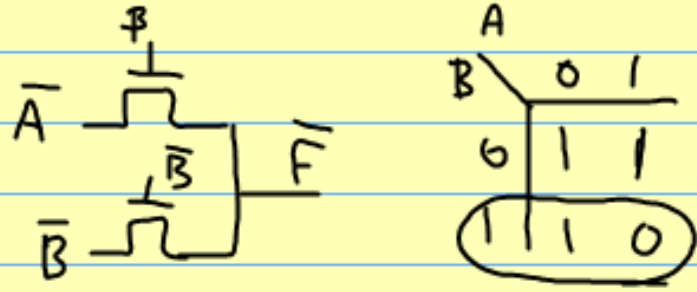
$$= C_L V_{dd} \underbrace{(V_{dd} - V_t)}_{\text{Swing}}$$

Differential PTL

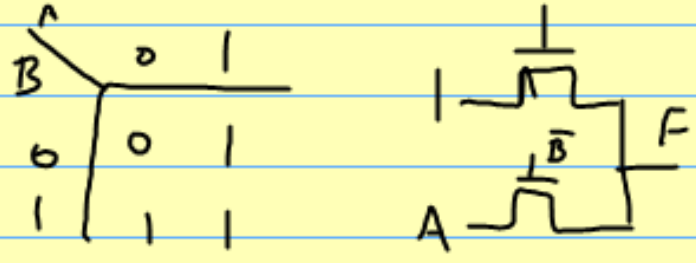
$F = A \cdot B$



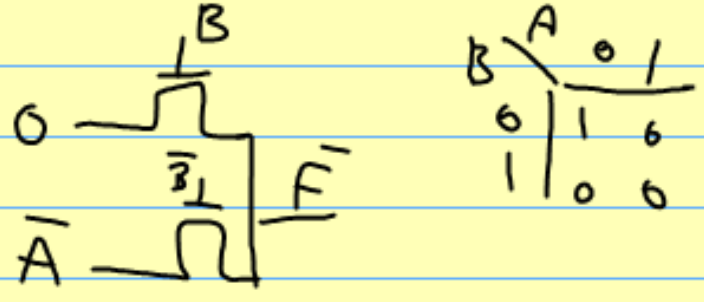
$\overline{F} = \overline{A \cdot B}$



$F = A + B$

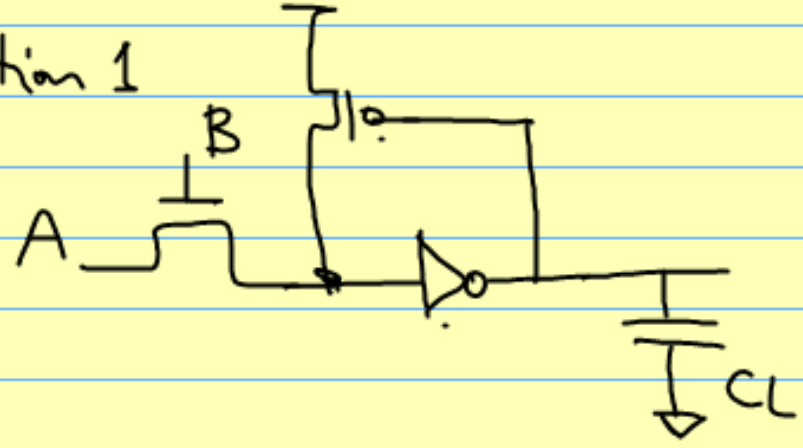


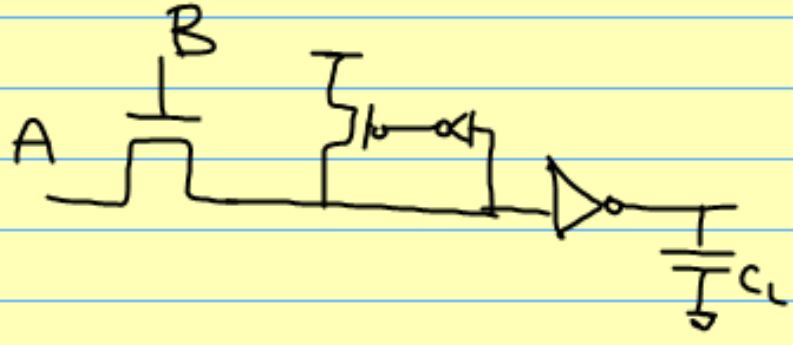
$\overline{F} = \overline{A + B}$



Robust & Efficient PTL

Solution 1

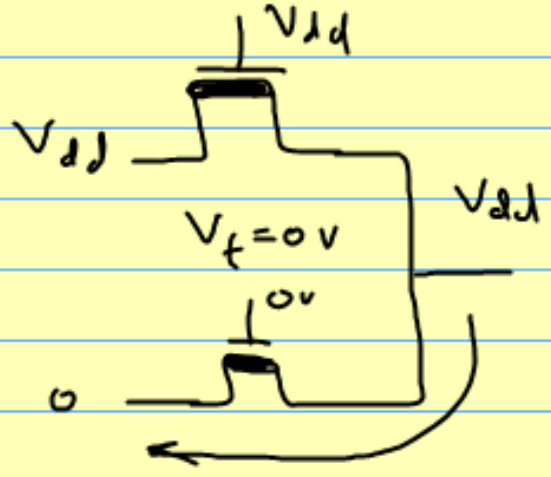


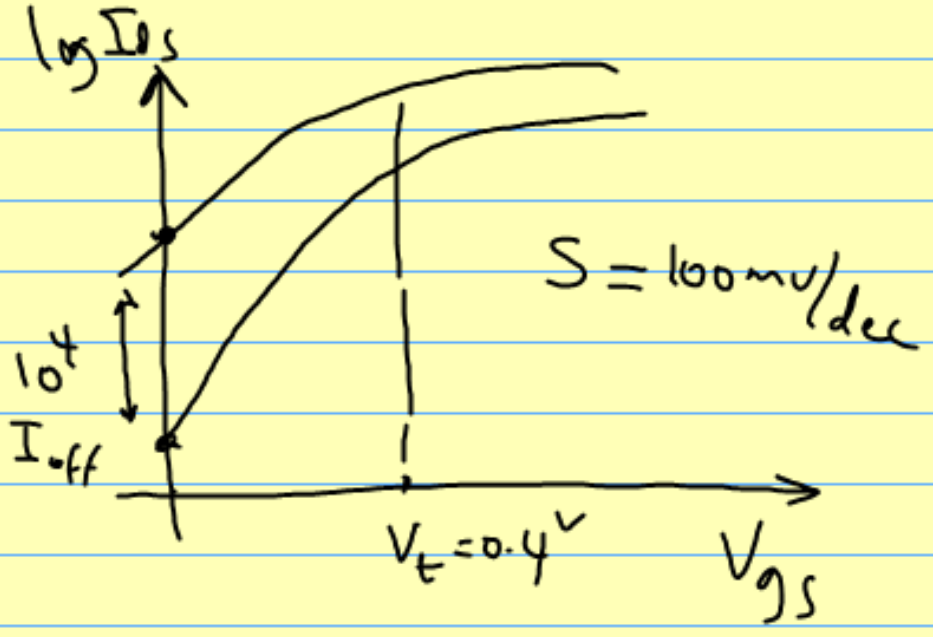


isolate large load

Better PTL

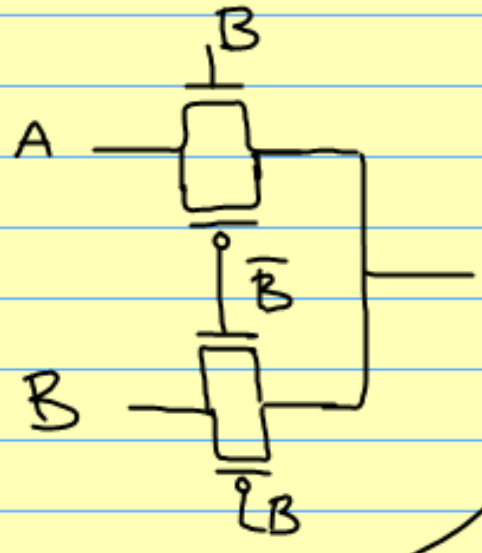
Solution 2





Better PTL

Solution 3: Transmission gates

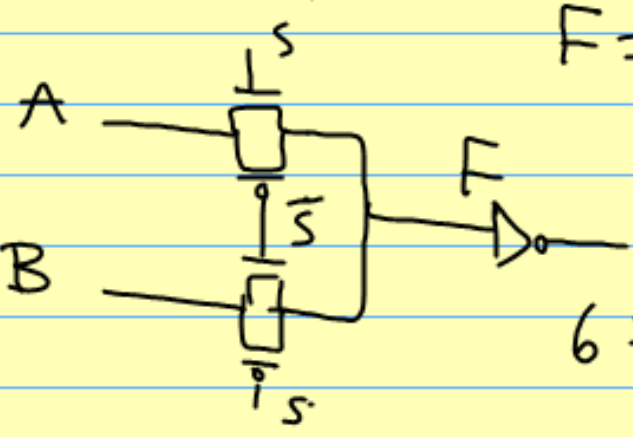


good for MUX

XOR

Multiplexer

$F = AS + B\bar{S}$

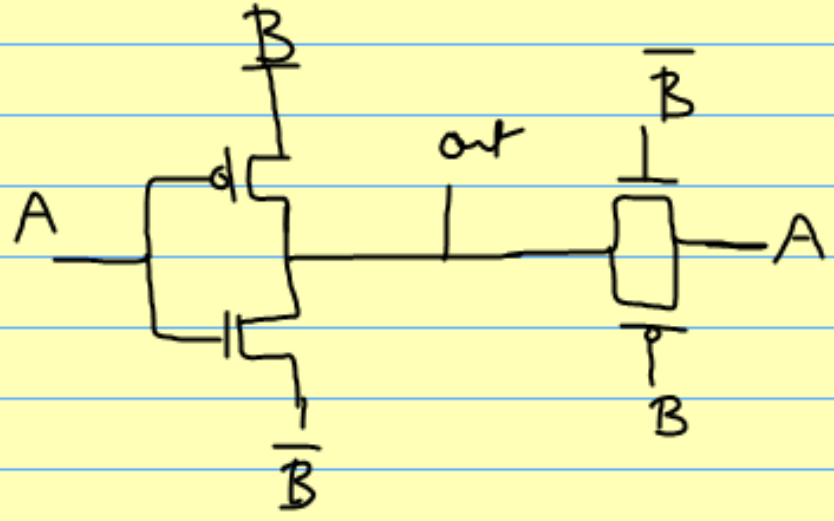


CMOS

8

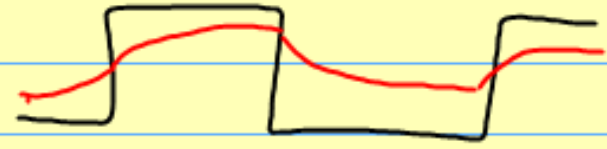
6 tr

XOR in PTL



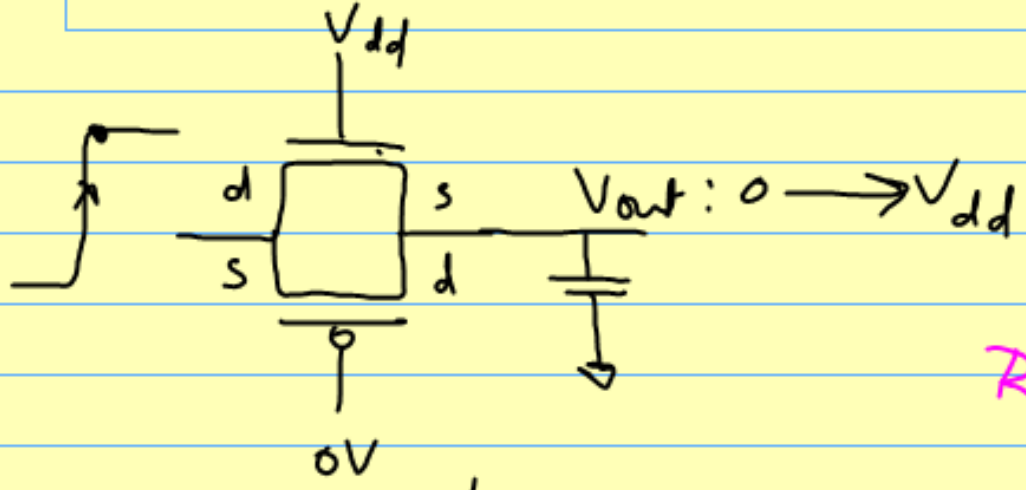
B = 1 out = $\bar{A}$

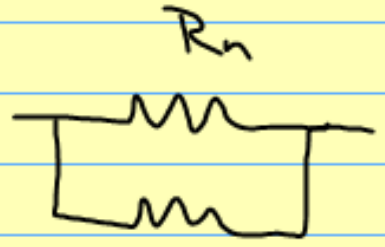
B = 0 A' A



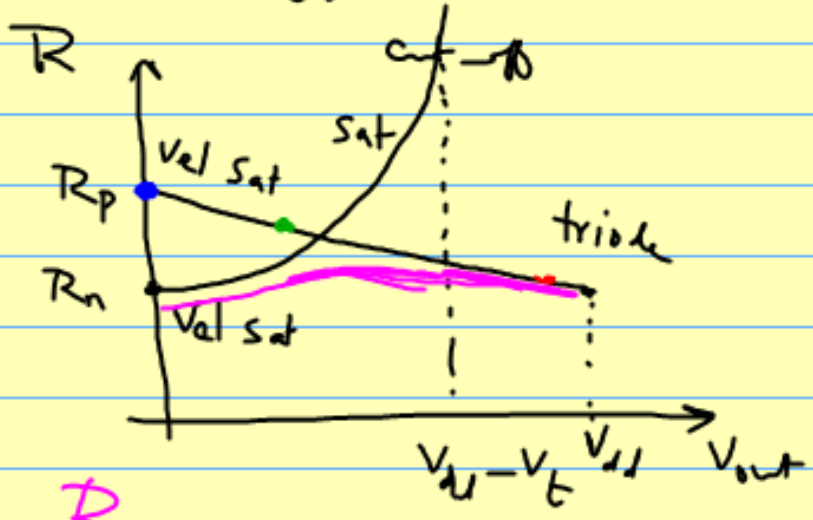
$B\bar{A} + \bar{B}A$

Performance Transmission Gate

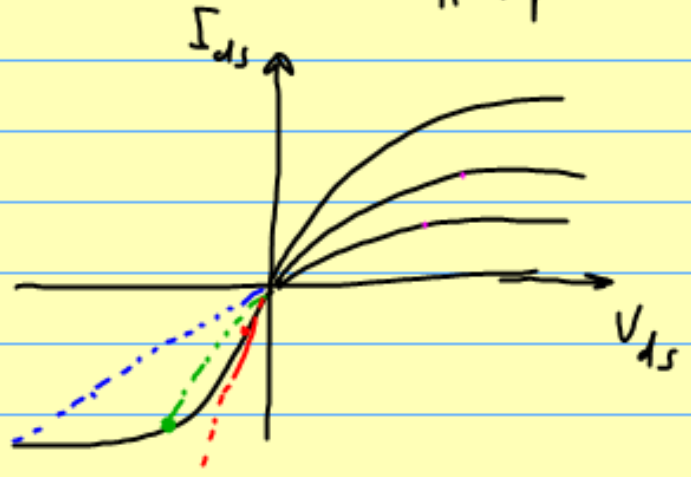


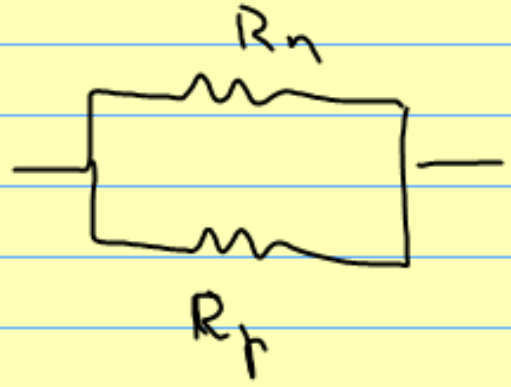


$R_{eq} = R = R_n \parallel R_p$



R_{eq}





NMOS 2R 2R

Pmos 2R → R

$R_n \| R_p = R$

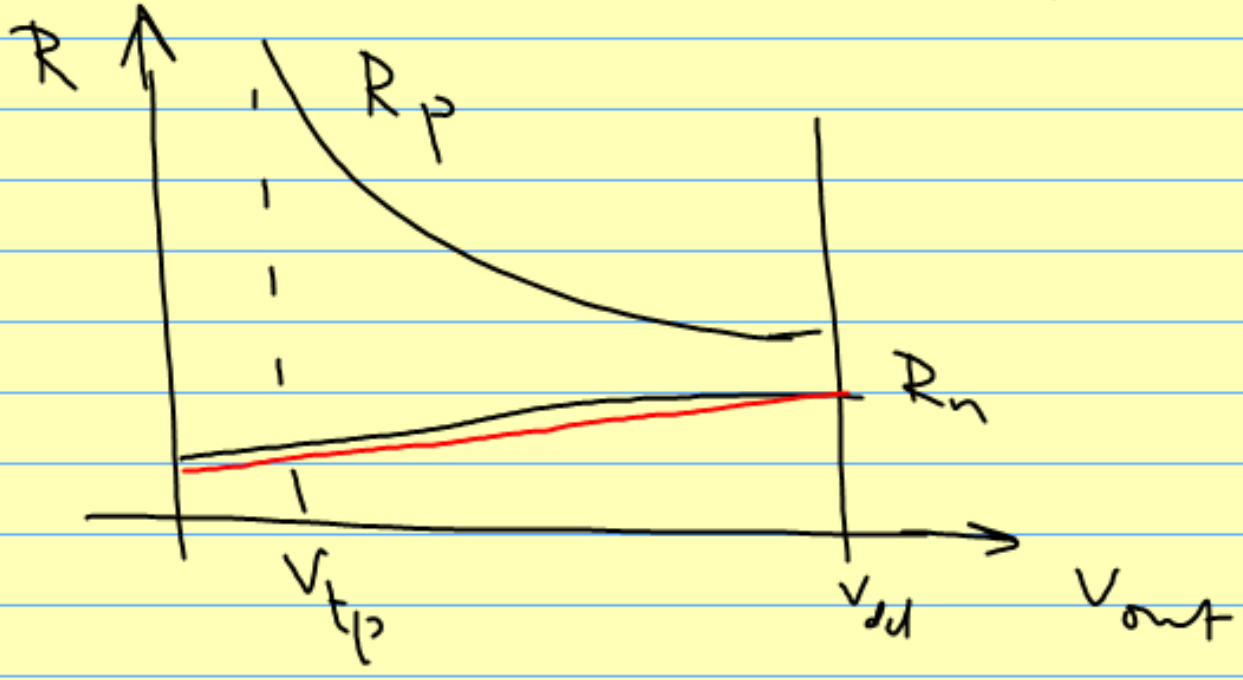
$2R \| R \quad \frac{2}{3}R$

$\frac{1}{\frac{1}{2R} + \frac{1}{R}}$

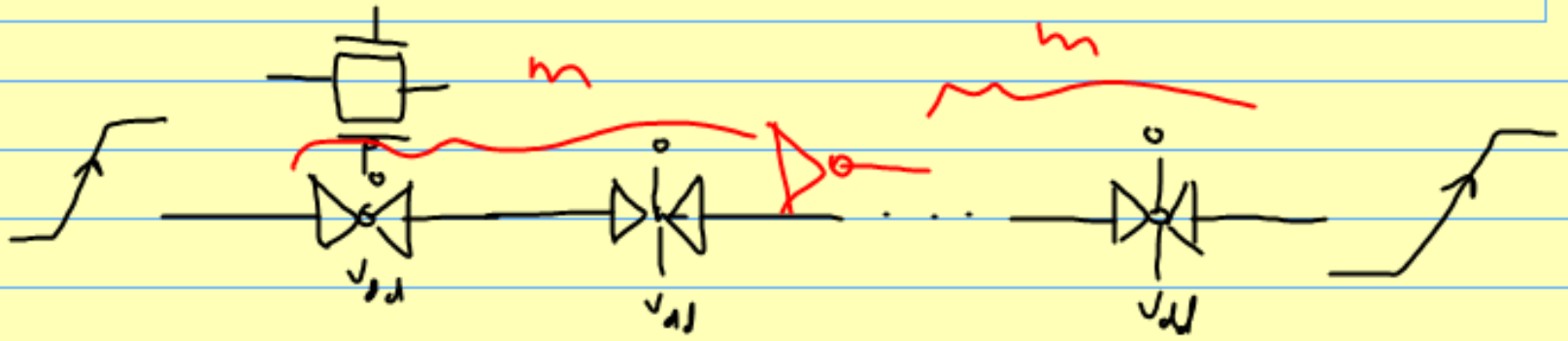
$C_g \uparrow \frac{3}{2}$

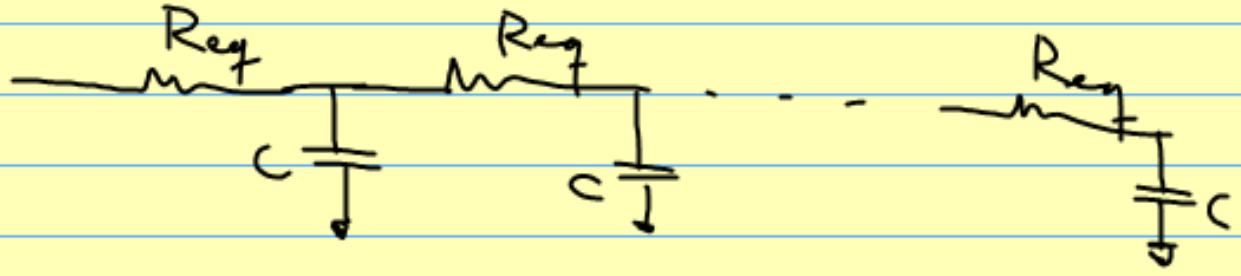
3rd. imp in R

Transmission Gate Req

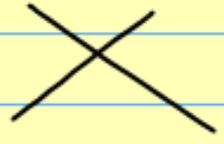


Chain of Xmission Gates





$$t_p = 0.69\ C\left(R_{eq} + 2R_{eq} + \cdots nR_{eq}\right) = 0.69\,R_{eq}C\frac{n(n+1)}{2}$$



Chain Xmsn Gate w/ Buffers

$$t_p = 0.69 R_{eq} C \left(\frac{m(m+1)}{2} \times \frac{n}{m} + t_{buf} \left(\frac{n}{m} - 1 \right) \right)$$

linear in terms of n

- $\frac{m(m+1)}{2}$: chain of m xmissim gates
- $\frac{n}{m}$: how many chains
- $t_{buf}\left(\frac{n}{m} - 1\right)$: assume not dep m

$$\frac{\partial t_p}{\partial m} = 0.69 R_{eq} C \frac{n}{2} - t_{pbuf} \frac{n}{m^2} = 0$$

$$m_{opt} = \sqrt{\frac{2 t_{buf}}{0.69 R_{eq} C}} \simeq 3-4$$