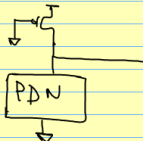
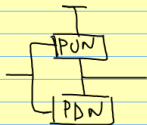
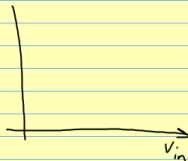


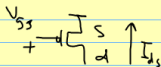
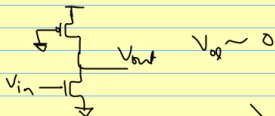
Ratioed Logic (Pseudo-nmos) ^{#263}



- Robustness $\times V_{OL} > 0$
- Static power
- + Reduced # tr
- + Higher performance: $c_{eq} \downarrow$



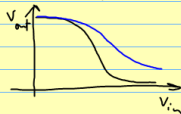
Ratiosed Logic: sizing W_p



$$k_n ((V_{DD} - V_{tn}) V_{ol} - \frac{1}{2} V_{ol}^2)$$

$$= -k_p ((-V_{DD} - V_{tp}) V_{dsatp} - \frac{1}{2} V_{dsatp}^2)$$

$$V_{ol} \approx \frac{-k_p}{k_n} \frac{(-V_{DD} - V_{tp}) V_{dsatp}}{V_{DD} - V_{tn}}$$

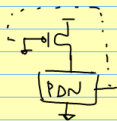


$$V_{ol} \propto \frac{-k_p}{k_n} = \left| \frac{\mu_p W_p}{\mu_n W_n} \right|$$

Ratioed Logic: Static Pwr

$$P_{\text{static}} = V_{dd} \cdot I \Big|_{V_{out} = V_{ol}}$$

$$= V_{dd} \cdot \left| k_p (-V_{dd} - V_{tp}) V_{dsatp} - \frac{1}{2} V_{dsatp}^2 \right|$$



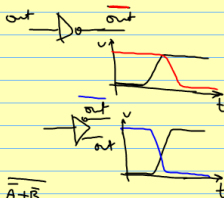
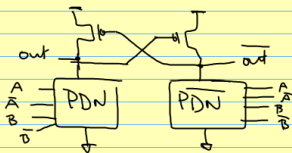
NOR

area
✓delay/noise
✓

NAND

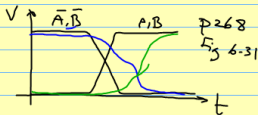
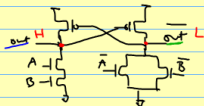


DCVSL: Differential Cascade Voltage Switch Logic



$$\text{out} = \overline{A \cdot B}$$

$$\overline{\text{out}} = \overline{\overline{A \cdot B}} = \overline{A + B}$$



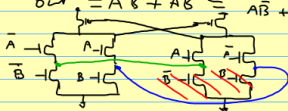
DCVSL

- + Reduces # tr
- + Rail-to-Rail voltage swing
- + No static pwr
- + differential logic
- + share tr

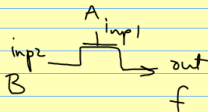
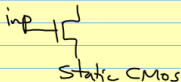
- still ratioed
- Design complexity

$$\text{out} = A\bar{B} + \bar{A}B = \overline{\bar{A} \cdot \bar{B}} + AB$$

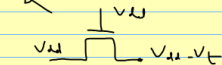
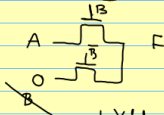
$$\overline{\text{out}} = \bar{A}\bar{B} + AB = \overline{A\bar{B} + \bar{A}B}$$



Pass Transistor Logic



$$F = A \cdot B$$



+ Reduce # tr

+ No pmos

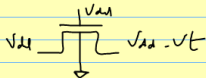
+ No static pwr

- Voltage swing
noise margin

- input imp

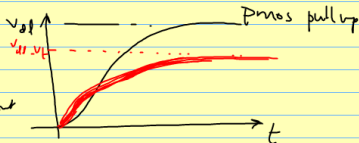
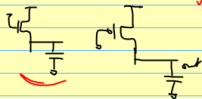
- delay

PTL Body Effect



$$V_t = V_{t0} + \gamma \left(\sqrt{2\phi_B + (V_{sd} - V_t)} - \sqrt{2\phi_B} \right)$$

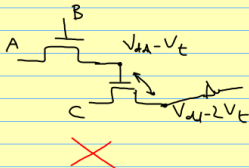
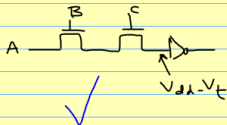
$$V_t > V_{t0}$$



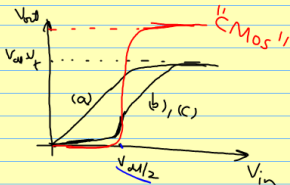
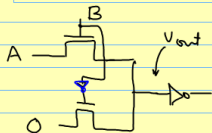
slow: V_t

Cascade Pass tr

$$F = A \cdot B \cdot C$$



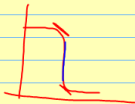
DC characteristics PTL



(a) $B=1$, $A: 0 \rightarrow 1$

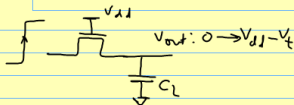
(b) $A=1$, $B: 0 \rightarrow 1$

(c) $A, B: 0 \rightarrow 1$



Power

PTL

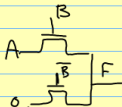


$$\begin{aligned}
 E_{0 \rightarrow 1} &= \int i(t) v_{DD} dt = \int_{t=0}^{\infty} C_L \frac{dv}{dt} v_{DD} dt = \int_0^{V_{DD}-V_t} v_{DD} dv \\
 &= C_L V_{DD} \underbrace{(V_{DD}-V_t)}_{\text{Swing}}
 \end{aligned}$$

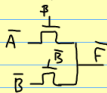
Differential PTL

$$F = A \cdot B$$

A \ B	0	1
0	0	0
1	0	1



$$\overline{F} = \overline{A \cdot B}$$



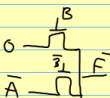
A \ B	0	1
0	1	1
1	1	0

$$F = A + B$$

A \ B	0	1
0	0	1
1	1	1



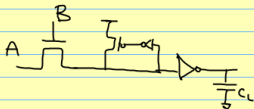
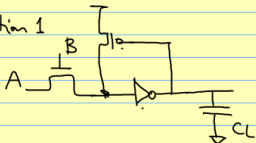
$$\overline{F} = \overline{A + B}$$



A \ B	0	1
0	1	0
1	0	0

Robust & Efficient PTL

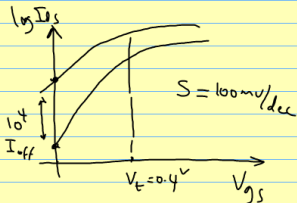
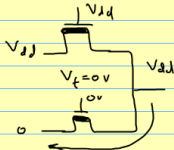
Solution 1



isolate large load

Better PTL

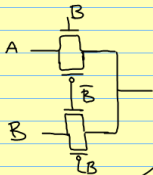
Solution 2



Better PTL

Solution 3: Transmission gates

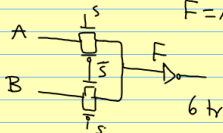
good for MUX
XOR



Multiplexer

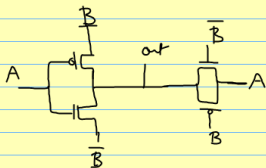
$$F = AS + B\bar{S}$$

CMOS
8



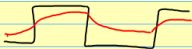
6 tr

XOR in PTL



$$B = 1 \quad out = \bar{A}$$

$$B = 0 \quad \xrightarrow{A'} \quad \xleftarrow{A}$$



$$B\bar{A} + \bar{B}A$$