Ratioed Logic (Pseudo_nmos)

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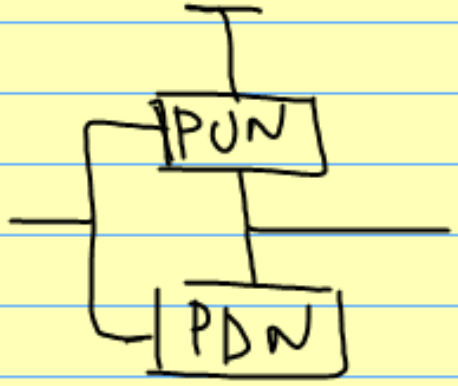
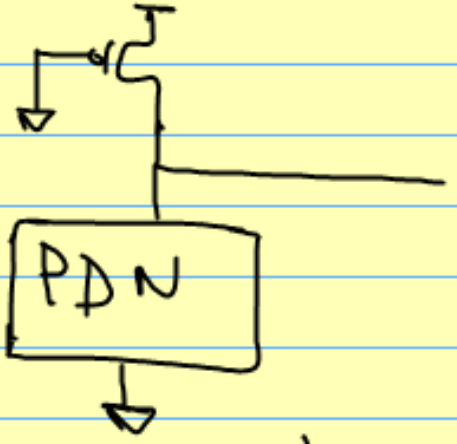
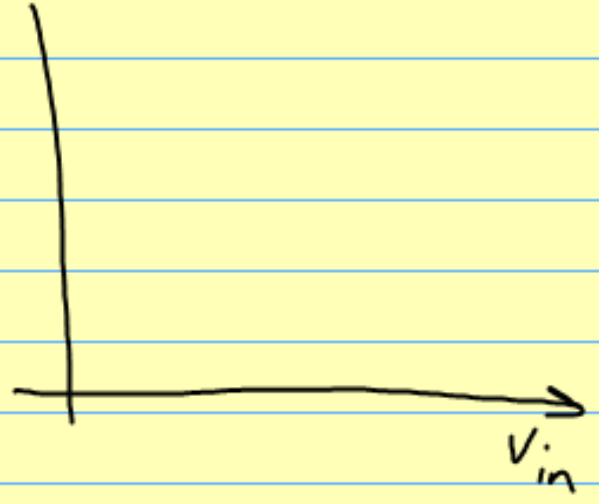
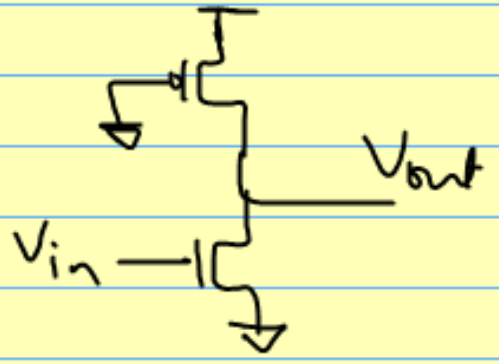




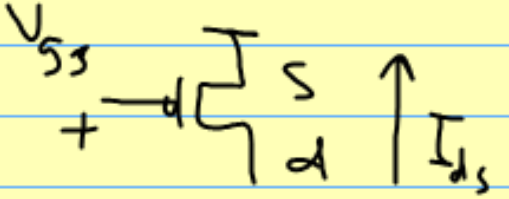
- Robustness $\times$ $V_{OL} > 0$
- Static power
+ Reduced # tr
+ Higher performance: cap ↓



Ratioed Logic : sizing W_p



$V_{ol} \sim 0$

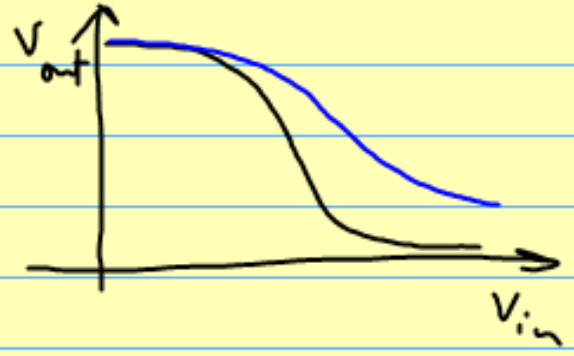


$$k_n\left((V_{dd}-V_{tn})V_{ol}-\frac{1}{2}V_{ol}^2\right)$$

$$= -k_p\left((-V_{dd}-V_{tp})V_{dsatp}-\frac{1}{2}V_{dsatp}^2\right)$$

$$V_{ol} \simeq -\frac{k_p}{k_n}\frac{(-V_{dd}-V_{tp})V_{dsat}}{V_{dd}-V_{tn}}$$

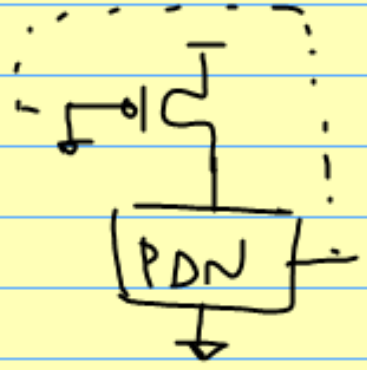
$$V_{ol} \propto -\frac{k_p}{k_n} = \left|\frac{\mu_p W_p}{\mu_n W_n}\right|$$



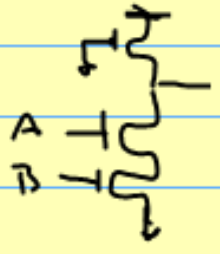
Ratioed Logic: Static Pwr

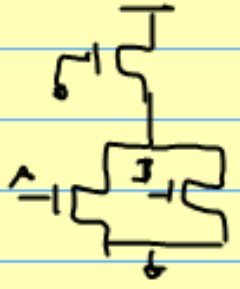
$$P_{static} = V_{dd} \cdot I \Big|_{V_{out}=V_{0l}}$$

$$= V_{dd} \cdot \left| k_p \left(-V_{dd} - V_t\right) V_{dsat_p} - \frac{1}{2} V_{dsat_p}^2 \right|$$

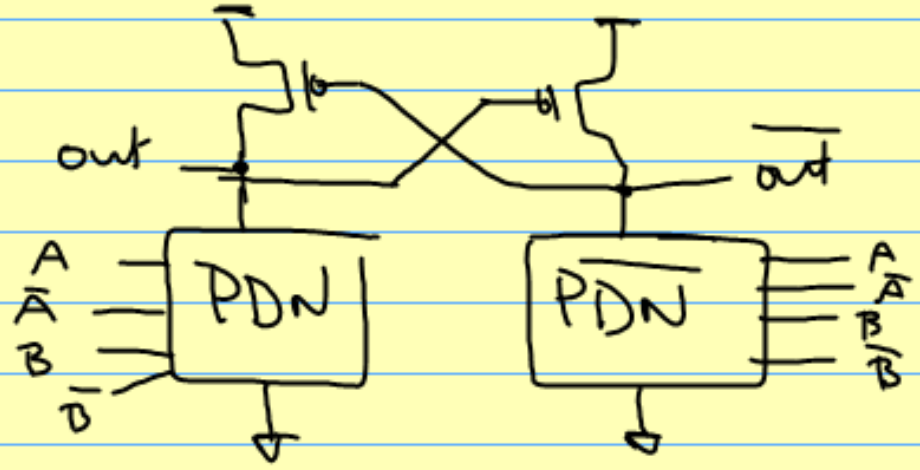


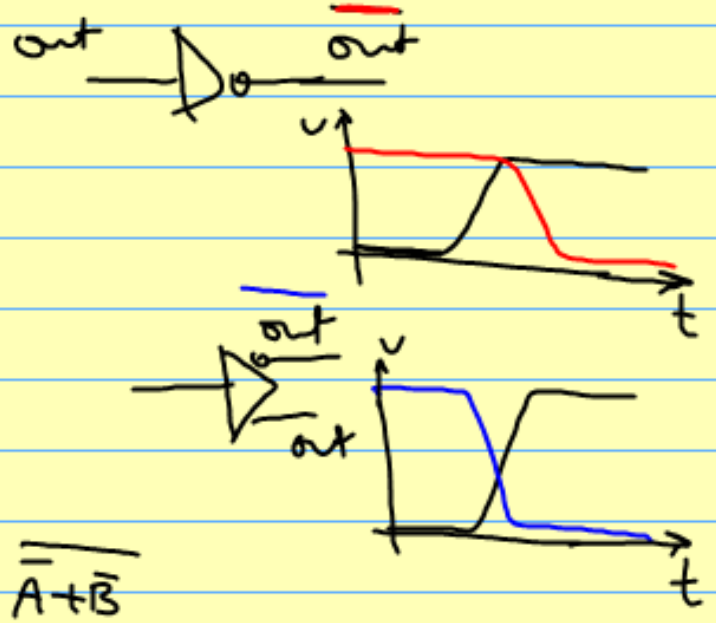
	area	delay/noise
NOR	✓	✓
NAND		



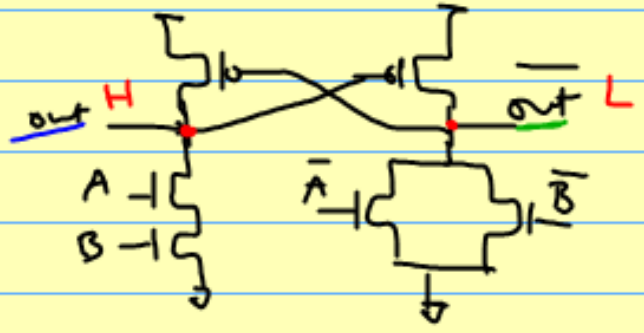


DCVSL : Differential Cascade Voltage Switch Logic





$out = \overline{A \cdot B}$ $\qquad \overline{out} = \overline{A \cdot B} = \bar{A} + \bar{B}$



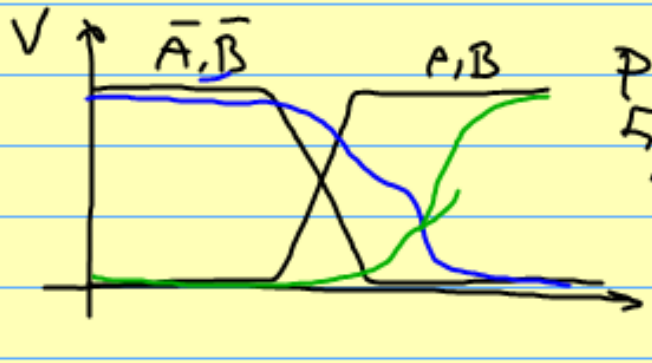


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Fig 6-31

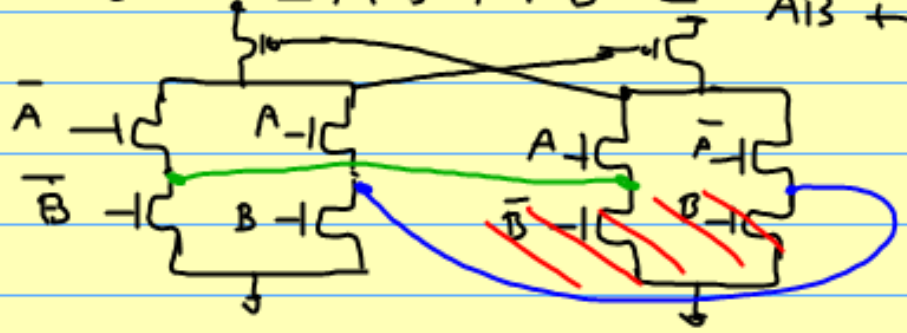
DCVSL

+ Reduces # tr
+ Rail-to-Rail voltage swing
+ No Static pwr
+ differential logic
+ share tr

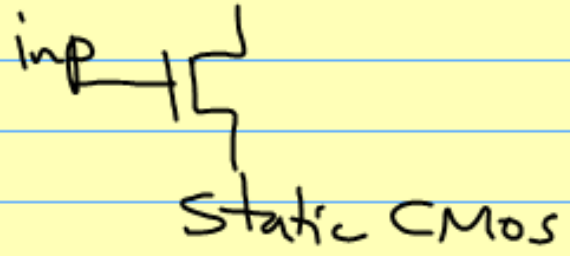
− still ratioed
− Design Complexity

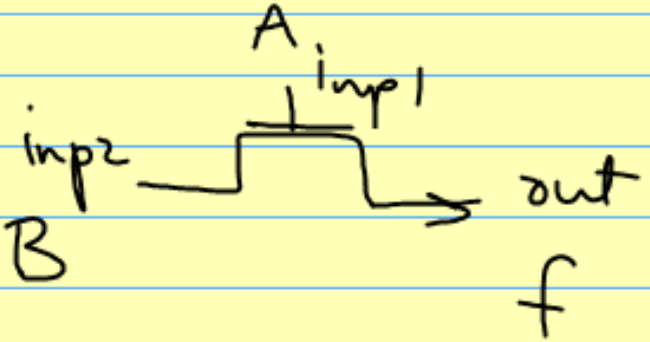
$$out = A\bar{B} + \bar{A}B = \overline{\bar{A}\cdot\bar{B} + AB}$$

$$\overline{out} = \bar{A}\bar{B} + AB = \overline{A\bar{B} + \bar{A}B}$$

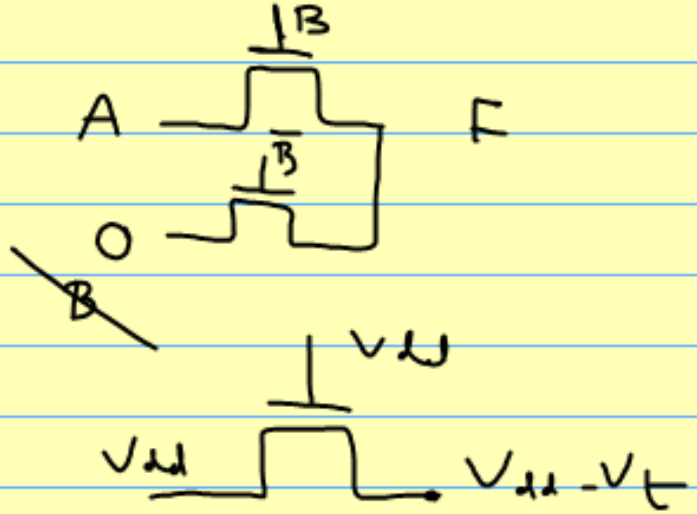


Pass Transistor Logic



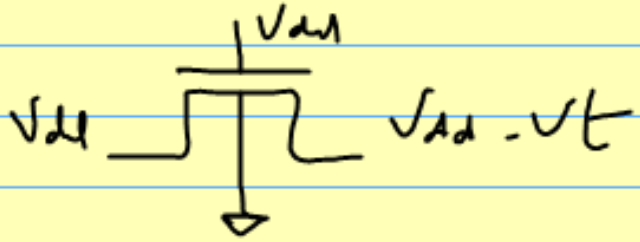


$F = A \cdot B$



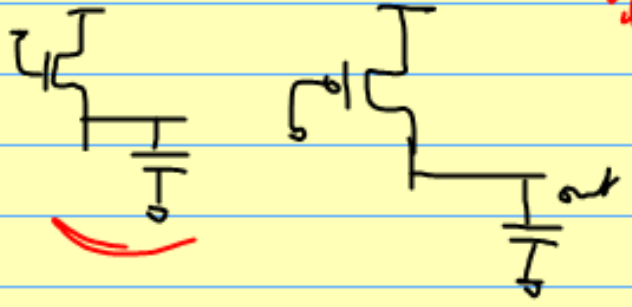
+ Reduce # tr
+ No pmos
+ No static pwr
− Voltage swing
noise margin
− input imp
− delay

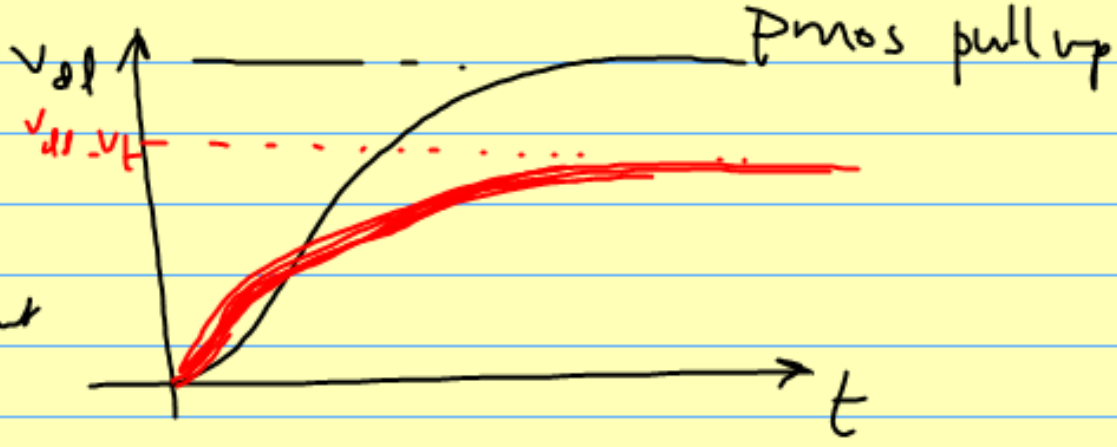
PTL Body Effect



$$V_t = V_{t_0} + \gamma\left(\sqrt{2\gamma_B + (V_{dd} - V_t)} - \sqrt{2\gamma_B}\right)$$

$$V_t > V_{t_0}$$





slow: V_t

Cascade Pass tr

$F = A \cdot B \cdot C$