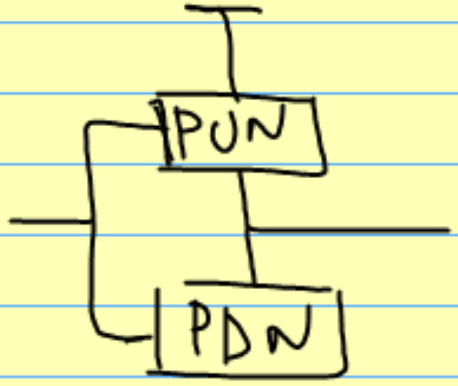
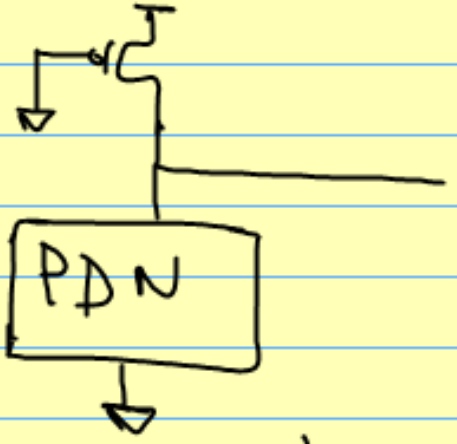
# Ratioed Logic (Pseudo_nmos)

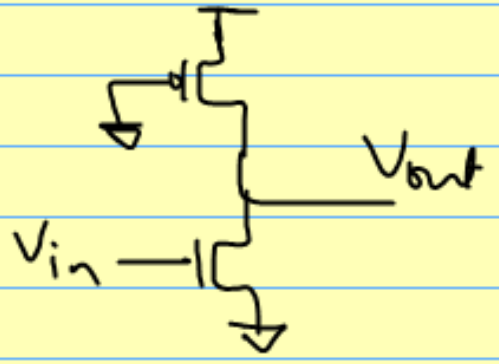
p263



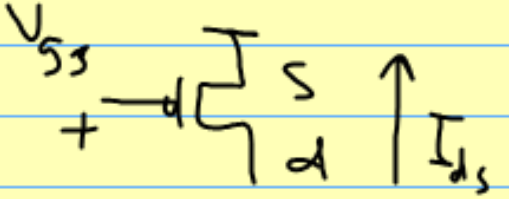




- Robustness X $V_{OL} > 0$
- Static power
+ Reduced # tr
+ Higher performance: cap ↓

# Ratioed Logic : sizing $W_p$




$V_{ol} \sim 0$

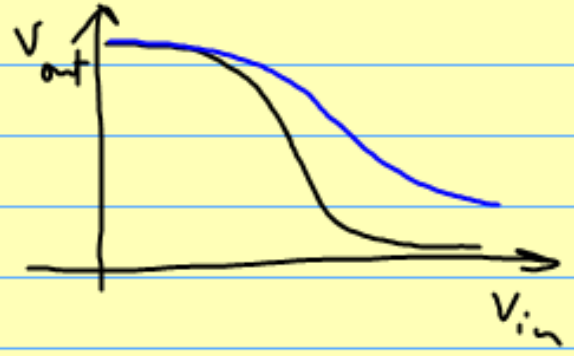



$$k_n\left((V_{dd}-V_{tn})V_{ol}-\frac{1}{2}V_{ol}^2\right)$$

$$= -k_p\left((-V_{dd}-V_{tp})V_{dsatp}-\frac{1}{2}V_{dsatp}^2\right)$$

$$V_{ol} \simeq -\frac{k_p}{k_n}\frac{(-V_{dd}-V_{tp})V_{dsat}}{V_{dd}-V_{tn}}$$

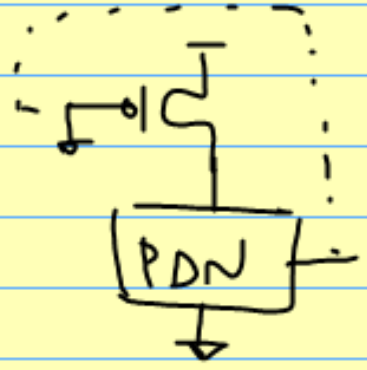
$$V_{ol} \propto -\frac{k_p}{k_n} = \left|\frac{\mu_p W_p}{\mu_n W_n}\right|$$



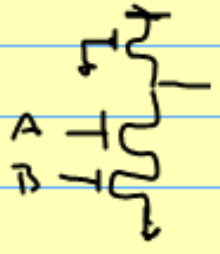
# Ratioed Logic: Static Pwr

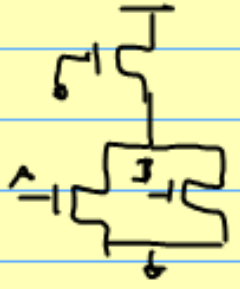
$$P_{static} = V_{dd} \cdot I\Big|_{V_{out}=V_{0l}}$$

$$= V_{dd} \cdot \left| k_p (-V_{dd} - V_t) V_{dsat_p} - \frac{1}{2} V_{dsat_p}^2 \right|$$

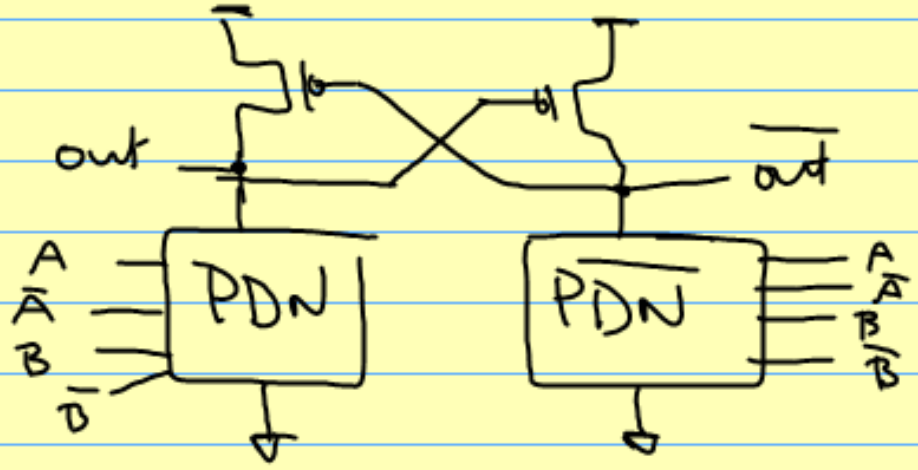


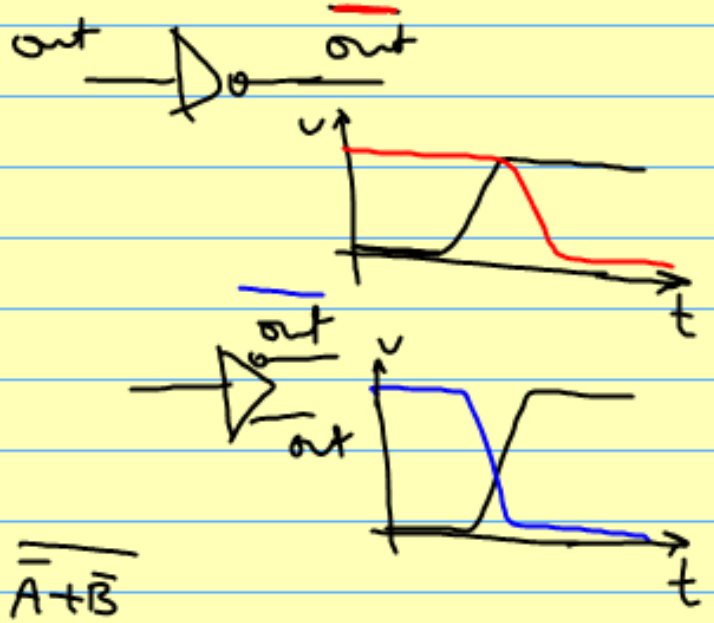

| | area | delay/noise |
|---|---|---|
| NOR | ✓ | ✓ |
| NAND | | |



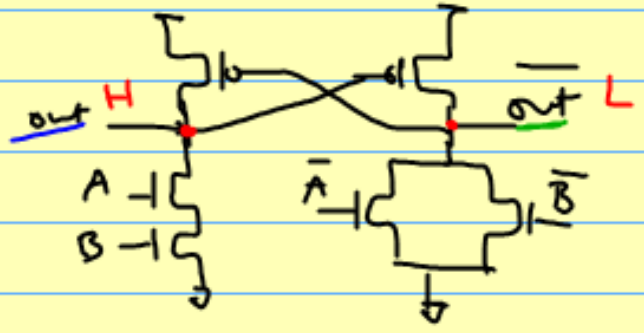



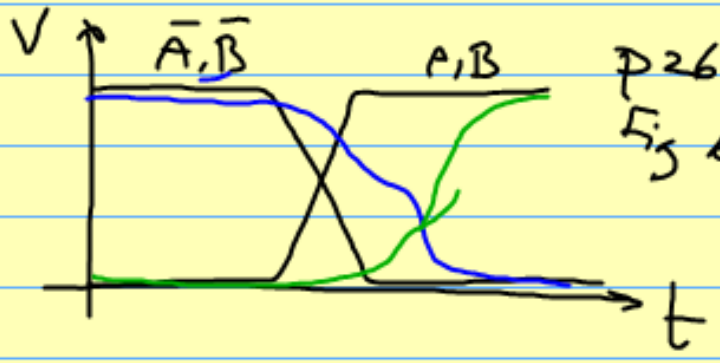
# DCVSL : Differential Cascade Voltage Switch Logic




$out = \overline{A \cdot B}$ $\qquad \overline{out} = \overline{A \cdot B} = \bar{A} + \bar{B}$




p268
Fig 6-31