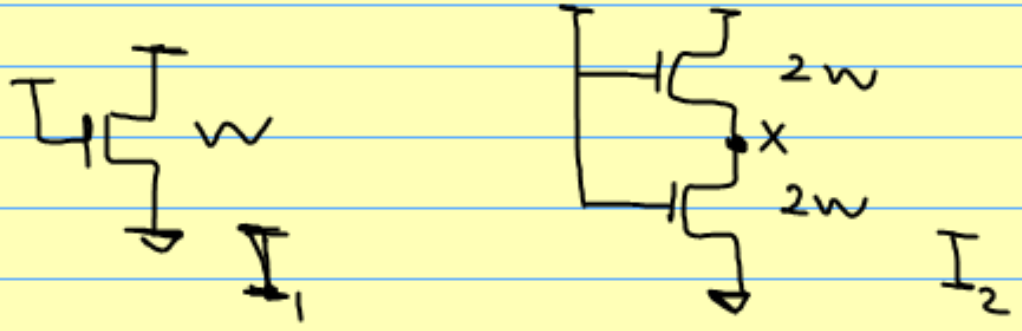
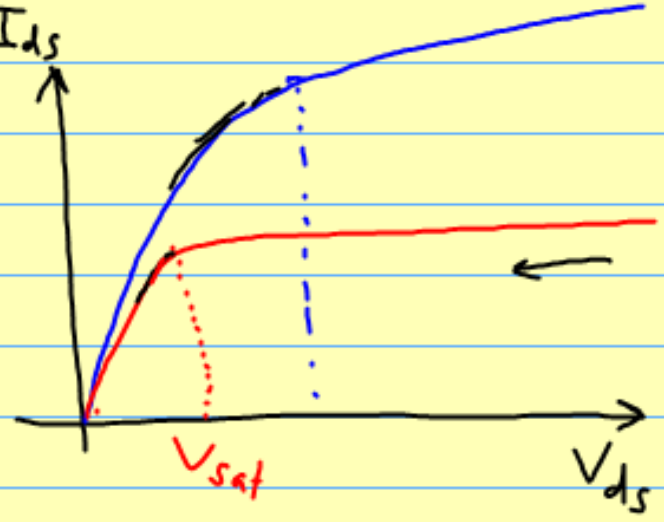
Long ch vs Sh ch

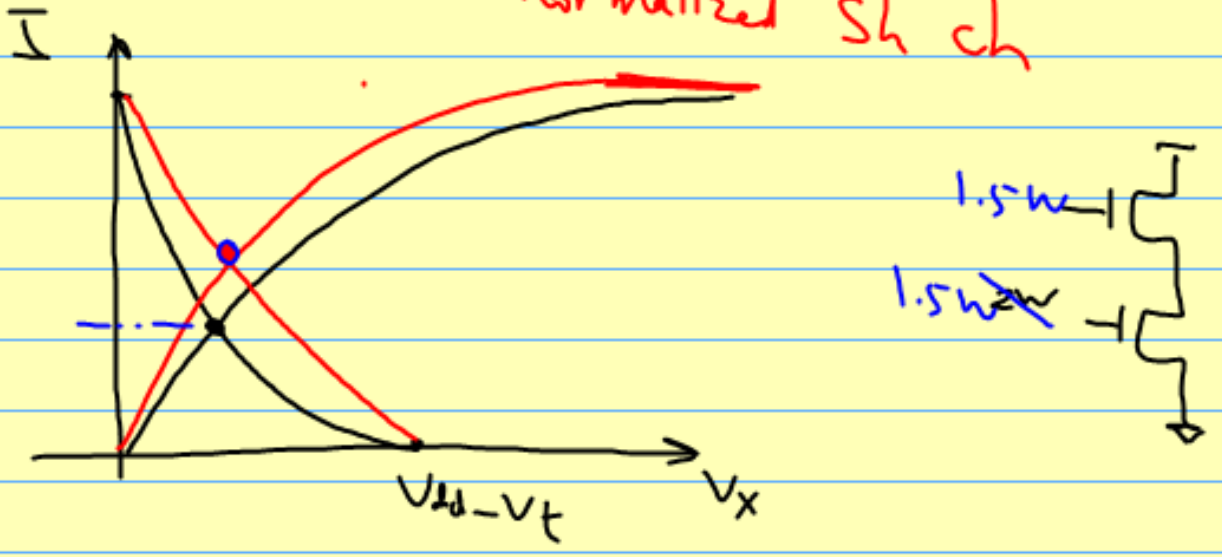


Long channel (no vel sat)

$$I_1 = I_2$$

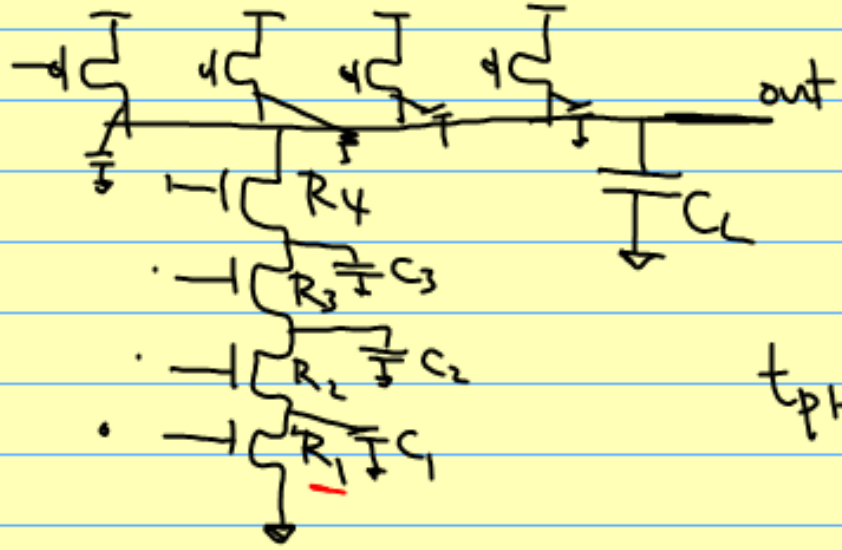
Short ch $I_1' < I_2'$




normalized Sh ch
I
$V_{dd}-V_t$
V_x

1.5w
1.5w

Speedup Tech CMOS



High-fan in gates
BAD idea

$$t_{pHL} = 0.69 \times \left[C_1 R_1 + C_2 (R_1 + R_2) + C_3 (R_1 + R_2 + R_3) + C_L (R_1 + R_2 + R_3 + R_4) \right]$$

assume $R = R_1 = R_2 = \cdots$

$$t_{pHL} = 0.69 \cdot R (C + 2C + 3C + 4C_L)$$

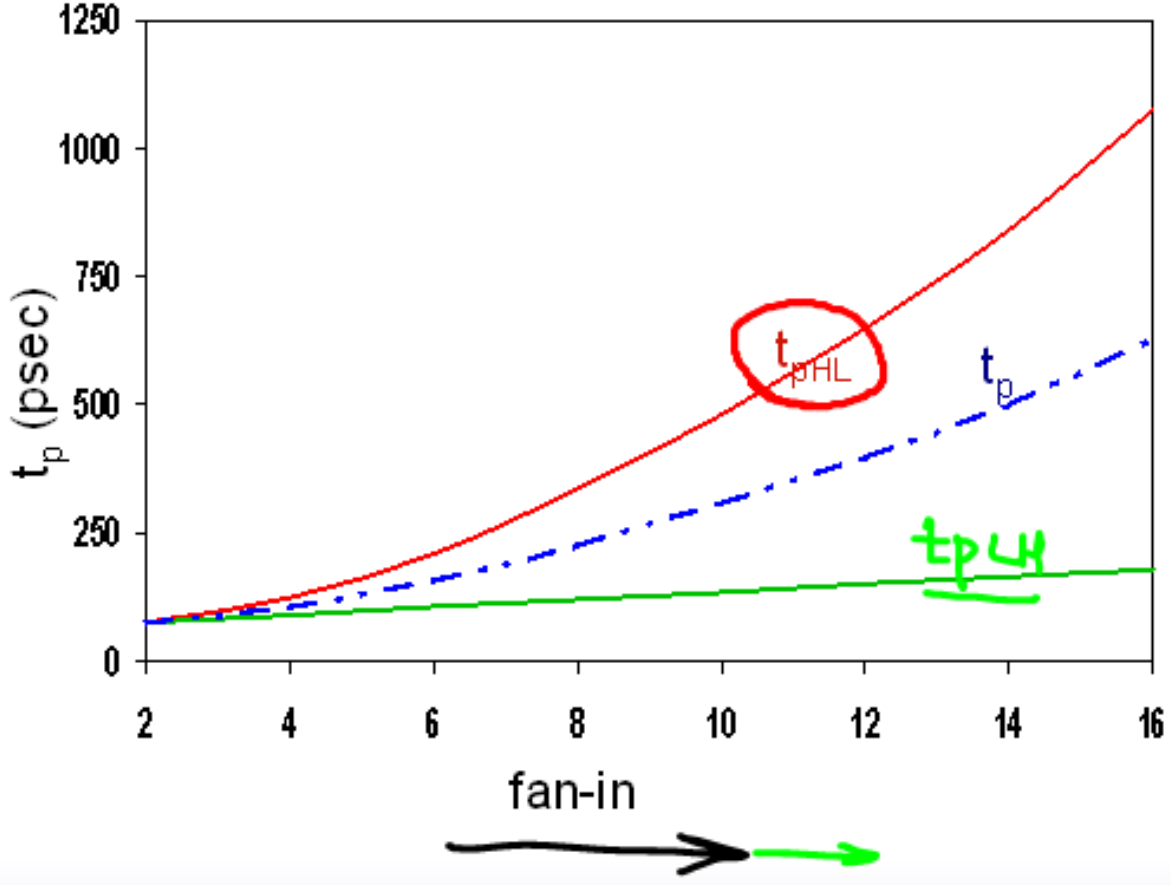
$$= 0.69 \cdot RC (1 + 2 + 3 + \cdots N)$$

N : fan in

$$t_{PLH} = \bigcirc^{N}$$

$C_L \gg C_1, C_2, C_3$

t_p as a Function of Fan-In



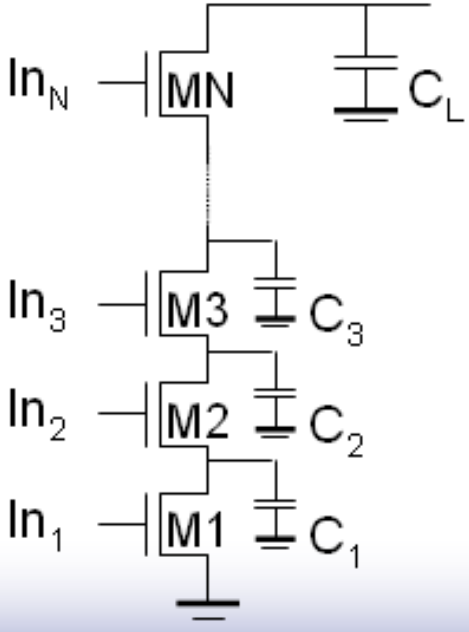
Gates with a fan-in greater than 4 should be avoided.

Fast Complex Gates: Design Technique 1

- Transistor sizing
  - as long as fan-out capacitance dominates
- Progressive sizing

Distributed RC line

width

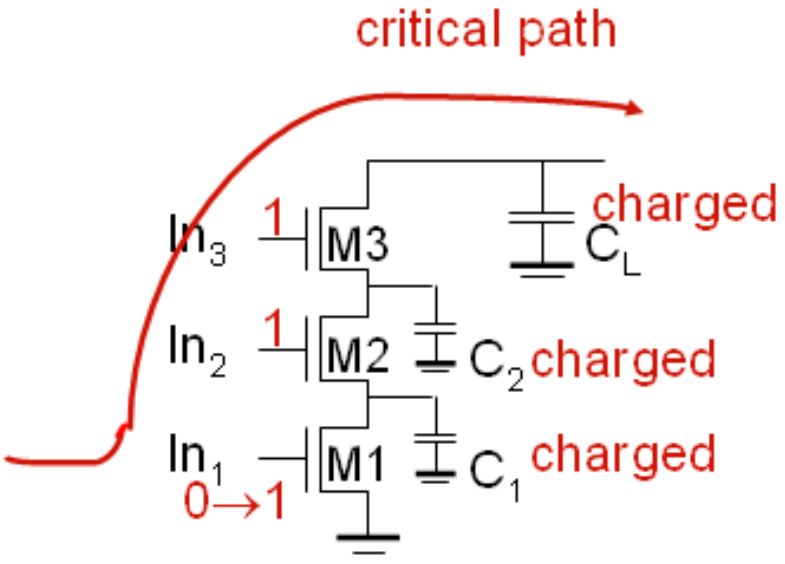


M1 > M2 > M3 > … > MN
(the fet closest to the output is the smallest)

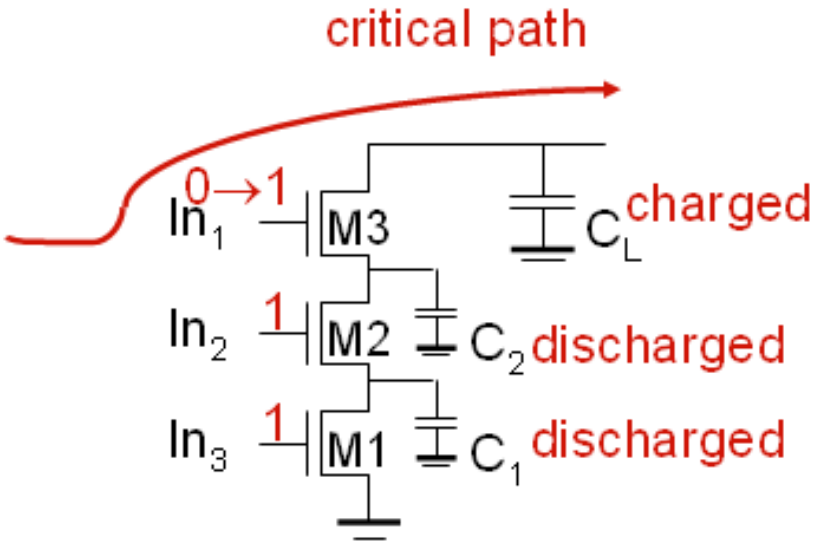
Can reduce delay by more than 20%; decreasing gains as technology shrinks

Fast Complex Gates: Design Technique 2

- Transistor ordering



delay determined by time to discharge C_L, C_1 and C_2

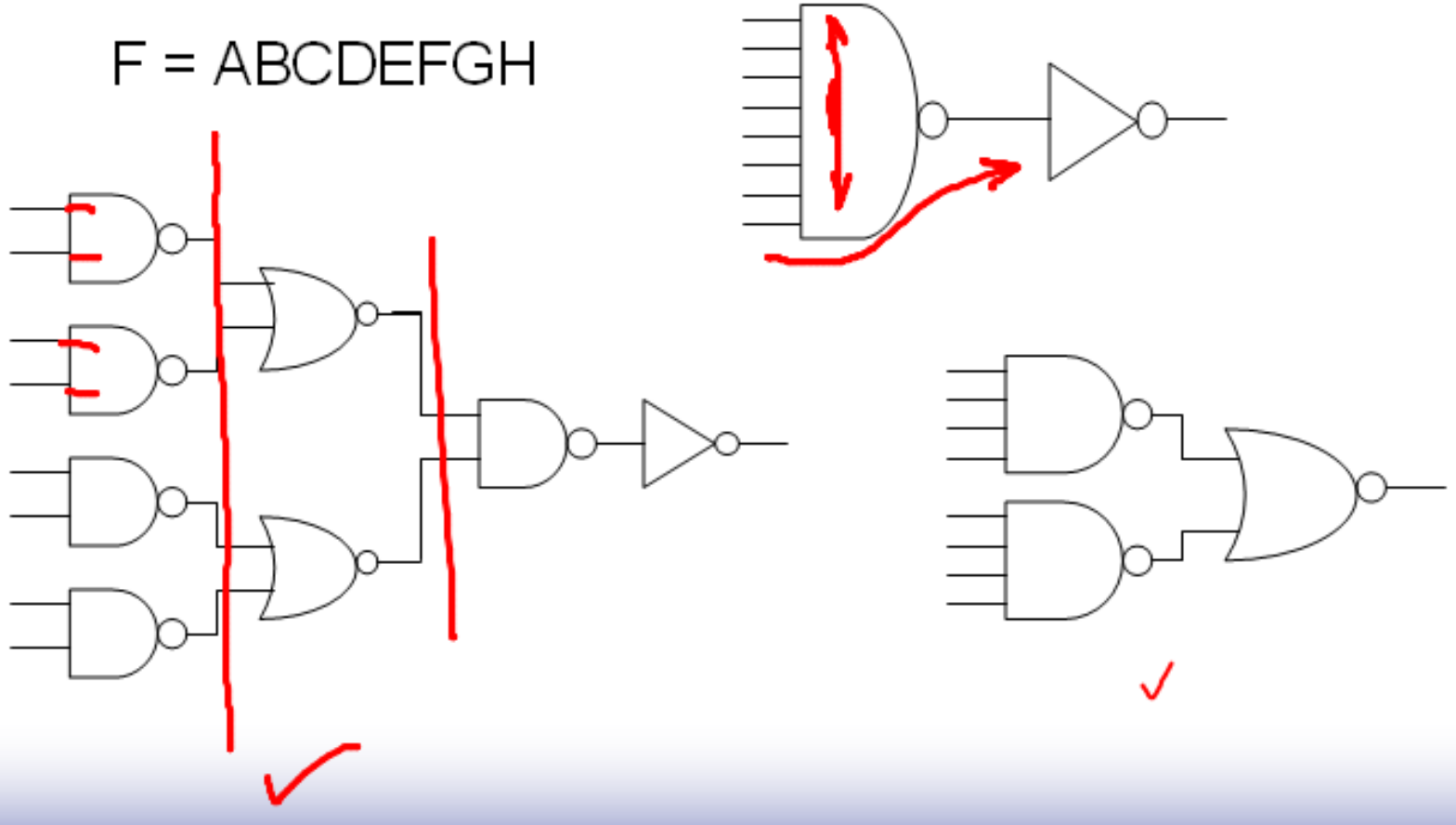


delay determined by time to discharge C_L

Fast Complex Gates: Design Technique 3

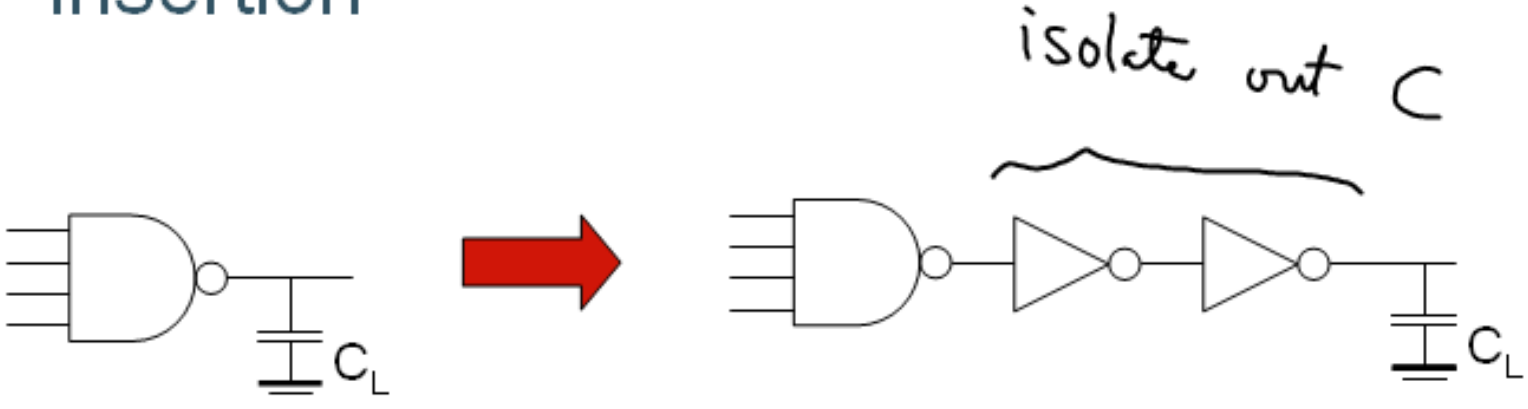
- Alternative logic structures

F = ABCDEFGH



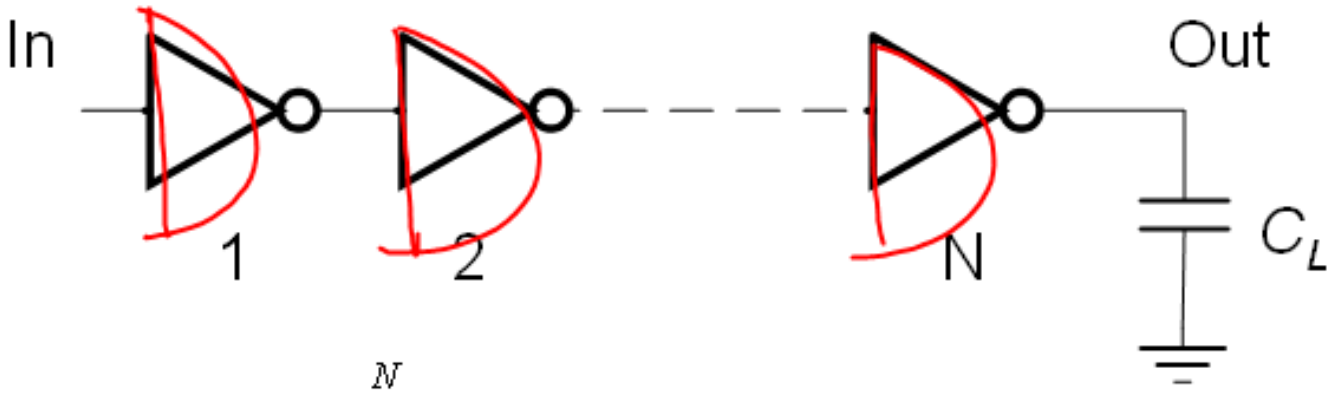
Fast Complex Gates: Design Technique 4

- Isolating fan-in from fan-out using buffer insertion



Buffer Example

$g_{NAND} = \frac{4}{3}$



$$Delay = \sum_{i=1}^{N} (p_i + g_i \cdot f_i)$$

(in units of τ_{inv})

For given N: $C_{i+1}/C_i = C_i/C_{i-1}$

To find N: $C_{i+1}/C_i \sim 4$ → 3.6

How to generalize this to any logic path?