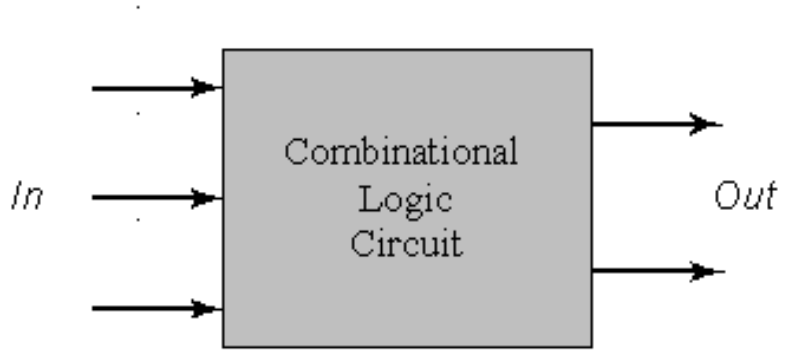
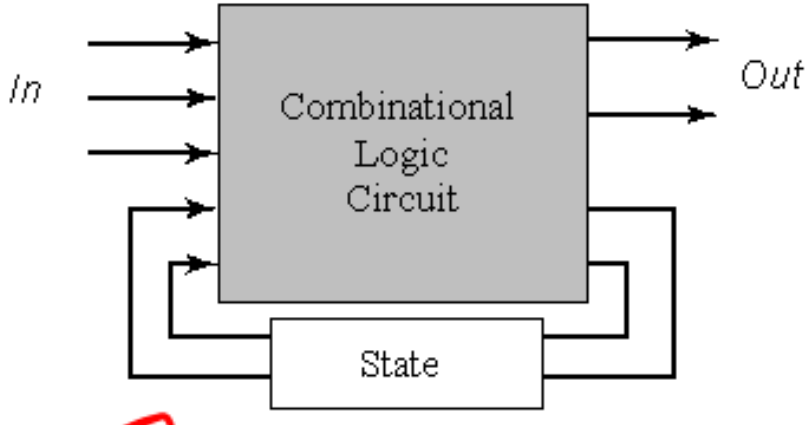
Combinational vs. Sequential Logic





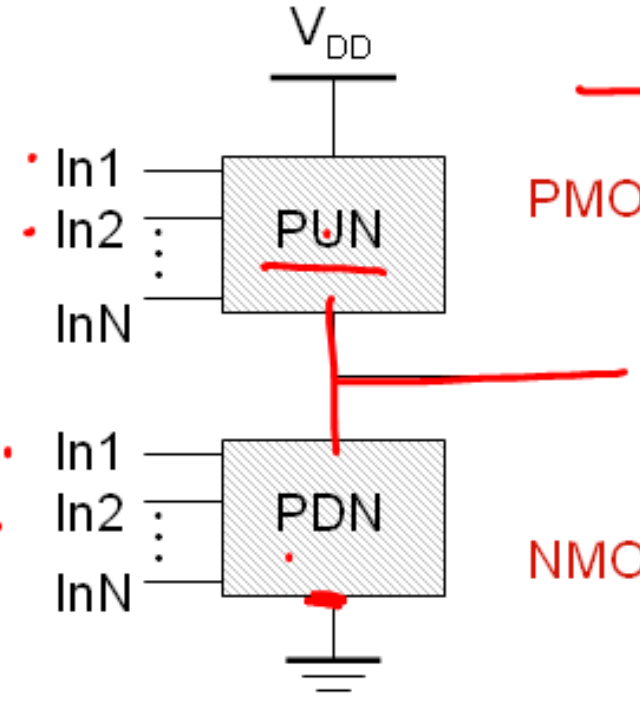
Combinational

Sequential

Output = *f*(*In*)

Output = *f*(*In, Previous In*)

Static Complementary CMOS



PMOS only

F(In1,In2,...InN)

Pull Down Network

NMOS only

PUN and PDN are dual logic networks

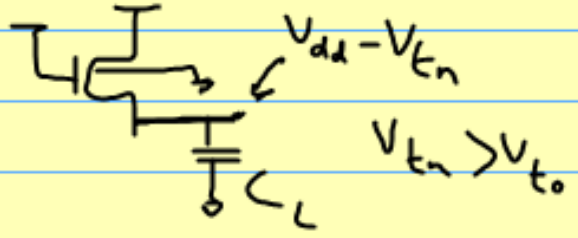
Combinational Logic Ch6

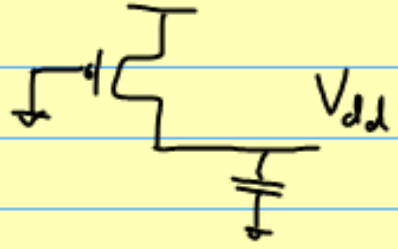
Static CMOS

— PUN and PDN EXCLUSIVE

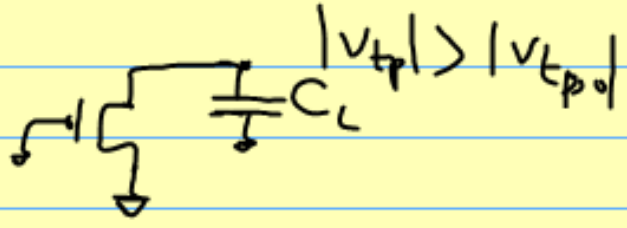
⇒ out conn EITHER Vdd or GND

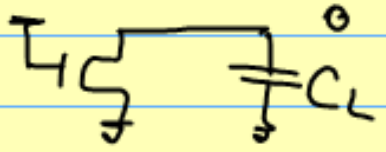
Pull-up:



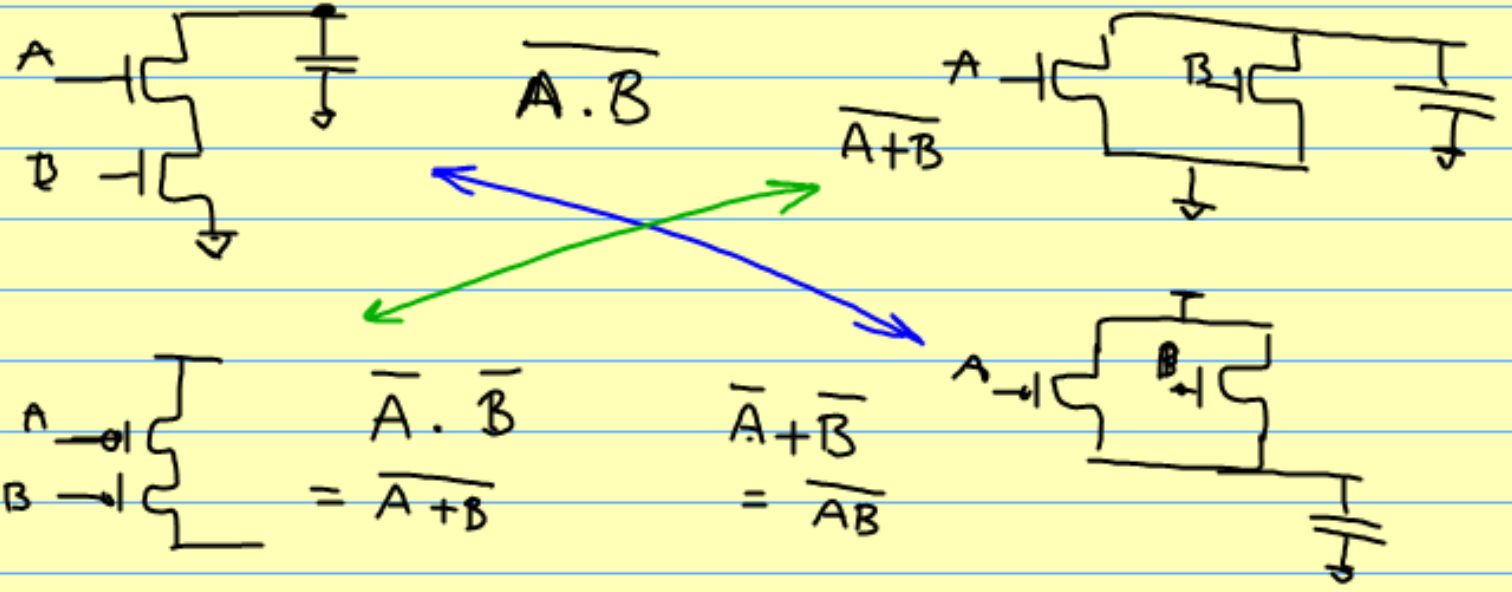


Pull-down:

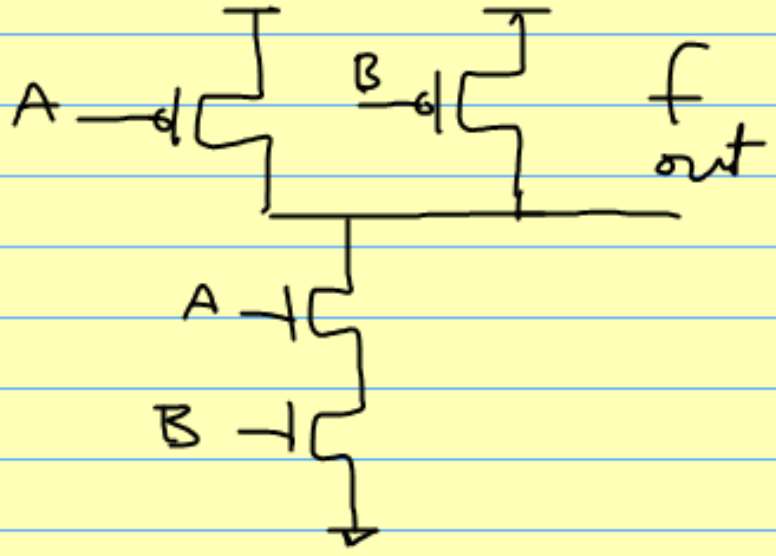




Logic Gates



NAND Gate (Static, Comp CMOS)

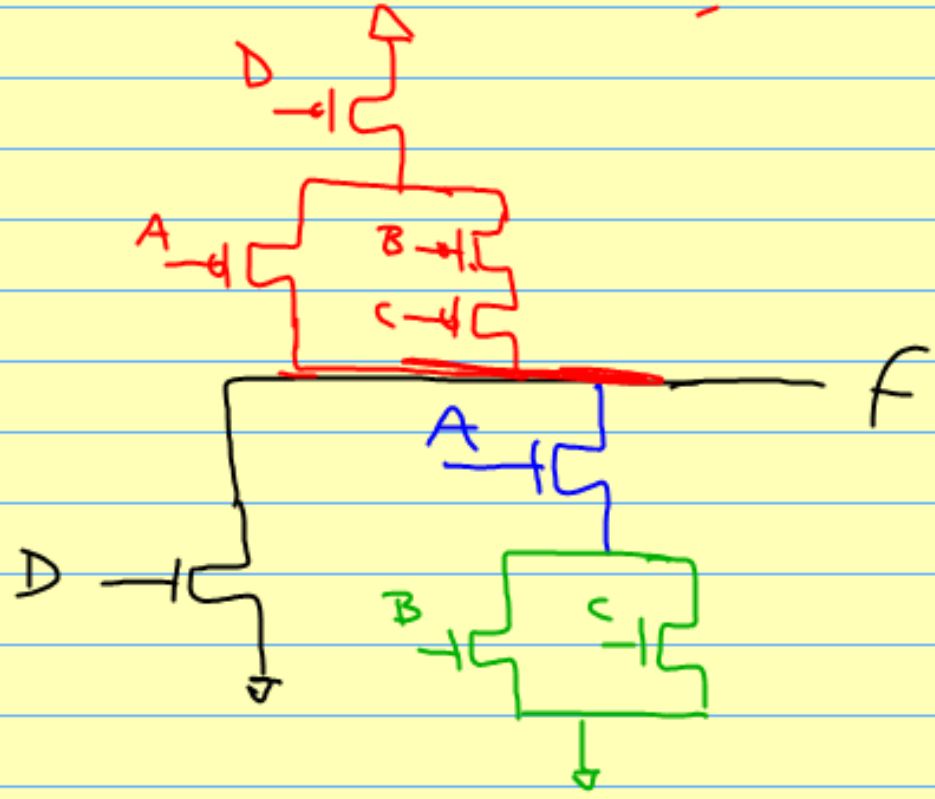


A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

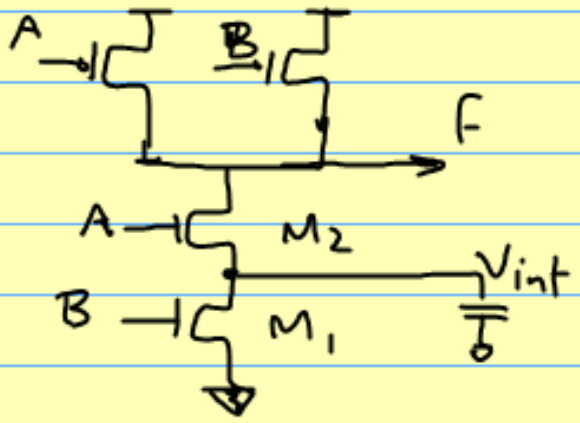
- Dual networks (series ⟷ parallel)
- inverting logic
- AND logic? add inv to out
- N inp func ⟶ 2N tr

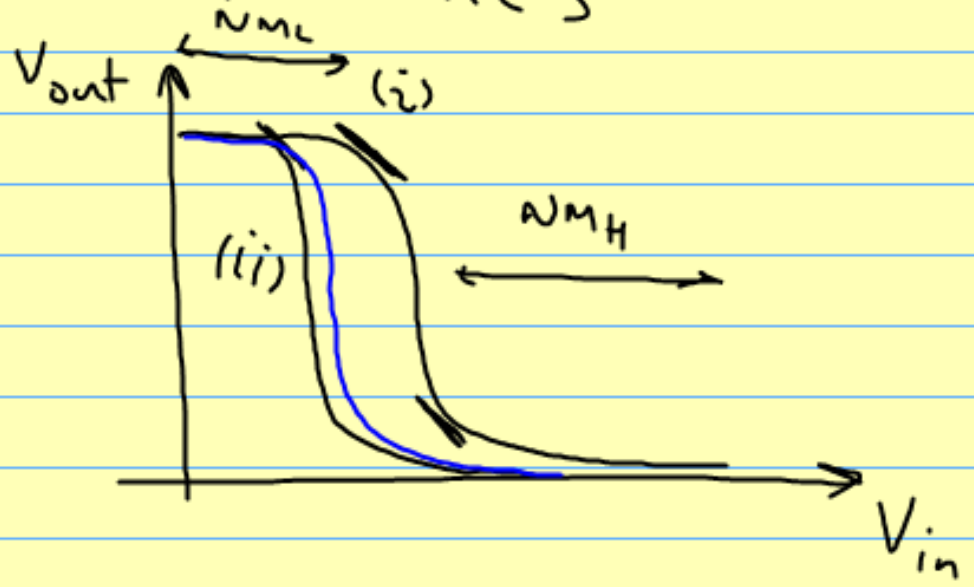
Complex CMOS func

$$F = \overline{D + (A \cdot \overline{(B+C)})}$$



DC characteristics





(i) $A = B : 0 \longrightarrow 1$

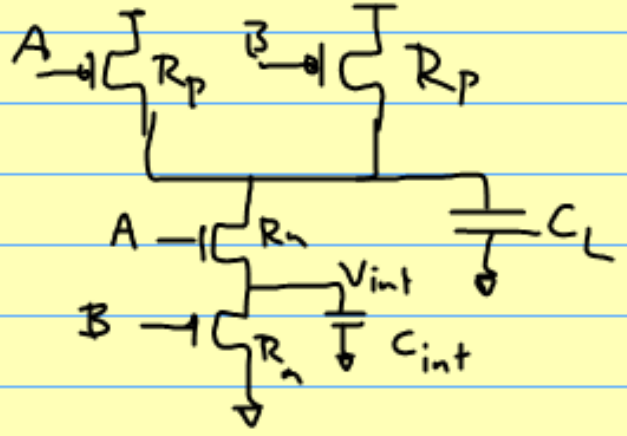
(ii) $A = 1$, $B : 0 \longrightarrow 1$ (pull up weaker (i).

(iii) $B = 1$, $A : 0 \longrightarrow 1$ nmos not as strong as (ii)

$$V_t(M_1) = V_{t_0}$$

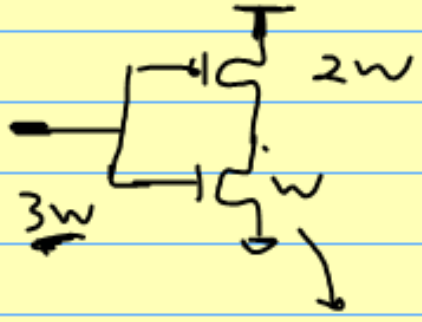
$$V_t(M_2) = V_{t_0} + \gamma \left(\sqrt{2\phi_B + V_{int}} - \sqrt{2\phi_B} \right)$$

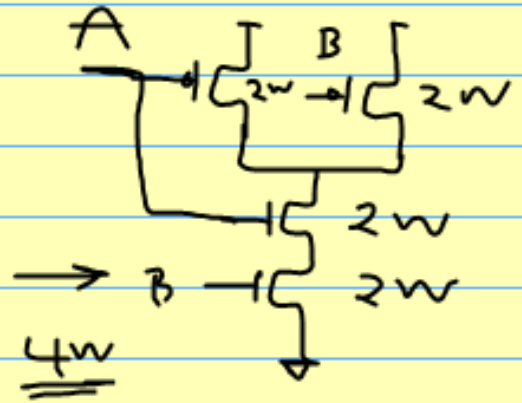
NAND: Propagation Delay

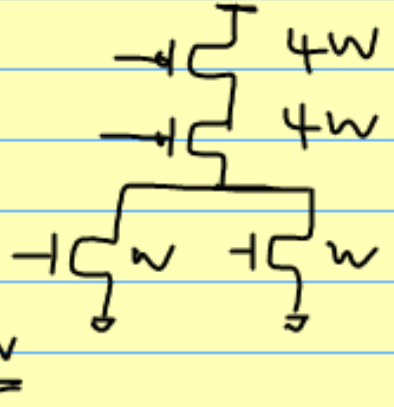


$$t_{pLH} = \begin{cases} A = B : 1 \to 0 \\ \quad 0.69 \frac{R_p}{2} \cdot C_L \\ B = 1,\ A : 1 \to 0 \quad (A = 1, B : 1 \to 0) \\ \quad 0.69\ R_p C_L \end{cases}$$

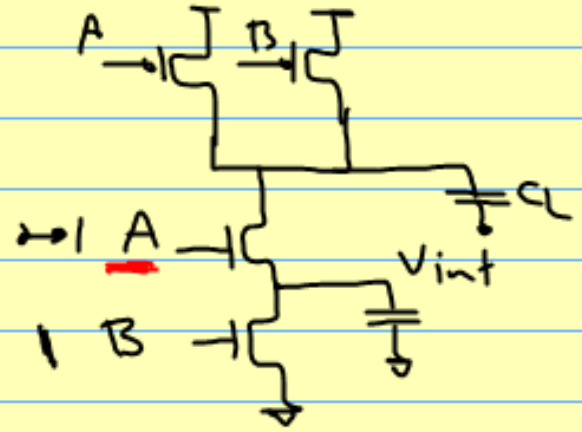
$$t_{pHL} = 0.69 \times 2 R_n C_L$$







Simulation NAND



t_{PLH}

(i) A=B : 1 → 0 fastest 35ps

(ii) A=1, B=1 → 0 slowest 76ps

(iii) B=1 A : 1 → 0 57ps

t_{pHL}

(i) A=B : 0 → 1 slowest 69ps

(ii) A=1, B: 0 → 1 62ps

(iii) B=1, A: 0 → 1 fastest 50ps