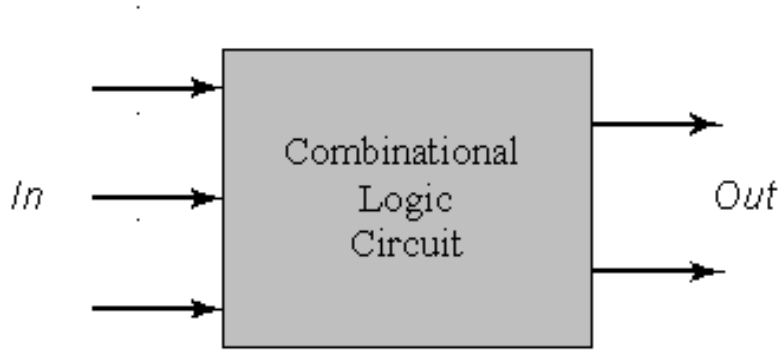
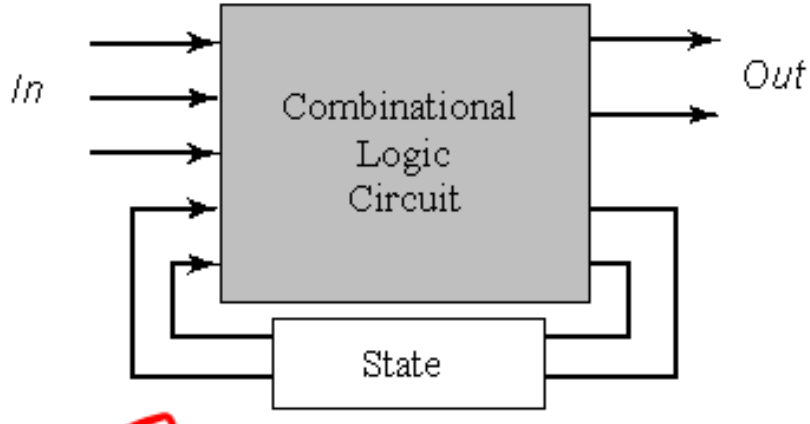
Combinational vs. Sequential Logic



Combinational

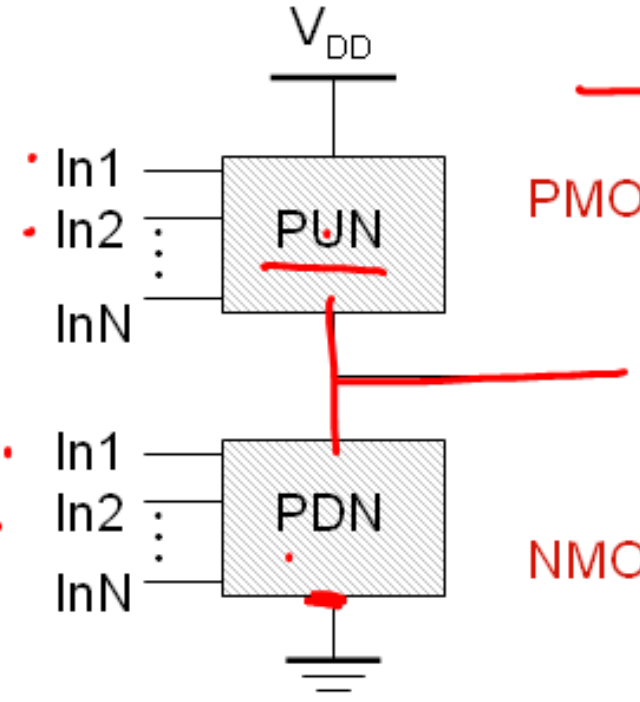


Sequential

Output = *f*(*In*)

Output = *f*(*In, Previous In*)

Static Complementary CMOS



F(In1,In2,...InN)

Pull Down Network

NMOS only

PUN and PDN are dual logic networks

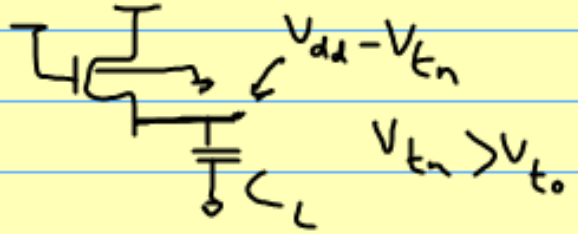
Combinational Logic Ch6

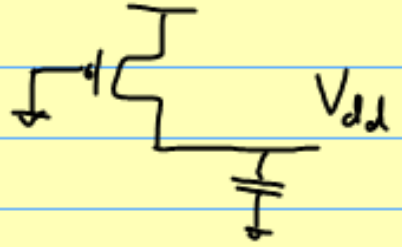
Static CMOS

— PUN and PDN EXCLUSIVE

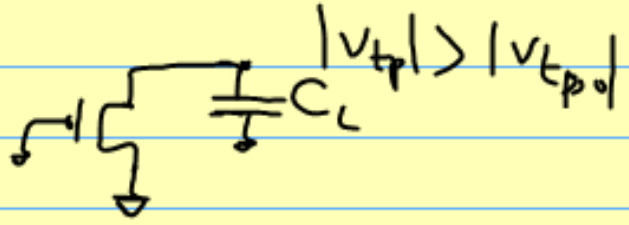
⇒ out conn EITHER Vdd or GND

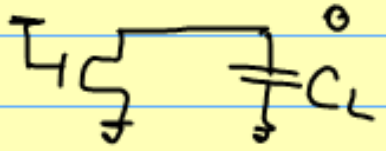
Pull-up:



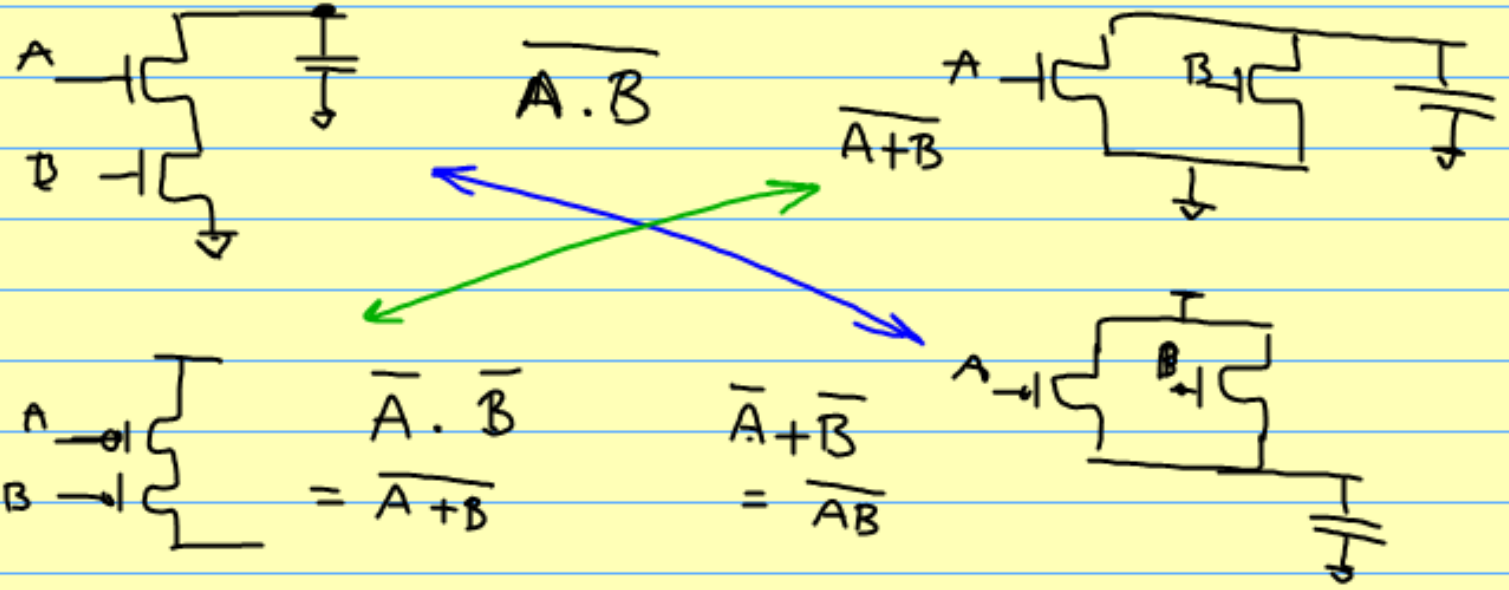


Pull-down:

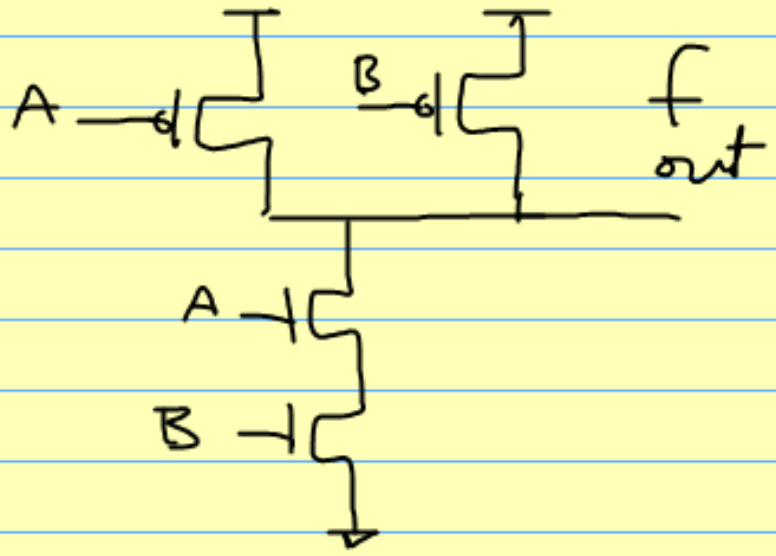




Logic Gates



NAND Gate (Static, Comp CMOS)



A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

- Dual networks (series ⟷ parallel)
- inverting logic
- AND logic? add inv to out
- N inp func ⟶ 2N tr

Complex CMOS func

$$F = \overline{D + (A \cdot (B + C))}$$