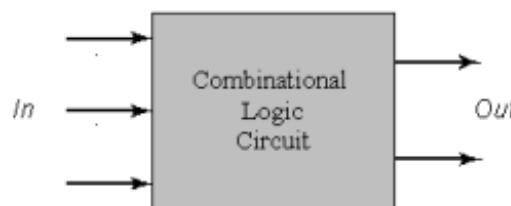
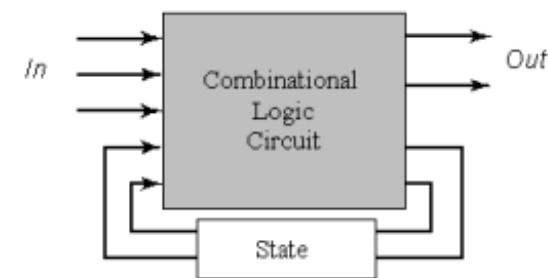


## Combinational vs. Sequential Logic



Combinational

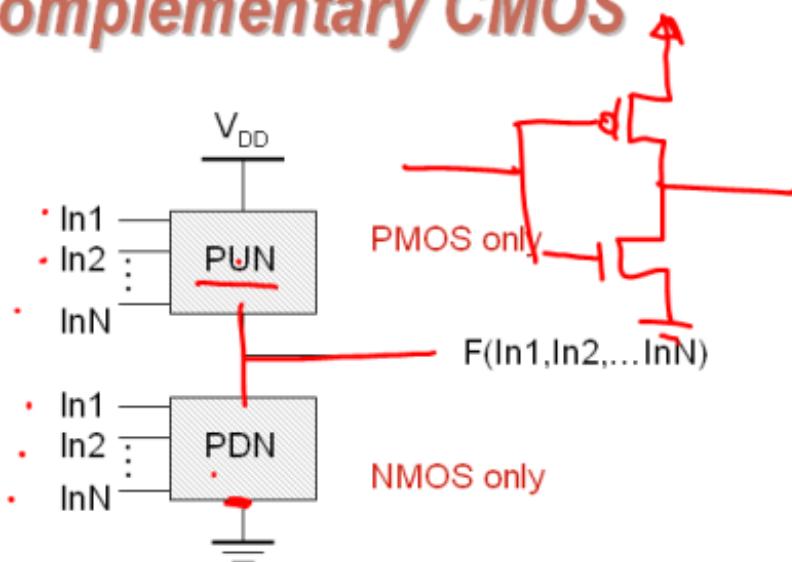
$$\text{Output} = f(\text{In})$$



Sequential

$$\text{Output} = f(\text{In}, \text{Previous In})$$

# Static Complementary CMOS



Pull Down Network

PUN and PDN are **dual** logic networks

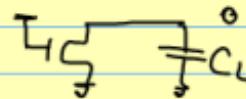
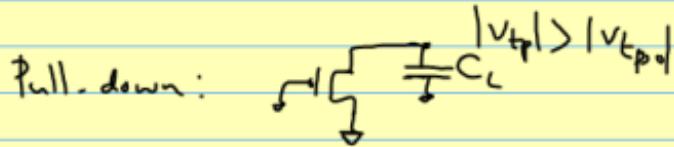
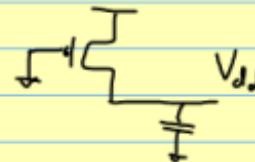
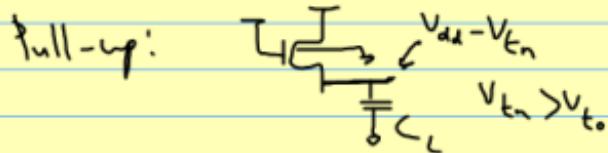
# Combinational Logic

Ch6

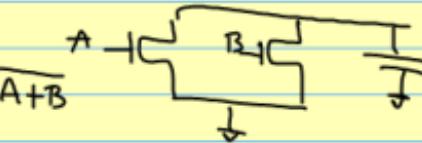
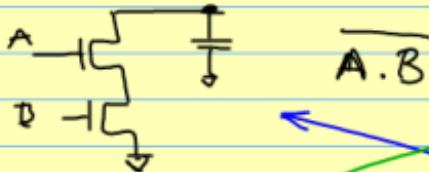
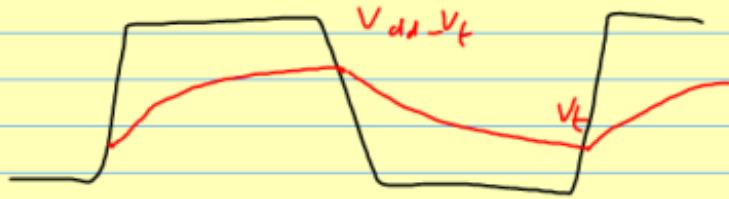
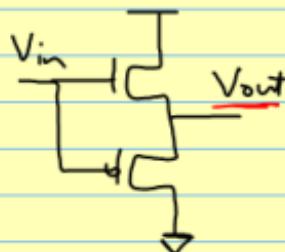
Static CMOS

- PUN and PDN EXCLUSIVE

$\Rightarrow$  out conn EITHER Vdd or Gnd



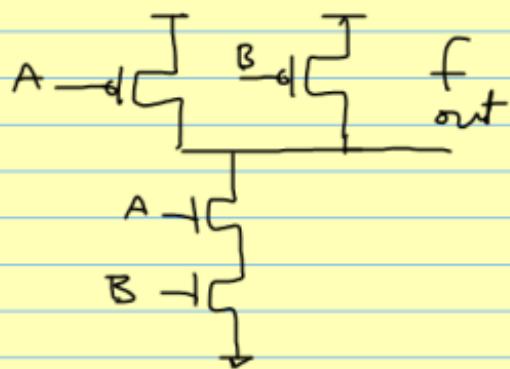
# Logic Gates



A circuit diagram of an AND-OR gate. It consists of two NMOS transistors in series. The first transistor has its gate at input  $A$  and its drain connected to the second transistor's gate. The second transistor has its gate at input  $B$  and its drain connected to the output node. The source of the second transistor is connected to ground. The output voltage is labeled  $\overline{A} \cdot \overline{B} = \overline{A+B}$ .

A circuit diagram of an OR-AND gate. It consists of two NMOS transistors in parallel. The first transistor has its gate at input  $A$  and its drain connected to the second transistor's gate. The second transistor has its gate at input  $B$  and its drain connected to the output node. The source of the second transistor is connected to ground. The output voltage is labeled  $\overline{A} + \overline{B} = \overline{AB}$ .

# NAND Gate (Static, Comp(Mos))



A	B	f
0	0	1
0	1	1
1	0	1
1	1	0

- Dual networks (Series  $\leftrightarrow$  parallel)
- Inverting logic
- AND logic? add inv to out
- N inp func  $\longrightarrow$   $2^N$  tr

## Complex CMOS func

$$F = \overline{D} + \underline{A} \cdot (\underline{B} + \underline{C})$$

