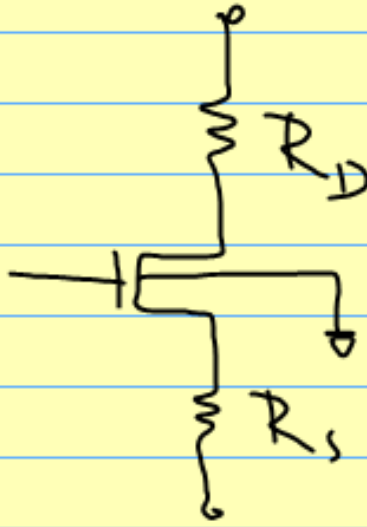
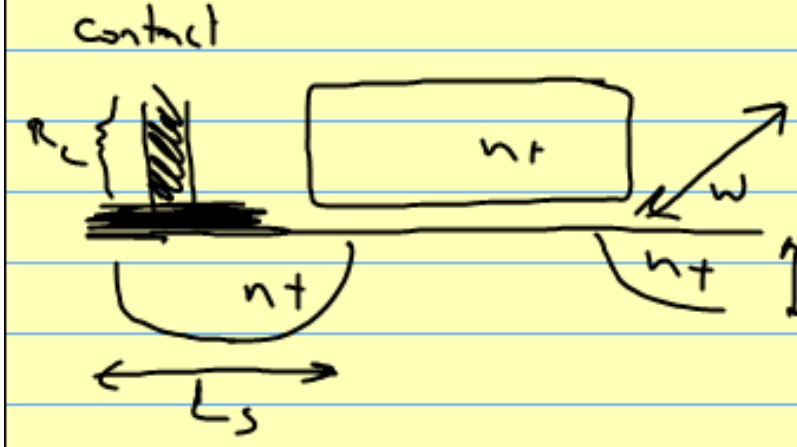
# Source - Drain Resistance




$R_{SD}$: $V_{gs}\downarrow$ $V_{ds}\downarrow$ $V_{bs}\downarrow$

$V_{gs}\downarrow \rightarrow I_{ds}\downarrow$

$V_{ds}\downarrow \rightarrow$ DIBL, CLM $\rightarrow V_t\uparrow$




$$R_{s,D} = \frac{L_{s,D}}{W} \cdot R_{\square} + R_c$$

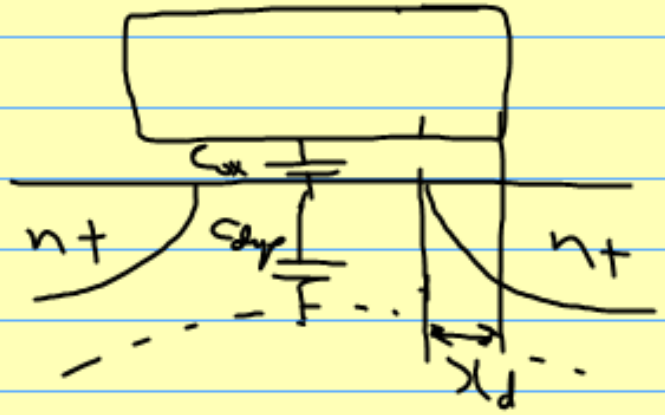
$R_{\square}$: Sheet Resistance

# Scaling Revisited

$$(W', L', t_{ox}', X_j', W_{dep}') = \frac{1}{S}(W, L, t_{ox}, X_j, W_{dep})$$

# MOS Structure Cap

(i) Intrinsic cap

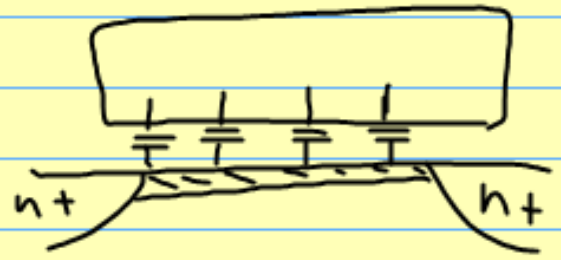



Cut-off region

$$C_g = W \times L \times (C_{ox} \| C_{dep})$$

$$\approx WL\, C_{dep}$$

$$(C_{gs} = C_{gd} = 0,\ C_{gb} = WLC_{dep})$$

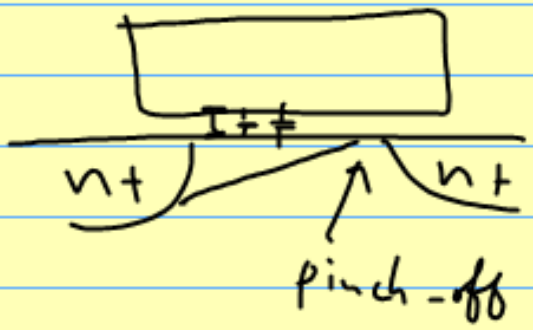



$$C_g = W \times L \times C_{ox}$$

$$(C_{gs} = C_{gd} = \tfrac{1}{2} WL\, C_{ox},\ C_{gb} = 0)$$

at low drain bias

# Intrinsic MOS Cap (Cont)

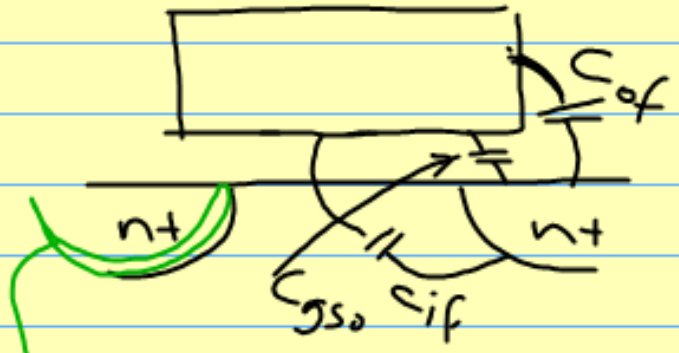



$$C_g = \frac{2}{3} WL C_{ox}$$

$$\left(C_{gs} = \frac{2}{3} WL C_{ox},\ C_{gd} = C_{gb} \approx 0\right)$$

# MOS Capacitance

## (iii) Parasitic MOS Cap

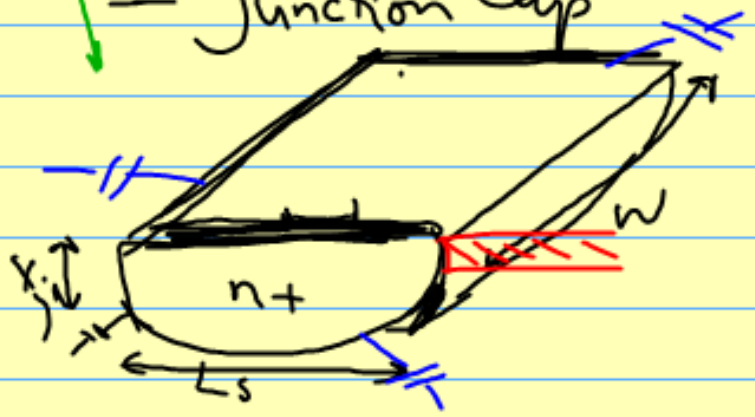



$$C_{gso} = C_{gdo} = W \cdot \underbrace{x_d \cdot C_{ox}}$$

$$= WC_o$$

$C_{if}$, $C_{of}$ : fringe Cap

– Junction Cap




$$C_{bottom} = C_j \cdot W \cdot L_s \quad \xrightarrow{\frac{\varepsilon_{si}}{W_{dep}}}$$

$$C_{sw} = C_{sw}' (2L_s + W)$$

$$= C_{jsw} (2L_s + W)$$