

EE5323 Homework #6

Sequential Logic

YOU DO NOT NEED TO SUBMIT THIS HW

1. For this problem, use the data in the table below.

	Setup time	Clk to Q	D to Q	Contamination delay	Hold time
Register	65ps	50ps	n/a	35ps	30ps
Latches	25ps	50ps	40ps	35ps	30ps

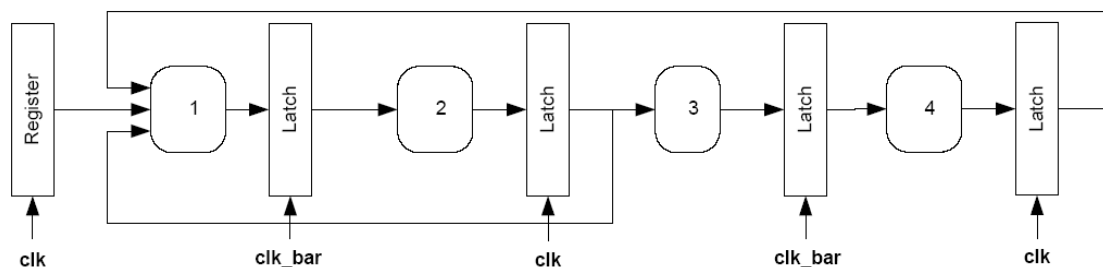
For each of the following sequencing styles, determine the maximum logic propagation delay available within a 500ps clock cycle. Assume there is zero clock skew.

- a. Register
- b. Two-phase transparent latches.

2. Consider a register built from a pair of transparent latches using nonoverlapping clocks. Express the setup time, hold time, and clock-to-Q delay of the register in terms of the latch timing parameters, namely $t_{\text{setup-latch}}$, $t_{\text{c-q-latch}}$ and $t_{\text{hold-latch}}$, as well as $t_{\text{nonoverlap}}$.

3. Determine the minimum clock period at which the circuit below will operate correctly for each of the following logic delays. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay Δ 's.

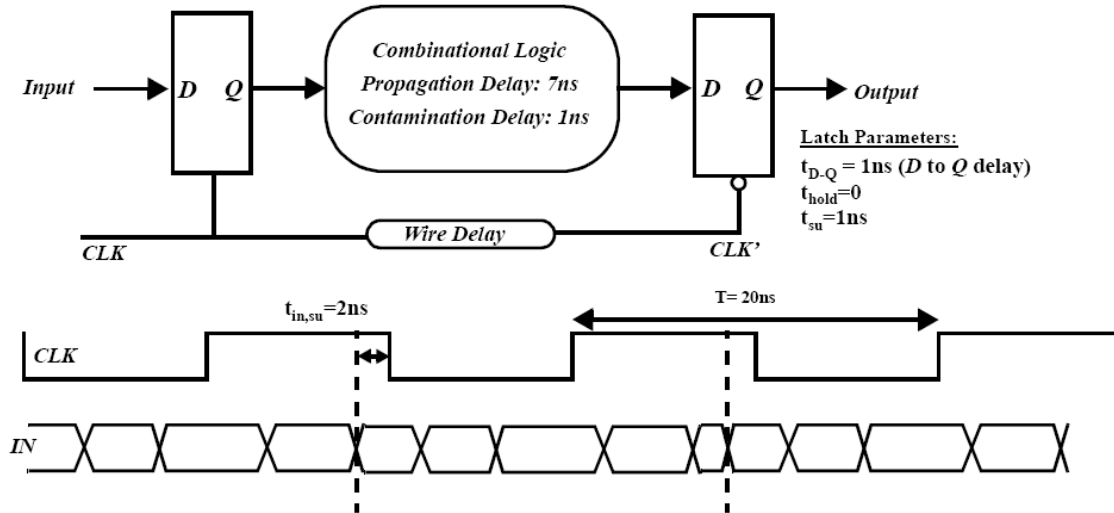
- a. $\Delta_1=300\text{ps}$; $\Delta_2=400\text{ps}$; $\Delta_3=200\text{ps}$; $\Delta_4=350\text{ps}$.
- b. $\Delta_1=300\text{ps}$; $\Delta_2=400\text{ps}$; $\Delta_3=400\text{ps}$; $\Delta_4=550\text{ps}$.
- c. $\Delta_1=300\text{ps}$; $\Delta_2=900\text{ps}$; $\Delta_3=200\text{ps}$; $\Delta_4=350\text{ps}$.
- d. repeat a ~ c if clock skew is 100ps.



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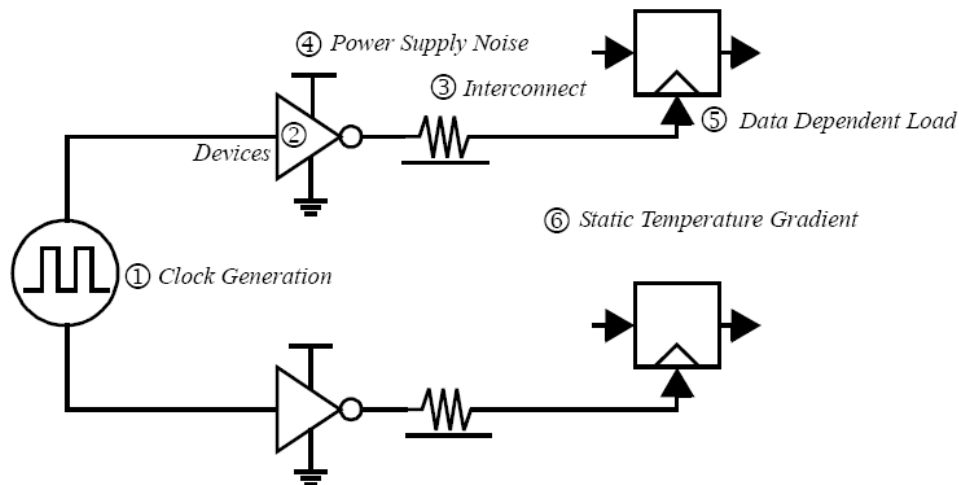
4. Consider the following latch based pipeline circuit shown below.

Assume that the input, IN , is valid (i.e., set up) 2ns before the falling edge of CLK and is held till the falling edge of CLK (there is no guarantee on the value of IN at other times). Determine the maximum *positive* and *negative* skew on CLK' for correct functionality.



5. This problem examines sources of skew and jitter.

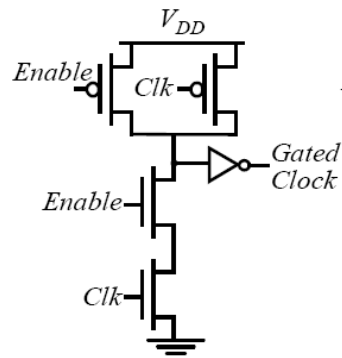
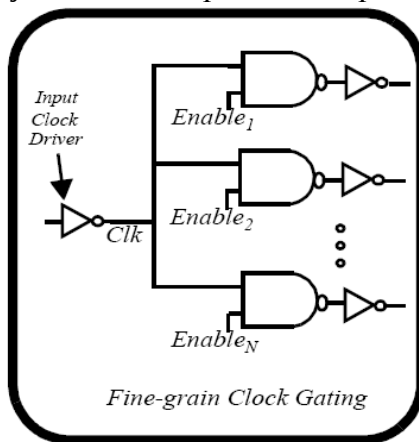
a. A balanced clock distribution scheme is shown below. For each source of variation, identify if it contributes to skew or jitter. Circle your answer in table below.



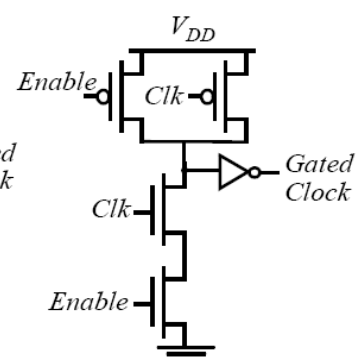
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1) Uncertainty in the clock generation circuit	Skew	Jitter
2) Process variation in devices	Skew	Jitter
3) Interconnect variation	Skew	Jitter
4) Power Supply Noise	Skew	Jitter
5) Data Dependent Load Capacitance	Skew	Jitter
6) Static Temperature Gradient	Skew	Jitter

- b. Consider a Gated Clock implementation where the clock to various logical modules can be individually turned off as shown below (i.e., $Enable_1, \dots, Enable_N$ can take on different values on a cycle by cycle basis). Which approach (A or B) results in lower jitter at the output of the input clock driver? (hint: consider gate capacitance) Explain.



Gating Approach A



Gating Approach B