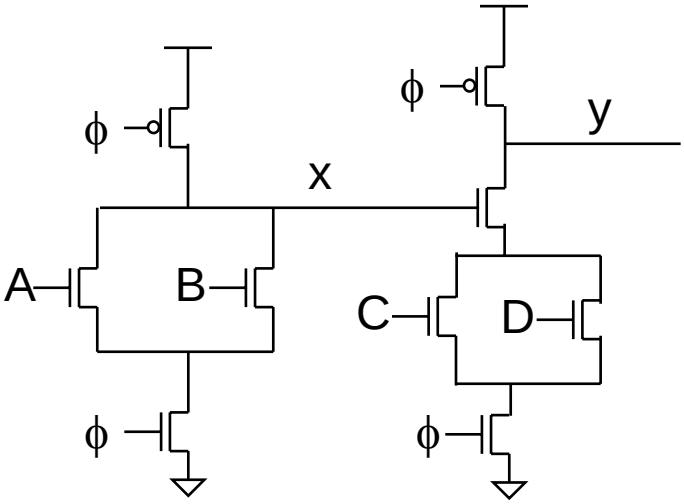
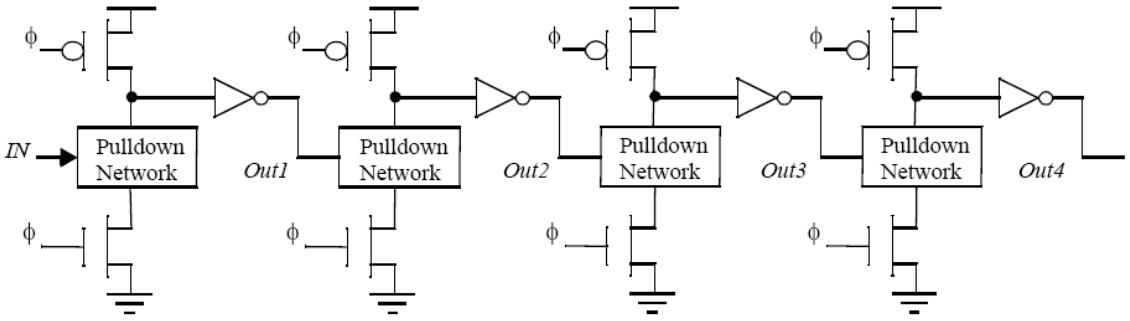
EE5323 Homework #5
Dynamic Circuits
Due by 11/26 in class

1. Consider the circuit below.
a. Give the logic function of *x* and *y* in terms of *A*, *B*, C, and *D*. Sketch the waveforms at *x* and *y* for the given inputs A=1, B=0, C=1, D=1. Do *x* and *y* evaluate to the values you expected from their logic functions? Explain (you may want to double-check your answer using a quick HSPICE simulation).
b. Redesign the gates using *np*-CMOS. Sketch the waveforms at *x* and *y* for your new circuit.



2. Consider a conventional 4-stage Domino logic circuit as shown below in which all precharge and evaluate devices are clocked using a common clock φ. For this entire problem, assume that the pulldown network is simply a single NMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all *T*/2. Assume that the transitions are ideal (zero rise/fall times).



a. Complete the timing diagram for signals *Out1*, *Out2*, *Out3* and *Out4*, when the *IN* signal goes high before the rising edge of the clock φ. Assume that the clock period is 10 T time units.
b. Suppose that there are no evaluate switches at the 3 latter stages. Assume that the clock φ

is initially in the precharge state (φ=0 with all nodes settled to the correct precharge states), and the block enters the evaluate period (φ=1). Is there a problem during the evaluate period, or is there a benefit? Explain.

c. Assume that the clock φ is initially in the evaluate state (φ=1), and the block enters the precharge state (φ = 0). Is there a problem, or is there any benefit, if the last three evaluate switches are removed? Explain.

3. Use HSPICE to plot the gate capacitance per unit area versus Vgs. Show two C-V curves; one for NMOS and another for PMOS. Assume Vds=0 and Vbs=0. Explain how your method works and analyze the C-V curve results.