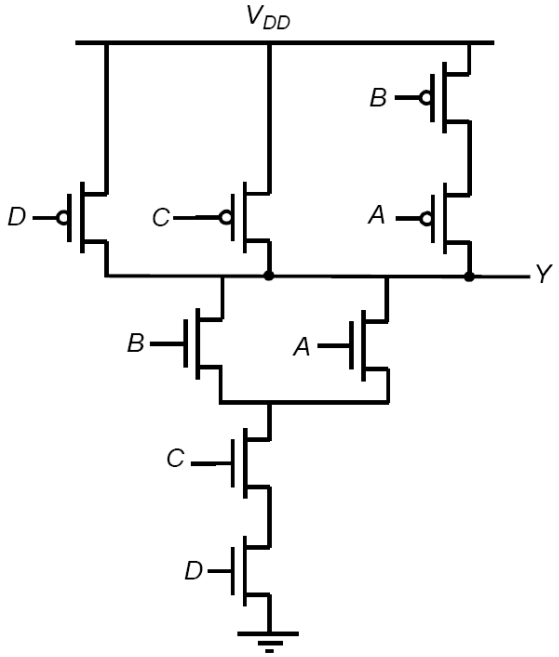
EE5323 Homework #3
Static CMOS Circuits
Due by 10/20/08 in class

1. Consider the circuit below:

a. What is the logic function implemented by the CMOS transistor network? Size the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 4 and PMOS W/L = 8.

b. What are the input patterns that give the worst case t_{pHL} and t_{pLH}. State clearly what are the initial input patterns and which input(s) has to make a transition in order to achieve this maximum propagation delay. Consider the effect of the capacitances at the internal nodes.

c. If P(A=1)=0.5, P(B=1)=0.2, P(C=1)=0.3 and P(D=1)=1, determine the power dissipation in the logic gate. Assume V_{DD}=2.5V, C_{out}=30fF and f_{clk}=250MHz.

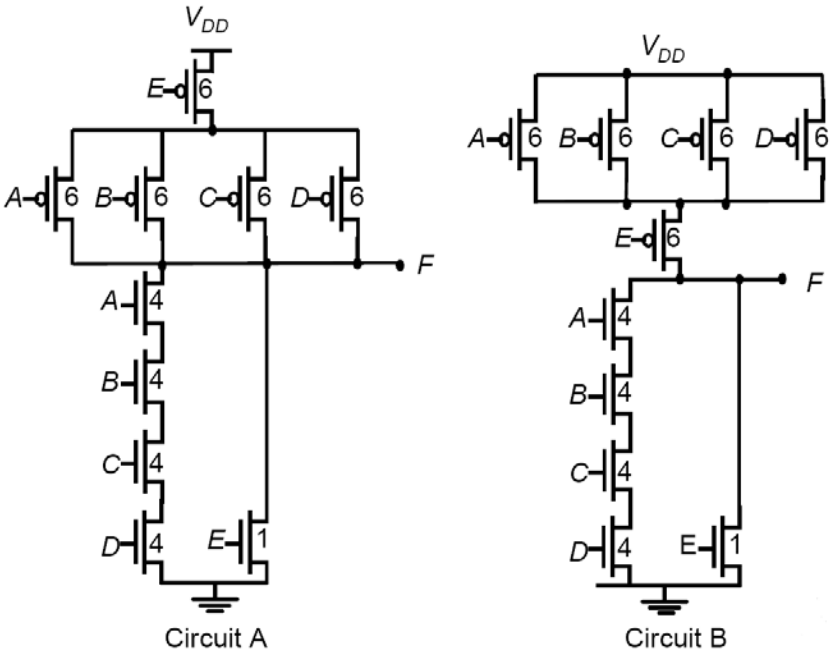


2. Consider the circuit below:

a. Do the following two circuits implement the same logic function? If yes, what is that logic function? If no, give Boolean expressions for both circuits.

b. Will these two circuits' output resistances always be equal to each other?

c. Will these two circuits' rise and fall times always be equal to each other? Why or why not?



3. Consider the circuit as below. Assume the inverter switches ideally at VDD/2, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

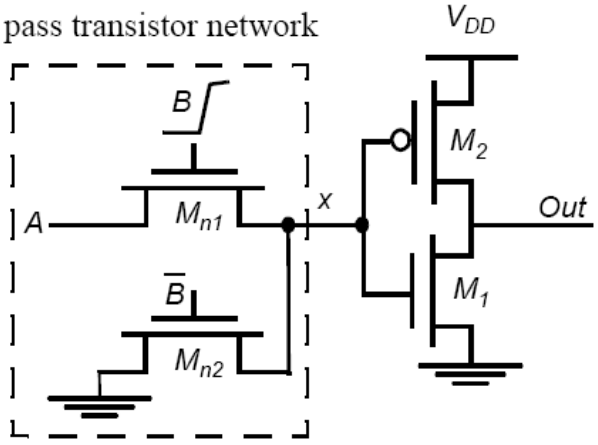
a. What is the logic function performed by this circuit?

b. Explain why this circuit has non-zero static dissipation.

c. Using only just 1 transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.

d. Implement the same circuit using transmission gates.

e. Replace the pass-transistor network in figure with a pass transistor network that computes the following function: x = ABC at the node x. Assume you have the true and complementary versions of the three inputs A, B and C.



$V_{DD} = 2.5V$

$(W/L)_2 = 1.5um/0.25um$

$(W/L)_1 = 0.5um/0.25um$

$(W/L)_{ni} = 0.5um/0.25um$

$k_n' = 115uA/V^2$, $kp' = -30uA/V^2$

$V_{tN} = 0.43V$, $V_{tP} = -0.4V$

4. Consider the circuit below.

a. What is the logic function implemented by this circuit? Assume that all devices (M1-M6) are 0.5μm/0.25μm.

b. Let the drain current for each device (NMOS and PMOS) be 1μA for NMOS at $V_{GS} = V_T$ and PMOS at $V_{SG} = V_T$. What input vectors cause the worst case leakage power for each output value? Explain (state all the vectors, but do not evaluate the leakage). Ignore DIBL**.**

c. Suppose the circuit is active for a fraction of time *d* and idle for *(1-d)*. When the circuit is active, the inputs arrive at 100 MHz and are uniformly distributed ($Pr_{(A=1)} = 0.5$, $Pr_{(B=1)} = 0.5$, $Pr_{(C=1)} = 0.5$) and independent. When the circuit is in the idle mode, the inputs are fixed to one you chose in part (b). What is the duty cycle *d* for which the active power is equal to the leakage power? Use equation $I = I_0 e^{(V_{gs} - V_T)/0.1}$ for leakage calculation. Assume V_T=0.43.