EE5323 Homework #2
The Devices and CMOS Inverter
Due on 10/13 in class (or upload to WebCT)

1. [chap. 3] An NMOS device is plugged into the test configuration shown below in Figure 0.4. The input V_{in} =2V. The current source draws a constant current of 50 μA. R is a variable resistor that can assume values between 10kΩ and 30 kΩ. Transistor M1 experiences short channel effects and has following transistor parameters: k' = 120*10^{-6} V/A^2 **,** V_T = 0.3 , and V_{DSAT} = 0.6V. The transistor has a W/L = 2.5μ/0.25μ. For simplicity body effect and channel length modulation can be neglected. i.e λ=0, γ=0.

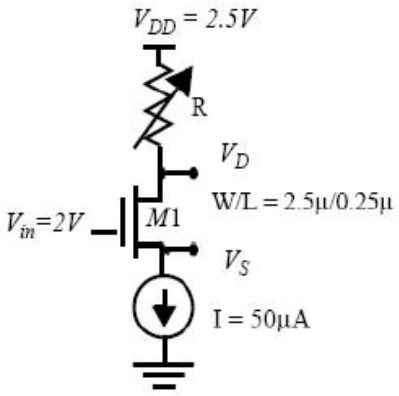

Figure 0.4 Test configuration for the NMOS device.

a. When R =10kΩ find the operation region, V_D and V_S.
b. When R= 30kΩ again determine the operation region V_D, V_S.
c. For the case of R = 10kΩ, would V_S increase or decrease if $\lambda \neq 0$. Explain qualitatively.

2. [chap. 3] Another equation, which models the velocity-saturated drain current of an MOS transistor is given by

$$I_{dsat} = \frac{1}{1 + (V_{GS} - V_t)/(E_{sat}L)} \left(\frac{\mu_0 C_{ox}}{2} \right) \frac{W}{L} (V_{GS} - V_T)^2$$

Using this equation it is possible to see that velocity saturation can be modeled by a MOS device with a source-degeneration resistor (see Figure 0.11).
a. Find the value of R_S such that $I_{DSAT}(V_{GS}, V_{DS})$ for the composite transistor in the figure matches the above velocity-saturated drain current equation. Hint: the voltage drop across R_S is typically small. Channel length modulation can be ignored.
b. Given E_{sat} = 1.5 V/μm and k' = $\mu_0 C_{ox}$ = 20 μA/V2, what value of R_S is required to model velocity saturation. How does this value depend on W and L?

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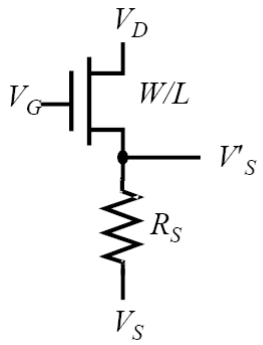
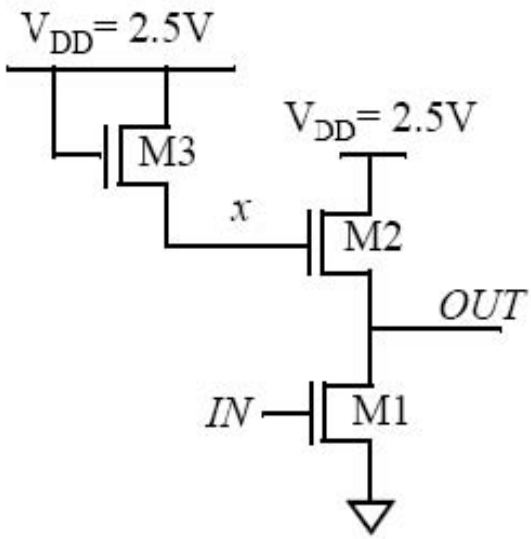


Figure 0.11 Source-degeneration model of velocity saturation.

3. [chap. 5] Consider the following NMOS inverter. Assume that the bulk terminals of all NMOS device are connected to GND. Assume that the input IN has a 0V to 2.5V swing and there is no leakage current. V_{T0}=0.43, Φ_F=0.3.



a. Set up the equation(s) to compute the voltage on node *x*. Assume the body effect coefficient γ=0.5 [$\sqrt{\mathbf{v}}$].
b. What are the modes of operation of device M2? Assume γ=0.
c. What is the value on the output node OUT for the case when IN =0V? Assume γ=0.
d. Assuming devices are in velocity saturation region, V_{DSAT} = 0.63V and γ=0, derive an expression for the switching threshold (VM) of the inverter. Recall that the switching threshold is the point where VIN= VOUT. Assume that the device sizes for M1, M2 and M3 are $(W/L)_1$, $(W/L)_2$, and $(W/L)_3$ respectively. What are the limits on the switching threshold?
For this, consider two cases:
i) $(W/L)_1 >> (W/L)_2$
ii) $(W/L)_2 >> (W/L)_1$

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4. [chap. 5] Sizing a chain of inverters.

a. In order to drive a large capacitance (C_L = 25 pF) from a minimum size gate (with input capacitance C_i = 10fF), you decide to introduce a two-staged buffer as shown in Figure 5.12. Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay. Assume the junction capacitance to gate capacitance ratio γ=1.

b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert? What is the propagation delay in this case?

c. Describe the advantages and disadvantages of the methods shown in (a) and (b).

d. Determine a closed form expression for the power consumption in the circuit. Consider both the gate and junction capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V, an activity factor of 1, and a clock period of *T*?

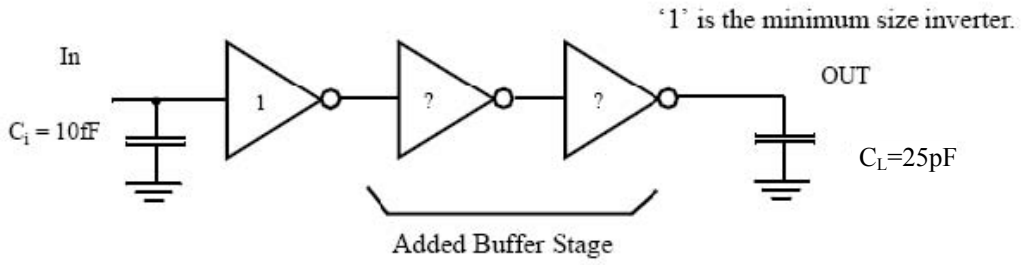

Figure 5.12 Buffer insertion for driving large loads.

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