EE5323 Homework #1
CMOS Inverter Schematic and Layout
Reports due by 09/29

Please go through the cadence tutorial posted on the class website and get familiar with the tools before starting the homework.

[Schematic]

1. Draw schematic of a single CMOS inverter (Vdd=1.1V, 45nm CMOS process, 25°C, minimum channel lengths of 50nm, NMOS width=100nm). Determine the PMOS width for V_M(switching threshold)=Vdd/2.
2. Simulate the high-to-low and low-to-high propagation delay of the designed inverter. Output of the inverter should be loaded with an identical inverter. Input of the inverter should be driven by an identical inverter to obtain a realistic (smooth) input waveform. For the input of the first inverter (driver), use a pulse with a rise/fall time of 0.03ns (tip: use "pwl" or "pulse" command in HSPICE to generate the input waveform).
3. Show how the high-to-low propagation delay changes as you vary the PVT (Process-Voltage-Temperature) parameters as follows. Analyze the results in a few sentences.
   A. Vth = +/- 10% (tip: change the VTH0 parameter in the device model file)
   B. Vdd = 0.9V, 1.0V, 1.1V
   C. Temperature = 0°C, 25°C, 110°C

[Layout]

4. Draw the layout of a single CMOS inverter equivalent to the schematic in part 1. Substrate contacts must be added. Cell height should be fixed as 15μm.
5. Run DRC, LVS, and extract the parasitics. Design violations must be fixed.
6. Simulate the high-to-low and low-to-high propagation delay of the inverter (loaded with and driven by an identical inverter) using the netlist from the extracted view. What is the % delay difference between the schematic and extracted layout?

[Deliverables]

1. Schematic view with transistor dimensions
2. Netlist (spice) file for the schematic
3. Layout view, extracted view
4. Extracted netlist from the layout
5. DRC and LVS reports
6. VTC (Voltage Transfer Characteristics)
7. Waveforms of high-to-low and low-to-high propagation delays from both schematic and post layout simulation. Mention the delay values in the plots.
8. Propagation delay values while varying PVT parameters.