References for EE8331

Ramesh Harjani
Department of Electrical Engineering
University of Minnesota
Minneapolis, Minnesota 55455
Tel: (612) 625-4032, Fax: (612) 625-4583, Email: harjani@ee.umn.edu

1 Low Power / Low Voltage Design

General references for low power applications MOS   [1] [2], [3], [4], [5], [6], [7], [50], [9]

References for minimum power bounds   [10], [64], [?]

General references for low power applications bipolar   [12]

References for weak inversion models   [13], [14]

References for lateral bipolar transistors   [15], [16], [17], [18], [19]

References for low voltage current mirrors   [20], [21], [22], [23], [24], [25], [26], [27]

References for low power amplifiers   [28], [29], [30], [31], [26], [27],

References for class AB amplifiers   [32], [33], [34], [35], [36]

References for dynamic amplifiers   [37], [38]

References for partial positive feedback   [39]

References for low power filter design   [45]

2 Data Converters

References for comparators   [40], [41], [42]

References for low power data converters   [43]

References for sigma delta converters   [53] [88] [89] [90] [91] [92] [93] [94] [95]

Double-sampling in sigma-delta converters   [96] [97] [98] [99] [100]

Pipelined converters   [60] [80] [81] [82] [83] [84] [85]

High-speed opamps   [84] [86] [87] [85] [88] [88] [85]

Wired Communications   [101] [102]

Design examples   [46], [47]

References

[1] R. R. Troutman, "Subthreshold design considerations for insulated gate field-effect transistors," *IEEE Journal of Solid-State Circuits*, vol. sc-9, pp. 55–60, April 1974.

[2] E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. SC-12, pp. 224–231, June 1977.

[3] D. C. Stone, "Analog cmos building blocks for custom and semi-custom applications," *IEEE Journal of Solid-State Circuits*, vol. sc-19, pp. 55–61, February 1984.

[4] E. C. Vittoz, *Micropower Techniques in Design of MOS VLSI Circuits for Telecommunications*, ch. 4. Prentice-Hall, 1985. Editors: Yannis Tsividis and Paolo Antognetti.

[5] E. A. Vittoz, "The design of high-performance analog circuits on digital CMOS chips," *IEEE Journal of Solid-State Circuits*, pp. 657–659, June 1985.

[6] P. R. Gray and R. Castello, *Performance Limitations in SC Filters in Design of MOS VLSI Circuits for Telecommunications*, ch. 10. Englewood Cliffs: Prentice Hall, 1985. Editors: Yannis Tsividis and Paolo Antognetti.

[7] E. A. Vittoz, "Very low power circuit design: Fundamentals and limits," in *IEEE International Symposium on Circuits and Systems*, pp. 1439–1442, 1993.

[8] R. J. V. D. Plassche, W. M. C. Sansen, and J. H. Huijsing, eds., *Analog Circuit Design Low-Power Low-Voltage, Integrated Filters and Smart Power*. Kluwer Academic Publishers, 1994.

[9] S. Sakurai and M. Ismail, *Low-Voltage CMOS Operational Amplifiers Theory, Design and Implementation*. Kluwer Academic Publishers, 1995.

[10] P. Kinget and M. Steyaert, "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits," in *IEEE Custom Integrated Circuits Conference*, 1996.

[11] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welvers, "Matching properties of MOS transistors," *IEEE Journal of Solid-State Circuits*, October 1989.

[12] C. A. Bittmann, G. H. Wilson, R. J. Whittier, and R. K. Waits, "Technology for the design of low-power circuits," *IEEE Journal of Solid-State Circuits*, vol. SC-5, pp. 29–37, February 1970.

[13] T. Grotjohn and B. Hoefflinger, "A parametric short-channel MOS transistor model for subthreshold and strong inversion current," *IEEE Journal of Solid-State Circuits*, vol. sc-19, pp. 100–112, February 1984.

[14] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytic MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83–114, July 1995.

[15] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their application in CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. sc-18, pp. 273–279, June 1983.

[16] M. G. R. Degrauwe, O. N. Leuthold, E. A. Vittoz, H. J. Oguey, and A. Descombes, "CMOS voltage references using lateral bipolar transistors," *IEEE Journal of Solid-State Circuits*, vol. sc-20, pp. 1151–1157, December 1985.

[17] T.-W. Pan and A. A. Abidi, "A 50-db variable gain amplifier using parasitic bipolar transistors in CMOS," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 951–961, August 1989.

[18] J. P. Bardyn and A. Kaiser, "Fully differential operational amplifiers using CMOS compatible lateral bipolar transistors with improved common-mode regulation," *Electronics Letters*, vol. 26, pp. 798–799, June 1990.

[19] H. W. Singor, C. Andre, and C. A. T. Salama, "A high performance CMOS compatible 8-bit current scaling D/A converter," *IEE Proceedings Pt. G*, vol. 137, pp. 169–174, April 1990.

[20] F. Krummenacher, "A high voltage gain CMOS OTA for micropower SC filters," *Electronics Letters*, vol. 17, pp. 160–162, 1981.

[21] J. Babanezhad and R. Gregorian, "A programmable gain/loss circuit," *IEEE Journal of Solid-State Circuits*, vol. SC-23, pp. 1082–1090, 1987.

[22] K. Bult and G. J. G. M. Geelen, "A fast settling CMOS opamp for SC circuits with 90 db gain," *IEEE Journal of Solid-State Circuits*, December 1990.

[23] D. G. Nairn and C. A. T. Salama, "High-resolution current-mode A/D converters using active current mirrors," *Electronics Letters*, vol. 24, pp. 1331–1332, 1988.

[24] R. C. S. et. al, "Ultra low power techniques for focal plane electronic applicatons." JPL Task Plan 80 3295, 1993.

[25] E. Sackinger and W. Guggenbuhl, "A high-swing high-impedance MOS cascode circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 289–298, February 1990.

[26] A. L. Coban and P. E. Allen, "A 1.75v rail-to-rail CMOS op amp," in *IEEE International Symposium on Circuits and Systems*, pp. 497–500, 1994.

[27] P. E. Allen and B. J. B. an Gabriel A. Rincon, "A 1v CMOS opamp using bulk driven MOSFETS," in *IEEE International Solid-State Circuits Conference*, pp. 192–193, 1995.

[28] P. M. V. Peteghem, I. Verbauwhede, and W. M. C. Sansen, "Micropower high-performance SC build ing block for integrated low-level signal processing," *IEEE Journal of Solid-State Circuits*, vol. sc-20, pp. 837–844, August 1985.

[29] R. Hogervorst, R. J. Weigerink, P. A. L. D. Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant-gm rail-to-rail input stage," *Analog Integrated Circuits and Signal Processing*, vol. 5, pp. 135–146, 1994.

[30] J. Huijsing, *Analog Circuit Design.* Kluwer Academic Publishers, 1993.

[31] P. J. Crawley and G. W. Roberts, "Designing operational transconductance amplifiers for low voltage operation," in *IEEE International Symposium on Circuits and Systems*, pp. 1455–1458, 1993.

[32] H. Parzhuber and W. Steinhagen, "An adaptive biasing one-stage CMOS operational amplifier for driving high capacitive loads," *IEEE Journal of Solid-State Circuits*, vol. 26, pp. 1457 – 1460, October 1991.

[33] R. Castello and P. R. Gray, "Performance limitations in switched-capacitor filters," *IEEE Transactions on Circuits and Systems*, vol. CAS-32, pp. 865–876, Septermber 1985.

[34] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. D. Man, "Adaptive biasing CMOS amplifiers," *IEEE Journal of Solid-State Circuits*, vol. sc-17, pp. 522–528, June 1982.

[35] L. G. A. Callewaert and W. M. C. Sansen, "Class AB CMOS amplifiers with high efficiency," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 684–691, June 1990.

[36] P. C. Yu and H.-S. Lee, "A high-swing 2-v CMOS operational amplifier with replica-amp gain enhancement," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 1265–1272, December 1993.

[37] B. J. Hostika, "Dynamic CMOS amplifiers," *IEEE Journal of Solid-State Circuits*, vol. sc-15, pp. 887–894, October 1980.

[38] F. Wang and R. Harjani, "Dynamic amplifiers: Settling, slewing and power issues," in *IEEE International Conference on Circuits and Systems*, 1995.

[39] R. Wang and R. Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs," *Analog Integrated Circuits and Signal Processing*, vol. 8, July 1995. Special issue on low-power design.

[40] Y. S. Yee, L. M. Terman, and L. G. Heller, "1 MV MOS comparator," *IEEE Journal of Solid-State Ciruits*, June 1978.

[41] J.-T. Wu and B. A. Wooley, "A 100-mhz pipelined cmos comparator," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 1379–1385, December 1988.

[42] F. Krummenacher, "Comparator CMOS rapide a faible consommation," rapport d'invention, EPF-Lausanne, 1984.

[43] E. MacRobbie, "Design techniques aimed at 3 volt CMOS delta sigma converters," in *IEEE International Symposium on Circuits and Systems*, pp. 1451–1454, 1993.

[44] J. C. Candy and G. C. Temes, eds., *Oversampling Methods for A/D and D/A Conversion*, pp. 1–25. IEEE Press, 1992.

[45] M. Steyaert, J. Crols, S. Gogaert, and W. M. Sansen, "Low-voltage analog CMOS filter design," in *IEEE International Symposium on Circuits and Systems*, pp. 1447–1450, 1993.

[46] D. Wayne, M. Rives, T. Huynh, D. Preves, and J. Newton, "A single-chip hearing aid with one volt switched-capacitor filters," in *IEEE Custom Integrated Circuits Conference*, pp. 7.5.1 – 7.5.4, 1992.

[47] W. C. Black and D. Stephens, "A small CMOS chip for invasive ultrasound," in *IEEE Custom Integrated Circuit Conference*, pp. 23.5.1 – 23.5.4, 1992.

[48] B. Razavi, *Principles of Data Conversion System Design*. IEEE Press, 1995.

[49] M. J. Demler, *High-Speed Analog-to-Digital Conversion*. Academic Press, 1991.

[50] R. J. V. D. Plassche, W. M. C. Sansen, and J. H. Huijsing, eds., *Analog Circuit Design Low-Power Low-Voltage, Integrated Filters and Smart Power*. Kluwer Academic Publishers, 1994.

[51] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley and Sons, 1997.

[52] S. R. Norsworthy, R. Schreier, and G. C. Temes, eds., *Delta-Sigma Data Converters Theory, Design, and Simulation*. IEEE Press, 1996.

[53] J. C. Candy and G. C. Temes, eds., *Oversampling Methods for A/D and D/A Conversion*, pp. 1–25. IEEE Press, 1992.

[54] P. J. Lim and B. A. Wooley, "A high-speed sample-and-hold technique using a miller hold capacitance," *IEEE Journal of Solid-State Circuits*, vol. sc-26, pp. 643–651, April 1991.

[55] C. Ryan, "Applications of a four-quadrant multiplier," *IEEE Journal of Solid-State Circuits*, vol. sc-5, pp. 45–48, February 1970.

[56] P. Petschacher and et. al., "A 10-b 75-MSPS subranging A/D converter with integrated sample and hold," *IEEE Journal of Solid-State Circuits*, vol. sc-25, pp. 1339–1346, December 1990.

[57] R. Barnett and R. Harjani, "A 200MHz differential sampled-data FIR for disk drive equalization," in *IEEE International Symposium on Circuits and Systems*, 1996.

[58] F. Moraveji, "A high-speed current-multiplexed sample-and-hold amplifier with low hold step," *IEEE Journal of Solid-State Circuits*, vol. sc-26, pp. 1800–1808, December 1991.

[59] P. Real and D. Mercer, "A 14 b linear, 250 nsec sample-and-hold subsystem with self-calibration," in *International Solid-State Circuits Conference*, pp. 164–165, February 1991.

[60] S. H. Lewis and P. R. Gray, "A pipelined 5MHz 9b ADC," *IEEE International Solid-State Circuits Conference*, pp. 210–211, 1987.

[61] Y. M. Lin, B. Kim, and P. R. Gray, "A 13-b 2.5-MHz self-calibrated pipelined A/D converter in 3-um CMOS," *IEEE Journal of Solid-State Circuits*, vol. sc-26, pp. 628–636, April 1991.

[62] S. K. Tewksbury and et. al., "Terminology related to the performance of S/H A/D and D/A circuits," *IEEE Transactions on Circuits and Systems*, vol. CAS-25, pp. 419–426, July 1978.

[63] S. Kuboki and et. al., "Nonlinearity analyisis of resistor string A/D converters," *IEEE Transactions on Circuits and Systems*, vol. CAS-29, pp. 383–389, June 1982.

[64] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welvers, "Matching properties ofMOS transistors," *IEEE Journal of Solid-State Circuits*, October 1989.

[65] T. Miki and et. al., "A 10 bit 50 ms/s CMOS D/A converter with 2.7v power supply," in *VLSI Circuits Symposium*, pp. 92–93, June 1992.

[66] N. Kumazawa and et. al., "An 8-bit 150MHz D/A converter with 2.2v wide range output," in *VLSI Circuits Symposium*, pp. 55–=56, June 1990.

[67] M. J. M. Pelgrom, "A 10-bit 50MHz CMOS D/A converter with 75-ohm buffer," *IEEE Journal of Solid-State Circuits*, vol. sc-25, pp. 1347–1352, December 1990.

[68] H. U. Post and K. Schoppe, "A 14 bit monolithic NMOS D/A converter," *IEEE Journal of Solid-State Circuits*, vol. SC-18, pp. 297–302, June 1983.

[69] A. G. Dingwall and V. Zazzu, "An 8-MHz CMOS subranging 8-bit A/D converter," *IEEE Journal of Solid-State Circuits*, vol. SC-20, pp. 1138–1143, December 1985.

[70] P. Vorenkamp and et. al., "A 1gs/s 10b dital-to-analog converters," in *International Solid-State Circuits Conference*, pp. 52–53, February 1994.

[71] W. T. Sagun and et. al, "A 125-mhz 12-bit digital-to-analog converter," *Hewlett-Packard Journal*, pp. 78–85, April 1988.

[72] P. Holloway and M. Norton, "A high yield, second generation 10-bit monolithic DAC," in *International Solid-State Circuits Conference*, pp. 106–107, February 1976.

[73] H. T. an M. Yokoyama, "A 10-bit 80 MHz glitchless CMOS D/A converter," in *Custom Integrated Circuits Conference*, pp. 26.5.1–26.5.3, May 1991.

[74] J. Colles, "TTL to CMOS voltage level translator." patent no. 4,794,282 granted December 27, 1988.

[75] H. J. Schouwenaars, D. W. J. Groeneveld, and H. A. H. Termeer, "A low-power stereo 16-bit CMOS D/A converter for digital audio," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 1290–1297, December 1988.

[76] B. Peetz, B. D. Hamilton, and J. Kang, "An 8-bit 250 megasample per second analog-to-digital converter: Operation without a sample and hold," *IEEE Journal of Solid-State Circuits*, vol. 21, pp. 997–1002, December 1986.

[77] Y. Gendai, Y. Komatsu, S. Hirase, and M. Kawata, "An 8-b 500mhz ADC," in *IEEE International Solid-State Circuits Conference*, (San Franscisco), pp. 172–173, February 1991.

[78] J. Doernbergh, P. R. Gray, and D. A. Hodges, "A 10-bit 5-msample/s CMOS two-step flash ADC," *IEEE Journal of Solid-State Circuits*, vol. sc-24, pp. 241–249, April 1989.

[79] R. K. Hester and et. al., "Fully differential ADC with rail-to-rail common mode range and nonlinear capacitor compensation," *IEEE Journal of Solid-State Circuits*, vol. SC-25, pp. 173–183, February 1990.

[80] S. Sutarja and P. R. Gray, "A pipelined 13-bit, 250-ks/s, 5-v analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 1316–1323, December 1988.

[81] S. Masuda, Y. Kitamura, S. Ohya, and M. Kikuchi, "A CMOS pipelined algorithmic A/D converter," *IEEE Custom Integrated Circuits Conference*, pp. 559–562, 1984.

[82] G. C. Temes, F.-J. Wang, and K. Watanabe, "Novel pipeline data converters," *International Symposium on Circuits and Systems*, pp. 1943–1946, 1988.

[83] K. Nakamura, M. Hotta, R. Carley, and D. Allstot, "A 85-mw, 10-bit 40-ms/s ADC with decimated parallel architecture," in *IEEE Custom Integrated Circuits Conference*, pp. 495–498, 1994.

[84] K. Nakamura, M. Hotta, L. R. Carley, and D. J. Allstot, "An 85 mw, 10 b, 40 msample/s CMOS parallel-pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 173–183, March 1995.

[85] W.-C. Song, H.-W. Choe, S.-U. Kwak, and B.-S. Song, "A 10-b 20-msamples/s low-power CMOS ADC," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 514–521, May 1995.

[86] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, pp. 629–633, December 1983.

[87] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE Journal of Solid-State Circuits*, vol. 19, pp. 919–925, December 1984.

[88] S. Rabii and B. A. Wooley, "A 1.8-v digital-audio sigma-delta modulator in 0.8-um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 783–796, June 1997.

[89] G. Yin, G. Stubbe, and W. Sansen, "A 16-b 320khz CMOS A/D converter using two-stage third-order sigma-delta noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 640–647, June 1993.

[90] I. Fujimori, K. Koyama, D. Trager, F. Tam, and L. Longo, "A 5-v single-chip delta-sigma audio A/D converter with 111 db dyanamic range," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 329–336, March 1997.

[91] T. Blalack and B. A. Wooley, "The effects of switching noise on an oversampling A/D converter," in *International Solid-State Circuits Conference*, pp. 200–201, 1995.

[92] A. Hairapetian and G. C. Temes, "A dual-quantization mult-bit sigma delta analog/digital converter," in *IEEE International Symposium on Circuits and Systems*, pp. 437–440, 1994.

[93] G. Yin and W. Sansen, "A high-frequency and high-resolution fourth-order sigma-delta A/D converter in BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 857–865, August 1994.

[94] M. Rebeschini, N. R. V. Bavel, P. Rakers, R. Greend, J. Caldwell, and J. R. Haug, "A 16-b 160khz CMOS A/D converter using sigma-delta modulation," *IEEE Journal of Solid-State Circuits*, vol. 25, pp. 431–490, April 1990.

[95] A. Marques, V. Peluso, and M. S. an W. Sansen, "Optimal parameter s for cascasde sigma-delta modulators," in *IEEE International Symposium on Circuits and Systems*, pp. 61–64, 1997.

[96] H.-K. Yang and E. I. El-Masry, "Double sampling delta-sigma modulators," *IEEE Journal of Solid-State Circuits*, vol. 43, pp. 524–529, July 1996.

[97] P. J. Hurst and W. J. McIntyre, "Double sampling in switched-capacitor delta-sigma A/D converters," in *IEEE International Symposium on Circuits and Systems*, pp. 902–905, 1990.

[98] T. V. Burmas, K. C. Dyer, P. J. Hurst, and S. H. Lewis, "A second-order double-sampled delta-sigma modulator using additive-error switching," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 284–293, March 1996.

[99] C. K. Thanh, S. H. Lewis, and P. J. Hurst, "A second-order double-sampled delta-sigma modulator usign individual-level averaging," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1269–1273, August 1997.

[100] D. Senderowicz, G. N. an Sergio Permici, A. Nagari, P. Confalonieri, and C. Dallavalle, "Low-voltage double-sampled sigma-delta converters," in *International Solid-State Circuits Conference*, pp. 210–211, 1997.

[101] D. A. Johns and D. Essig, "Integrated circuits for data transmission over twisted-pair channels," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 398–406, March 1997.

[102] D. D. Harman, G. Huang, G.-H. Im, M.-H. Nguyen, J.-J. Werner, and M. K. Wong, "Local distribution of IMTV," *IEEE Multimedia*, pp. 14–23, 1995.