EE8331: Advanced Analog Integrated Circuit Design

Design Project

Important Dates: final project report due date: **Friday, May 5th**
interim project report due date: **March 24th**
project proposal due date: **Friday, Feb 11th**

A major portion of your grade in this course will come from your final project. Each design project needs to concentrate on some aspect of low power design or data converters or PLLs. Make sure you speak to me about your project ideas real early in class. The most important aspect of the project is to show some originality in the idea, in the approach, and/or in the analysis. Projects need to be individual efforts.

The project will consist of the following:

1) A short (2-4 page) proposal describing what you want to do in the project. Please provide relevant references. In addition, this paper should include a description of how you intend to approach the remainder of the project.
2) An interim project report letting me know what progress you have made. I am looking for about 10 pages. Most of the material in this report should be able to be reused in the final report as well.
3) A final written report describing the project and its results. This report should be written in the style of a journal/conference paper. This paper should include a background section with an extensive survey of previous work in related fields. You need to show me that you have adequately researched the relevant literature and understand the basic problems in your proposed topic area. It should be written in the style of a tutorial paper.

Students are expected to know and use HSPICE, Switcap, and Matlab or equivalent circuit and switched capacitor simulators, for design problems. It is also recommended that students use MathCad / Theorist / Maple / Mathematica or equivalent numerical and symbolic computer program to work on homework and design problems.

Some project ideas:

1) Compare the minimum power bounds for sigma-delta converters and Nyquist rate converters. In particular, it may be sufficient to consider only a few Nyquist rate converters, i.e. charge redistribution and algorithmic.
2) Design a N bit pipelined converter with digital error correction. The value of N will depend on complexity of the correction algorithms used.
3) Design a N bit folding analog-to-digital converter . The value of N will depend on complexity of the design developed.
4) Develop an exact analysis for the minimum power consumption for a pipelined converter with different number of bits per stage.
5) Design a 50MHz 14bit bit A/D using a FRC topology.
6) Design an extremely fast sample-and-hold with 95db+ SFDR.