

EE8331: Advanced Analog Circuit Design Techniques

Midterm II:

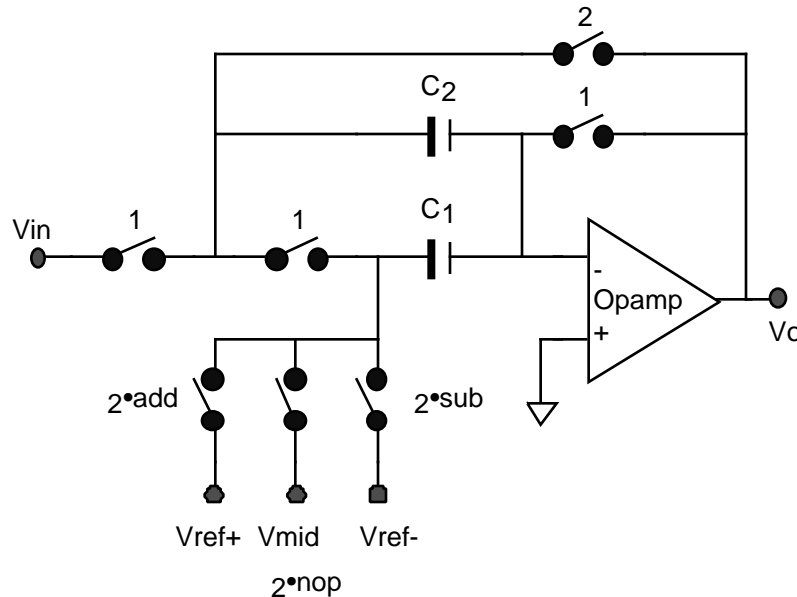
Take Home: Due before class 9am on Monday, May 1st

Open books, open notes

1. This is a design problem. You are expected to use matlab/simulink/spice and hand analysis to develop your design. Develop the design for a 12 bit pipelined converter. You will design the complete converter assuming that you will eventually have all twelve bits. However, for your spice simulations I want you to implement two complete stages. Develop your design with 1.5bit stages that use digital error correction. Use all the references given to you in class.

a) Given a power supply of ± 1.25 Volts and a maximum signal swing of ± 1.0 Volts calculate the SNR in dB assuming that the thermal noise is equal to $1/2$ LSB for the full-scale sinewave input. (10 points)

b) Using this SNR (i.e., again assuming that the thermal noise is $1/2$ LSB) and knowledge of the signal swing to calculate the smallest input capacitor size given that you are using a **fully differential circuit**. Don't forget that you are sampling more than one capacitor. Assume you are using the method that uses two identical capacitors to sample the input and obtain a gain of two. The circuit below shows a single-ended version of the circuit. (10 points)



c) Now calculate the capacitor size given that a 0.2pF capacitor matches to 0.1% and capacitor matching is proportional to the square root of the capacitor size. Assume that a 1 sigma design gives less than 1 LSB error. Hint: if your capacitor size is less than 0.1pF and more than 25pF you are doing something wrong for both part b and c. (10 points)

d) Use the bigger of the two capacitors from part a and part b. Assume that you are supplied with a single-ended clock with a frequency of 200kHz . Calculate the minimum number of time constants required if the opamp never slews. Using nand gates and inverters design the non-overlap clock generator. Use the parameters from the TSMC 0.25μ CMOS process given on

the mosis website (www.mosis.com).(10 points)

e) Now design a symmetrical opamp to meet the speed and settling specifications. This time as you note the ΔV for the diff pair is finite and you have slewing. Design your opamp to have a ΔV of 0.5 volts. For a 12 bit converter the minimum gain for the first stage of the pipelined converter is $20 \cdot \log(2^{13})$. For this reason you **may** have to cascode. If you do use the low voltage cascode design. Hint: Does this circuit accomplish gain squaring? Don't forget you have to drive the input of the next stage as well. For simplicity use the same capacitor size for the next stage as well. In practice the capacitor of the next stage can be made smaller from both a noise and matching perspective. (50 points)

f) Now develop a scheme to develop the plus and minus voltage references, and thresholds for your comparators from your power supply. You need to minimize power dissipation. Recall you have to charge capacitors from this reference so, calculate the settling time and use this to guide your choices. (50 points)

g) Now design the comparator using the circuit shown in class and your homework. You do not need to use the shield transistors. Just pull up and pull down. Use the correct clock phases for your circuit. (50 points)

h) Complete the design for a single stage of the converter and simulate two conversion clock period for a differential input of +0.7Volts. (25 points)

i) Now put two of these stages back to back and simulate them. Make sure both circuits work well. Also check that the digital error correction logic works. Use the sheets on the following pages for help. You do not need to implement the digital logic. However, you need to verify its operation. (50 points)