EE8331: Advanced Analog Integrated Circuit Design

HW #4
Due Monday 04/24/00

1) Develop a matlab/simulink model for a 4 stage, 1.5 bit per stage pipelined converter with digital error correction. Let the voltage range be +-0.5V and the Vref be equal to +-0.25V. Let the sample rate for this converter be 10Ms/s. Suggestion: simulink models are much easier

a) Draw the input-output transfer function for this converter. Let the +ve comparator in stage 2 have a +0.131 voltage offset. Plot the new input-output transfer function.

b) Let the 3rd stage D/A have an error. Let it subtract 0.4 instead of 0.25. Draw the input output transfer function.

c) For a 1MHz full scale input plot and calculate the SFDR for the error in (b)