A 100MS/s 9-bit Companding SAR ADC with On-Chip Input Driver in 65nm CMOS for Multi-Carrier Communications

Anindya Saha, Saurabh Chaubey and Ramesh Harjani
Department of Electrical & Computer Engineering, University of Minnesota, Minneapolis, MN 55455, USA

***Abstract*—This paper presents a 100MS/s 9b companding SAR ADC which exploits the statistical properties of broadband multi-carrier signals to reduce the dynamic range requirement for the ADC. The architecture emulates the performance of a higher resolution ADC by reducing the PAPR of a multi-carrier signal to that of a single carrier. Additionally, gain-before-sampling results in reduced sampling capacitor size which lowers power and area. To verify the concept, a prototype implemented in TSMC's 65nm GP CMOS process consumes 12.27 mW at 100 MS/s while extending the dynamic range of the sub-ADC by 13 dB, and resulting in a Schreier FOM of 150.7 dB.**

I. Introduction

The launch of LTE/LTE-A networks has accelerated the transition from voice-centric to data-centric communications, causing an exponential increase in mobile broadband data consumption. Multi-carrier modulation techniques such as OFDM are rapidly becoming the defacto standard for wireless communications as they are spectrally efficient and tolerant to multipath propagation effects. However, one significant limitation of OFDM is the high peak-to-average-power ratio (PAPR), resulting in a Gaussian distributed PDF of the data values. A waveform with a high PAPR not only requires the PA to have a finite backoff on the TX end but also adds directly to the required dynamic range (DR) of the ADC on the RX end [1]. For N sub-carriers, the PAPR of an OFDM waveform is $2 \times ln(N)$ when N is large [2]. PAPR for many multi-carrier standards (e.g. 802.22, LTE-A, DVB-T) vary up to ~13 dB, with the bandwidth extending up to 100 MHz [1], [2]. Accommodating large peaks in a multi-carrier signal results in inefficient ADC operation, since increasing the SNDR by 6 dB requires a 2x increase in the power, which increases to 4x for thermal noise limited ADCs (SNDR>75 dB) [3].

This paper presents an ADC targeted for broadband multi-carrier systems which exploits the signal statistics by providing amplitude-specific gain in a *sample-by-sample* basis with a fast instantaneous AGC (i-AGC), reducing the effects of PAPR to that of a single-carrier, and optimizing quantization noise (QN) after the companding gain correction. As we are able to provide different gains for different signal levels, we need to maintain a much lower ADC SNR. Additionally, gain before sampling allows us to scale the sampling capacitor (C_{samp}) of all the paths; resulting in a power and area reduction. Conceptually, the idea is similar to a companding signal-processor which utilizes internally non-linear and/or time variant systems to process externally linear, time invariant signals [4]. We employ a 'compander' which amplifies the smaller signals (i.e., expansion) in a binary piecewise linear fashion for easier digital compression after the ADC.

Fig. 1: PDF of a single-carrier (bathtub) and multi-carrier signals (Gaussian).

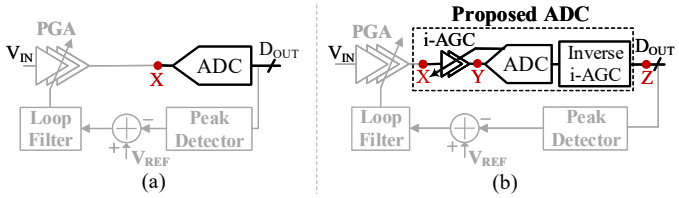

Fig. 2: Block diagram of (a) conventional (b) proposed ADC in a typical receiver chain with PGA. The PGA time constants are slow (~kHz range).

II. System Architecture

Fig. 1 compares the PDF of a single carrier and a multi-carrier signal. Unlike the bathtub distributed single carrier, where majority of the samples are large, the PDF of a multi-carrier signal has a Gaussian distribution, where large values occur rarely. The Gaussian shape becomes more prominent if a wideband blocker is present at the adjacent channel. A companding ADC is the most efficient way to quantize the frequently occurring smaller samples. Fig. 2(a) and (b) compares the proposed ADC with a conventional ADC in a typical RX chain, each is preceded by a programmable gain amplifier (PGA). The PGA responds to the average signal strength and is conventionally slow (hundreds of kHz to a few MHz) so as to retain the amplitude modulation information and is impractical for a fast changing OFDM signal [5]. In the

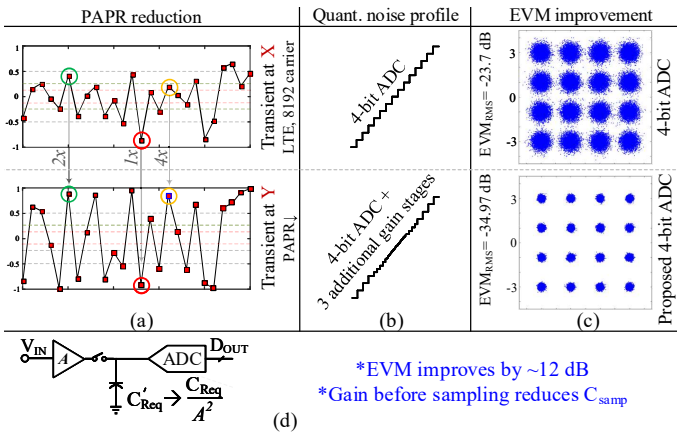

Fig. 3: (a) PAPR reduction at Y (refer to Fig. 2) (b) quantization noise reduction after digital compression (c) EVM improvement (d) C_{samp} reduction.

978-1-5386-7392-8/18/$31.00 ©2018 IEEE

proposed ADC, we use an i-AGC scheme to provide gain in a sample-by-sample basis to increase the instantaneous SNR.

Fig. 3(a) compares multiple samples of an OFDM signal at the input of a conventional and the proposed 4b ADC for illustration purposes. The PAPR at the input of the proposed ADC becomes comparable to that of the single carrier due to the i-AGC, reducing the DR requirement for the ADC. Fig. 3(b) and (c) compare the QN profile and output EVMs of a conventional and the proposed 4b ADC with 3 additional parallel gain stages (2x, 4x, 8x) as part of the i-AGC. The proposed ADC optimizes the quantization level depending on the signal amplitude. Here, the reduction in the PAPR and the associated reduction in quantization noise improves the EVM by ∼12 dB (depending on the input signal statistics). We select 3 additional binary stages since it can reduce the combined effect of the increased PAPR in most standards (∼13 dB) and fast transient effects (∼3-4 dB) [6]. Adding additional paths results in only a small reduction in the PAPR. Fig. 3(d) demonstrates that providing gain before sampling allows C_{samp} to be scaled by a factor of the gain squared, i.e., 64 in this example, reducing the required driver power.

To verify the concept, we investigate the design technique of a 9b ADC using the proposed method. We use a SAR process, which is popular due to its low-power operation. In a moderate/high-resolution SAR ADC, C_{samp} is on the order of hundreds of fF to a few pF, which requires significant driver power (typically more than the ADC) to reach the required accuracy in a short window [3], [7]. A conventional SAR ADC having $C_{samp} = C$ and preceded by a driver of gain 1x converts a multi-carrier signal with large PAPR inefficiently, since we are spending the same amount of energy to quantize large but rarely appearing values that have little impact on the BER performance. In the proposed architecture (Fig. 4(a)), the 9b SAR ADC is preceded by 3 additional drivers (along with 1x), sampling the signal in parallel with different $radix$-2 gains (2x, 4x & 8x) for easier digital compression. Fig. 4(a) also shows the signal PDF at various points of the circuit (X, Y, Z). We note that the PAPR reduces from ∼13dB at point X to ∼3dB at point Y. Fig. 4(b) shows the timing diagram for the operation. We use the same ADC for both gain selection and conversion, which reduces mismatch effects but adds a few additional cycles, depending on the number/gain of drivers. First, the signal is sampled in all the parallel paths. The ADC uses the sampled value in the 1x path to determine the path with the highest gain that is not saturated. During the gain selection, the sampled values are not lost since C_{samp} and C_{DAC} are separated using current domain subtraction, which is slightly different from a traditional charge-redistribution SAR converter [8]. After gain selection, the ADC proceeds with the conversion and digital compression using the selected path. The drivers can be re-used in a time interleaved process after recovering from saturation.

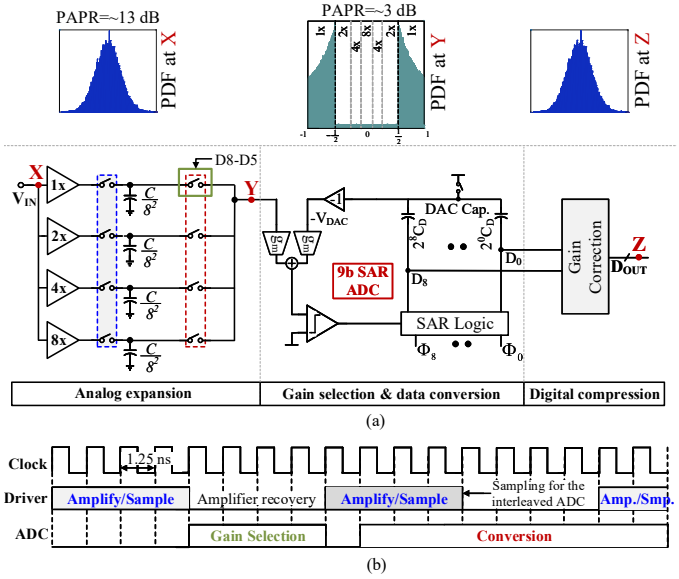

Fig. 4: (a) Proposed 9b ADC with 3 additional gain stages with scaled C_{samp}. The PDF of the signal at various points are shown. (b) Timing diagram.

Effect on PAPR: i-AGC shifts the average of the PDF from the center towards the peaks (point Y at Fig. 4(a)), reducing the PAPR. The 1x region (usually contains a few samples) at Y has contributions from all the regions now, resembling a bathtub distribution. For 8192 sub-carrier, 46% of the symbols use the 8x path, 32% use the 4x, 21% use the 2x and ∼1% use the 1x path (simulated with 2^{22} 64QAM OFDM symbols).

Effect on Quantization & Thermal Noise: The i-AGC requires a digital block which divides the ADC output by the corresponding gain for digital compression. This reduces the quantization noise, emulating a higher resolution ADC. Samples with a gain of 8 $(= 2^3)$ will have the effective QN of a (9+3)-bit ADC after digital compression. Gain before sampling allows C_{samp} of 8x path to be reduced by $\frac{1}{64}$x without increasing the thermal noise, see (1). Likewise, larger signals (in 1x-4x path) can be sampled by a even smaller capacitor than that dictated by their gain because the signal has sufficient SNR for a reasonable BER. Refer to Fig. 4(a), even after scaling C_{samp} for all paths by $\frac{1}{64}$x, the 1x path (which now contributes a thermal noise equivalent to a 9b ADC) has sufficient SNR since the larger samples of the modulated signal requires only a finite SNR for demodulation [6].

$$SNR = \frac{A^2/2}{kT/C_1} = \frac{(8.A)^2/2}{kT/C_2/8^2} \Longrightarrow C_2 \longrightarrow \frac{C_1}{8^2} = \frac{C_1}{64} \qquad (1)$$

Power Reduction: Here, we consider the power savings in the driver and ADC separately.

Driver power: Increasing the SNDR by 6dB requires a 4x increase in C_{samp} (see (1)) and in the driver power, since $P_{Driver} \propto C_{samp}$ for same GBW [9]. Recall, we get a ∼12dB (2b of effective resolution) increase in EVM from the proposed ADC. If a 12b ADC requires $C_{samp} = C$, it follows that an 11b ADC will require a $C_{samp} = \frac{C}{4}$. The proposed 9b ADC with 4 parallel paths requires $4 \times \frac{C}{64} = \frac{C}{16}$ for a 12 dB increase (equivalent 11b), reducing equivalent driver power by 4x.

ADC power: Increasing the SNDR by 6dB requires a 2x increase in the ADC power (4x if SNDR>75 dB). For the proposed 9b ADC, we use 3 additional gain paths, increasing

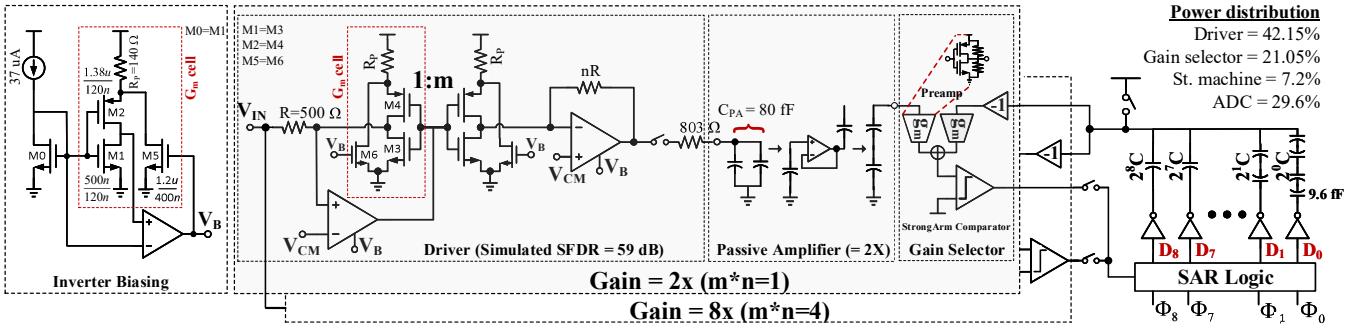

Fig. 5: Single-ended circuit implementation of the proposed differential prototype. For simplicity, time interleaving has not been shown.

the effective resolution by 2-bit while using the same lower resolution ADC. The ADC power increases by the amount required for running the extra clock cycles (4 cycles for selection, 9 for conversion, increasing the time by 1.44x ($\frac{9+4}{9} = 1.44$). This results in a potential 2.78x ($\frac{4}{1.44} = 2.78$) reduction in the ADC power.

III. Circuit Implementation

The circuit architecture is shown in Fig. 5 (refer to Fig. 4(a) for clarity). Compared to a switched-capacitor compander, it requires less power due to inverter based feedback, and less driving power due to resistive input [4], [8]. For simplicity, We implemented only 1x & 4x path using 3 clock cycles for gain selection, where the samples with a gain of 4 ($= 2^2$) will have the effective QN of a 11b (= 9+2) ADC. The gain paths are followed by a passive amplifier of gain 2x. Note, passive gain does not scale C_{samp} since the signal is already sampled. A 9b SAR ADC, which also works as the gain selector, follows the passive amplifier. A 2x time interleaving has been used to double the speed, where the drivers are reused. Radix-2 digital compression along with calibration are done off-chip.

Driver Amplifier: An ADC driver which relaxes the gain and UGB requirements of the feedback loop has been used for implementing the gain paths [8]. Both the current mirror and amplifier are designed using inverters to benefit from its higher g_m/I_d efficiency and linear operating range. The inverters are biased with a constant current for low PVT variations [8]. Driver output swing is limited to $0.5V_{DD}$ for better linearity and becomes full scale with the help of a passive amplifier. When idle, drivers are turned off to save power.

Passive Amplifier: Passive amplification achieves a highly linear full-scale output while introducing less noise compared to its active counterpart. However, the parasitic bottom plate capacitance (C_{par}) causes gain error and its impact is larger for higher gains. In this design, we use a dynamic amplifier to only charge the parasitics, which eliminates the gain error while consuming minimum power. Fig. 6 shows the details of the implementation. In ϕ_1, the capacitors are charged by the input driver. The dynamic amplifier charges the bottom plate parasitics C_{par} in ϕ_2, during which time the bias current of the amplifier changes dramatically and eventually goes to zero [10]. During ϕ_3, the amplifier is detached and the capacitors are stacked for a parasitic insensitive 2x gain.

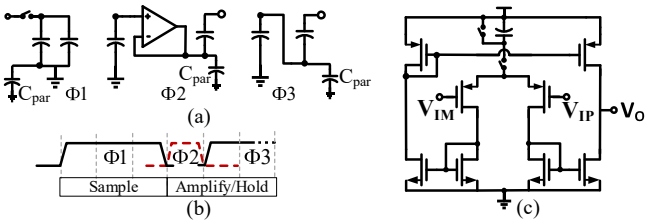

Fig. 6: (a) Passive amplifier (b) Timing diagram (c) Dynamic amplifier.

SAR ADC: In the 9-bit SAR ADC, C_{samp} and the binary weighted DAC capacitor is separated by performing the input and DAC reference subtraction in the current domain rather than charge domain [8].

IV. Measurement Results

The proposed ADC, fabricated in TSMC's 65nm GP process, occupies an active area of $0.163mm^2$ (Fig. 7(a)). It consumes 12.27 mW at 100 MS/s including the buffer and driver power of the SAR ADC. In this conservative design, C_{samp} (= 80 fF instead of an ideal 327 fF required for 11b, where $V_{FS} = 0.8V$) is scaled by only a 4x factor instead of 16x, as could have been scaled for a maximum gain of 4x (refer to Fig. 4(a)), due to concerns about parasitics and preamp C_{in} variation. Also, we used multiple comparators to avoid switching in the signal path. Power can be further reduced by using an auto-zero comparator (i.e., smaller devices, less C_{in} variation) and using bootstrapped switches in the signal path.

Fig. 7(b) and 7(c) show the single and TI sub-ADC spectrum for the Nyquist full-scale input. The single-ADC achieves 6.92 ENOB with an SFDR of 50 dB without any post processing, while the TI-ADC achieves 6.59 ENOB with an SFDR of 51 dB after gain/offset calibration. Measured DNL and INL is 0.69/-0.71 LSB and 1.96/-2.2 LSB. Fig. 8 shows the effective DR (EDR), SFDR, $|HD2|$ and $|HD3|$ for the sub-ADC as a function of frequency for a full-scale single-sinusoid. The measured EDR at Nyqist is 54.6 dB which is 13 dB better than the sub-ADC. The SFDR is limited by either HD2 or HD3 which is likely a by-product of the pseudo-differential front-end driver stages. Fig. 9 shows the SNDR vs input power for a single-carrier signal. Unless it is saturated, we always choose the 4x path, which reduces the quantization noise after gain correction. For large signals, profile follows the gain = 1 path.

A signal composed of 100 equal power QPSK-modulated carriers (30kHz BW, 50kHz spacing, PAPR=12 dB) in the

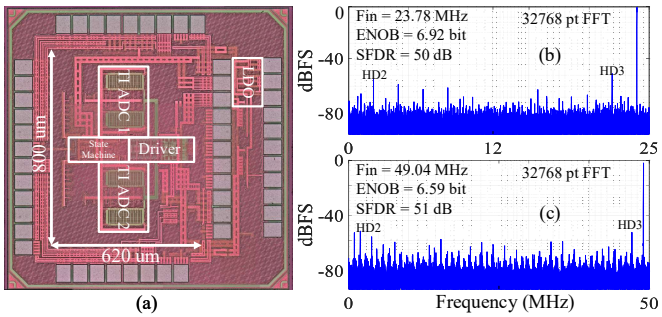

Fig. 7: (a) Die photo (b) Measured frequency spectrum of sub-ADC (single) (c) Measured frequency spectrum of sub-ADC (time-interleaved) at Nyquist.

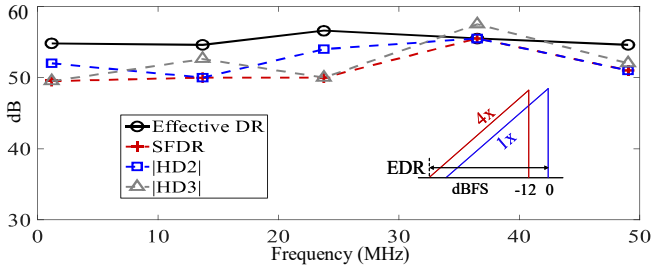

Fig. 8: Measured Performance of the ADC and sub-ADC vs input frequency.

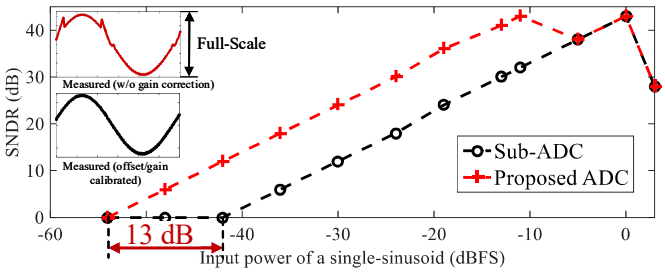

Fig. 9: Measured SNDR vs input power for a single-carrier signal.

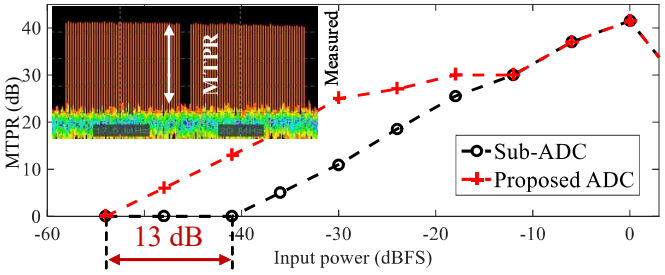

Fig. 10: Measured MTPR vs input power for a multi-carrier signal.

first Nyquist band was used to test the ADC in a multi-carrier environment. Fig. 10 shows the measured multi-tone power ratio (MTPR) vs the input power. Achieved EDR is improved by 13 dB compared to the sub-ADC. The reduced MTPR at higher powers is due to the signal PAPR of 12 dB.

The estimated power in 65nm for digital compression and gain/offset calibration (one adder and one multiplier with a word length of 9b, and registers to store the coefficients) is approximately 187.5 uW from an 1V supply at 100MS/s for an average fanout of 3. Table I summarizes and compares the design with state-of-the-art ADCs with similar concept/performance. [11] uses a similar concept but requires ∼5.4x more area and ∼3x more power for similar speed. Reference [7], [12] and [13] all include on-chip driver power. While [7] and [13] capitalizes on smaller feature sizes and more optimized traditional architectures, our design, designed in a GP process for ease of integration, achieves a better FOM than [11] and [12].

V. Conclusions

In this paper, a prototype companding SAR ADC based on exploiting the statistical properties of multi-carrier signals is demonstrated in 65nm CMOS. By using a gain-before-sample technique, we have been able to get a 13 dB improvement in the effective DR over the sub-ADC by reducing the PAPR of a multi-carrier signal to approximate that of a single carrier (∼3 dB), and by optimizing quantization noise. We also reduced the required power and area compared to conventional designs by scaling the sampling capacitor. Our prototype design was a little conservative in sizing the capacitors and included redundancy for failsafe operation. However, revised designs have the potential for increased power savings and the savings can be even larger for thermal noise limited ADCs, which require 4x additional power for every 6 dB increase in SNDR.

Acknowledgement: Research funded by DARPA CLASIC.

References

[1] H. A. Mahmoud, T. Yucek, and H. Arslan, "OFDM for cognitive radio: merits and challenges," *IEEE Wireless Comms.*, vol. 16, no. 2, 2009.
[2] N. Dinur and D. Wulich, "Peak-to-average power ratio in high-order OFDM," *IEEE Transactions on Comms.*, vol. 49, no. 6, 2001.
[3] B. Murmann, "A/D converter trends: power dissipation, scaling and digitally assisted architectures," in *IEEE CICC*, 2008, pp. 105–112.
[4] Y. Tsividis, "Externally linear, time-invariant systems and their application to companding signal processors," *IEEE TCAS II: Analog and Digital Signal Processing*, vol. 44, no. 2, pp. 65–85, 1997.
[5] K.-I. Wu, S.-Y. Hung, S.-H. Hung, and C. C.-P. Chen, "A fast-settling high linearity auto gain control for broadband OFDM-based PLC system," in *IEEE ISCAS*, 2015, pp. 2852–2855.
[6] T. Burger and Q. Huang, "A 13.5-mw 185-Msample/s ΔΣ modulator for UMTS/GSM dual-standard IF reception," *IEEE JSSC*, vol. 36, no. 12, pp. 1868–1878, 2001.
[7] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 db SNDR and 99 db SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE JSSC*, vol. 50, no. 12, pp. 2891–2900, 2015.
[8] R. K. Palani and R. Harjani, *Inverter-Based Circuit Design Techniques for Low Supply Voltages*. Springer, 2017.
[9] W. M. Sansen, *Analog Design Essentials*. Springer, 2006.
[10] B. J. Hosticka, "Dynamic CMOS amplifiers," *IEEE JSSC*, vol. 15, no. 5, pp. 881–886, 1980.
[11] Y. Lin *et al.*, "An 11b 1GS/s ADC with parallel sampling architecture to enhance SNDR for multi-carrier signals," in *IEEE ESSCIRC*, 2013.
[12] M. El-Chammas *et al.*, "A 90 db-SFDR 14b 500 MS/s BiCMOS switched-current pipelined ADC," *IEEE ISSCC*, pp. 286–287, 2015.
[13] A. Venca, N. Ghittori, A. Bosi, and C. Nani, "A 0.076 mm2 12b 26.5 mw 600MS/s 4×-interleaved subranging SAR-ΔΣ ADC with on-chip buffer in 28nm CMOS," in *IEEE ISSCC*, 2016, pp. 470–472.

TABLE I: Performance Comparison

	[11]	[7]	[12]	[13]	**This work**
Technology	65nm	40nm	180nm	28nm	**65nm**
Architecture	Pipeline	SAR	Pipeline	SAR-ΔΣ	**Comp. SAR**
Supply(V)	2.5/1.2	2.5/1.2	3.3/1.8	1.2-1.5	**1**
Area(mm^2)	4.14	0.236	2.5	0.076	**0.163****
f_s(MS/s)	1000	35	500	600	**100**
DR(dB) @Nyq	54	74.4	64	58	**54.6**
Power(mW)***	350	54.5	550	26.5	**12.27**
$FOM^{****}_{Schreier,nyq}$	145.55	159.5	150.6	158.5	**150.7***

*Adding estimated digital compression power results in a FOM of 150.6 dB
**Active area ***All except [11] includes on-chip driver power
****$FOM_{Schreier,nyq} = DR_{nyq} + 10 * log_{10}(\frac{f_s}{2}/Power)$ dB