Highly digital 1 GS/s 7-bit PWM ADC in 65 nm CMOS using time-domain quantisation

A. Saha✉ and R. Harjani

A 2 × time-interleaved 1 GS/s 7b ADC is presented, which uses pulse-width modulation and time domain quantisation for digitisation and is designed for wide channel bandwidths available at mm-wave frequencies. The area, resolution and power performance of the highly digital time-domain architecture is likely to scale with technology. The prototype ADC achieves 5.24 ENOB at a Nyquist rate while consuming 5.22 mW of power, resulting in a $FOM_{Walden,nyq}$ = 138.13 fJ/conversion step in TSMC's 65 nm GP CMOS process.

Introduction: As our desire for wireless spectrum continues unabated, mm-wave band frequencies (28, 38, 60 GHz and the E-band) with wide unlicensed spectrum availability is increasingly being explored. ADC requirements for these applications have been estimated to be about 5 bits of resolution and 1 GHz of signal bandwidth [1]. Flash and time-interleaved SAR ADCs have been primarily used for multi-Gbps applications. Flash becomes impractical for over 6–7 bits resolution due to the exponential growth of comparators with each additional bit. SAR ADCs typically need extensive time interleaving due to its inherent low-speed binary search mechanism, but unfortunately, clock skew errors are harder to calibrate and limit the achievable parallelism [1]. Additionally, it is getting increasingly difficult to obtain a higher resolution in the voltage domain due to the continuous decrease of V_{DD}, relatively constant V_{th}, and the lower g_m/g_{ds} ratio of the transistors.

This work presents a pulse-width modulated (PWM) ADC using quantisation in time instead of the voltage domain. Time resolution has traditionally doubled every 4 years due to technology scaling and will ultimately be limited by jitter noise [2]. The highly digital delay line based design of time quantisers allows for the scaling of the area and power with technology improvement. Although time quantisation has been used extensively in all-digital PLL and VCO-based ADCs, high-resolution time-domain based ADCs in the GHz range have rarely been reported. Naraghi *et al.* [3] demonstrated a 300 kHz 9b PPM ADC, which uses complex post-processing. Li *et al.* [4] report a 1 GS/s 4b ADC, which modulates the delay of a buffer. As far as we are aware, this is the first GHz time-based ADC with over 4-bit resolution.

Circuit implementation: Fig. 1 shows the block diagram of the proposed ADC, consisting of a triangular wave generator (TWG, refer to Fig. 2), a sampler, a comparator and a time-to-digital converter (TDC). The power distribution and the single-ended version of the differential prototype are shown in Figs. 3 and 4. The comparator compares both inputs to generate a PWM wave, which propagates through a TDC, producing a digital output. The timing diagram of the circuit is shown in Fig. 5*a*. A 2 × time interleaving is used to increase the speed up to 1 GS/s. For this prototype, gain/offset calibration for the time interleaved ADCs are done off-chip.

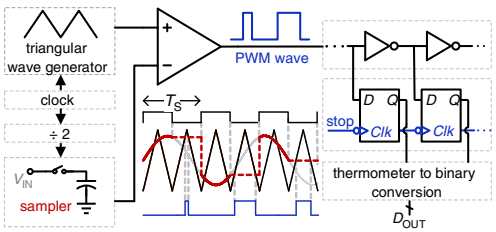

Fig. 1 *Block diagram of the proposed ADC with colour-coded waveforms*

Sampler and comparator: A constant V_{GS} sampler is used for uniform sampling and to reduce switch R_{ON} variation. An open-loop amplifier with seven cascaded stages is used as the continuous time comparator.

Triangular wave generator: A differential pair acting as a pair of current-mode switches charges/discharges the output load linearly to generate a triangular wave (refer to Figs. 2*a* and *b*). Fig. 2*c* shows the simulated polynomial fit and goodness of fit by R^2 linear regression. The polynomial fit confirms > 60 dB linearity for both edges. Here, $C_{gate,in}$ variation of the comparator constrains the smallest capacitive load (C_{TWG}) that can be used. The TWG power can be further reduced by utilising an auto-zero comparator that reduces the input device size. The mismatch between pull-up and pull-down currents is limited by the g_m/g_{ds} ratio of M4.

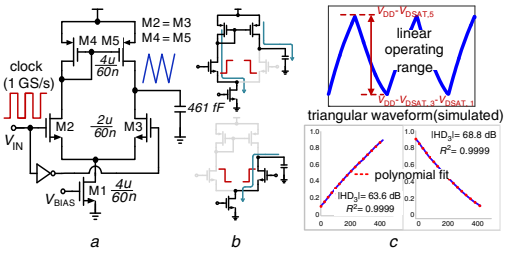

Fig. 2 *Triangular wave generator*

a TWG,
b TWG charging/discharging,
c Linear operating range and goodness-of-linear-fit of the triangular wave

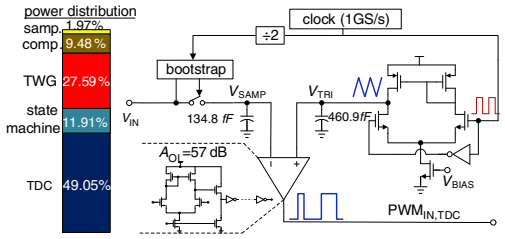

Fig. 3 *Single-ended PWM generation of the proposed differential prototype*

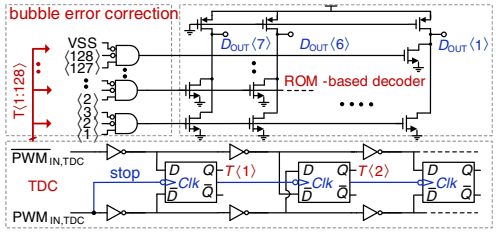

Fig. 4 *TDC implementation (time interleaving is not shown)*

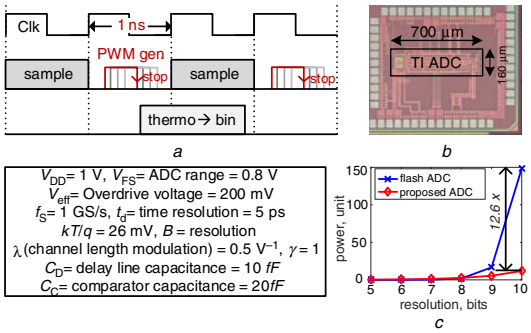

Fig. 5 *Timing, chip micrograph and performance comparison*

a Timing diagram
b Die photo,
c Power comparison

Time-to-digital converter: An inverter-based delay line forms the core of the TDC. Sense amplifier-based D-flipflops (DFFs) are used to sample the thermometer coded data with the falling edge of the PWM signal [3], which is converted to binary using a ROM-based decoder with bubble error correction (Fig. 4).

System advantages: Increasing ADC SNDR by 6 dB requires a 2 × /4 × increase in the power, depending on targeted resolution [5]. For digital CMOS, scaling a technology reduces the area by 50% and increases the operating frequency by 43%. With V_{DD} being scaled down by 70% (constant *E*-field scaling), a 50% reduction in the digital power can be

achieved [2]. Scaling the digital circuits of the proposed highly digital ADC by a technology will scale the FOM by a factor of $((1-0.5x)/1.43) = 0.48$ ($x =$ % digital power, 0.61 in this design). We kept the analogue power constant in this calculation, although C_{TWG} ($\propto$ power) can theoretically be reduced by ~19× from a thermal noise perspective if an auto-zero comparator is used for offset correction, having a negligible impact on the FOM.

$$P_{Proposed} = P_{TWG} + P_{Comp} + P_{TDC} \quad (1)$$

$$P_{TWG} = \frac{36 \cdot kT \cdot \gamma \cdot f_s \cdot 2^{2B}}{\lambda \cdot V_{eff}} \quad (2)$$

$$P_{Comp} = \frac{9\pi \cdot kT \cdot \gamma\lambda \cdot V_{eff}^2 \cdot f_s \cdot 2^{2B} \cdot V_{DD}}{V_{FS}^2} \quad (3)$$

$$P_{TDC} = \underbrace{2^B \cdot C_D \cdot V_{DD}^2 \cdot f_s}_{\text{Delayline}} + \underbrace{\frac{2^B \cdot C_C \cdot V_{eff} \cdot V_{DD} \cdot \ln 2}{1/(2f_s) - 2^B t_d}}_{\text{DFF}} \quad (4)$$

$$P_{Flash} = (2^B - 1) \cdot 24kT \cdot B \cdot \ln 2 \cdot f_s \cdot \frac{V_{eff}}{V_{DD}} \cdot 2^{2B} \quad (5)$$

The total power consumption of the proposed B-bit ADC (1) is compared with a thermal noise limited B-bit flash ADC in Fig. 5*c* [6]. Sampler power is ignored in both the cases. A 10-bit flash at 1 GS/s will require *12.6*× more power than the proposed ADC, increasing more aggressively for higher resolution. The power consumption of TWG and comparator in the proposed ADC are given (without proof) in (2) and (3), respectively (refer to Fig. 5*c* for the parameter definition). We derived these equations considering the total jitter noise generated by the TWG, comparator and the sampler is equal to the quantisation noise of the TDC and is equally distributed. The power consumption of a B-bit TDC is given by (4) [3].

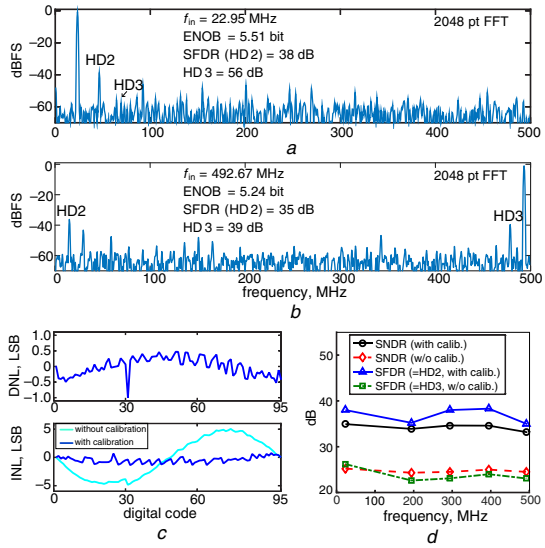

Fig. 6 *Measurement results of the proposed ADC*

a, *b* Measured frequency spectrums (after calibration) of the time-interleaved ADC

c DNL/INL

d SNDR/SFDR versus input frequency

Measurement results: The proposed ADC, fabricated in TSMC's 65 nm GP CMOS occupies an active area of 0.112 mm^2, where the scalable TDC occupies 78.5% of the area (Fig. 5*b*). Figs. 6*a* and *b* show the FFT spectrum of the time-interleaved ADC output at 1 GS/s. It achieves 5.51 ENOB at 22.91 MHz and 5.24 ENOB at 492.67 MHz with LUT based INL calibration [7] to reduce the pulse width non-linearity resulting from parasitic capacitance, which could be eliminated with a careful layout effort. The total power consumption at 1 GS/s is 5.22 mW. The TWG is operated from 1.2 V supply to increase the linear range. The rest of the blocks operate from a 1 V supply. Fig. 6*c* shows the measured DNL (0.47/−1 LSB) and INL (0.76/−1.36 LSB with calibration, 5.04/−4.85 LSB without calibration). The ADC does not span the complete range due to increased time resolution from the parasitic effect. Fig. 6*d* shows the SNDR and SFDR as a function of input frequency. The calibrated SFDR is limited by HD2 which is likely the by-product of the pseudo-differential TWG and comparator. Table 1 compares the proposed ADC with state-of-the-art ADCs ($1GS/s < f_s < 6GS/s$) [8–10]. The proposed ADC is better than similar specification flash ADCs and is comparable to subrange and SAR ADCs. Note, reported FOM for SAR ADCs often do not include driver and buffer power which can be >50% [5]. Scaling the proposed design to 40 nm will result in a $FOM_{W,nyq} = 66.3$ fJ/conv step and a 40% reduction in the area.

Table 1: Performance comparison

	[8]	[9]	[10]	This work
Technology	40 nm LP	65 nm	65 nm	65 nm
Architecture	folding-flash	subrange	TI-SAR	PWM
Supply(V)	1.1	1.2	1.2	1–1.2
f_s (GS/s)	2.2	1.2	6	1
Resolution	7b	7b	6b	7b
SNDR(dB) @Nyq	37.4	36.2	30.13	33.3
Power (mW)	27.4	8.11	10.6	5.22
Area (mm^2)	0.052	0.087	0.09	0.112
FOM_W^a@LF	205.7	114	116.7[b]	114.55
FOM_W^a@Nyq	205.7	125	116.7[b]	138.13

[a] $FOM_W = ((\text{Power})/(2^{ENOB} \cdot \min(f_s, 2 \cdot f_{in,max})))$ fJ/conversion-step.
[b]Estimated FOM, considering driver power [5].

Conclusion: In this Letter, a prototype 1 GS/s 7b PWM ADC for mm-wave bands using time-domain quantisation is demonstrated in TSMC's 65 nm GP CMOS process. The architecture is highly digital, and scaling by one technology generation to 40 nm will likely result in a 52% improvement in the FOM and 40% reduction in the area. The architecture provides a superior alternative to the flash architecture for GS/s applications and possibly can outperform any voltage domain ADCs with scaling.

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One or more of the Figures in this Letter are available in colour online.

A. Saha and R. Harjani (*Department of Electrical & Computer Engineering, University of Minnesota, Minneapolis, MN, USA*)

✉ E-mail: sahax008@umn.edu

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