A 0.4-1.0GHz, 47MHop/S Frequency Hopped TXR Front-End With 20dB In-Band Blocker Rejection

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***Abstract*—An ultra-fast frequency hopping spread spectrum transceiver front-end architecture is presented that provides 20dB of processing gain at RF for the first time. This enables the receiver front-end to supress any in-band interferes by 20dB before they arrive at the LNA. The circuit consists of passive mixers and agile digital oscillator/DAC engines that are capable of quickly moving in the frequency domain with very low power. A transient hop time of 1.5ns is achieved in this design. The front-end implemented in 65nm CMOS technology, occupies an active area of 3.1mm^2, and consumes 24mW (=P_{TX}=P_{RX}) from a 1V power supply for a center frequency of 1GHz.**

I. Introduction

Frequency hopped spread spectrum (FHSS) techniques have traditionally been used for secure and resilient communications. Conventionally, FHSS systems avoid blocking signals by avoiding their frequency of operation. However, this requires blocker identification to continue communications. Additionally, any in-band blocker would eventually end up jamming the active frontend circuits. Currently, the fastest FHSS systems operate at a maximum of one symbol per hop [1]. FHSS schemes, in theory, have the capability of suppressing in-band jammers if a single symbol is spread over multiple hops. Unfortunately, this has traditionally not been possible due to the limited transient response of PLLs. In particular, the transient response of PLLs from one frequency to another is limited by the filter loop bandwidth. Given a loop bandwidth that is 1/10th of the input reference frequency and approximating the settling time as four time constants the maximum hop-rate for a 30MHz input reference frequency PLL is limited to 75kHops/S [2]. In this design, we present a FHSS system that is able to hop at 47MHops/S and provides 20 dB of processing gain and in-band blocker suppression.

N-path *band-stop* filters have sometimes been used to suppress in-band blockers. However, they suffer from poor linearity, limited jammer rejection and require a priori knowledge of the exact location of the blocker in the frequency domain thus, requiring power hungry spectrum sensing techniques. Additionally, these circuits becomes power hungry and complex with multiple LOs, one for each jammer, when attempting to suppress multiple blockers at the same time. Furthermore, as they operate in-band, they need to have a very small bandwidth so as to not reduce the usable bandwidth for the spectrum. Narrowband N-path notch filters require extremely large on-chip area. In our design however, utilizing low-power ultra-fast circuit architectures, multiple blockers can be suppressed without any a priori knowledge of their frequency content. Like other designs, out of band blockers can be canceled using well known on/off chip techniques [3].

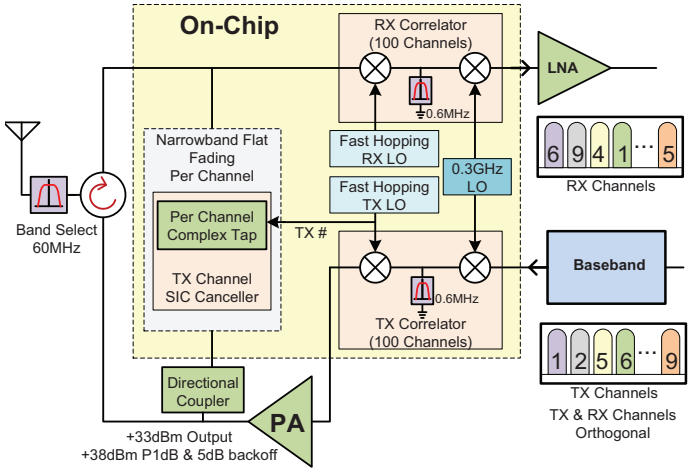

Fig. 1. Proposed fast-FHSS transceiver architecture

II. System Architecture

The system spreads each symbol into 100 channels to provide 20dB of processing gain for the signal that suppresses the jammer by the same amount. A single channel's bandwidth is 0.6MHz for a total band of 60MHz. The transmitter and receiver co-exist in the same 60MHz band but never operate on the same channel frequencies. As Fig. 1 shows, direct self interference is avoided by utilizing orthogonal channels for the transmitter and receiver, i.e., the transmitter and receiver never occupy the same channel at any given time. To accommodate a 470Kbit/s data rate and 20 dB of blocker suppression, a hopping speed of 47Mhop/s is required for the frontend. A 4-path filter is used that is tuned to one of the channels at any point in time. Being passive, the filter is highly linear with noise performance that is largely limited by its load termination, i.e., the low-noise amplifier (LNA). Even with the 25dB suppression from the duplexer, about 8dBm of TX power shows up at the RX frontend. An all passive self-interference cancellation circuit is used to suppress this TX channel interference (orthogonal from the RX channel) from overloading the RX frontend [4]. A 60MHz band-select filter is used directly after the antenna to suppress any out of-band interference. The required fast hopping local oscillator signals for the transmitter/receiver is generated using programmable ultra-fast hopping digital oscillators (DO). Two separate DOs are required as the TX and RX channels are orthogonal. An external PA is used to generate the +33dBm output required. A portion of the PA output is coupled via a directional coupler for on-chip self-interference cancellation (SIC).

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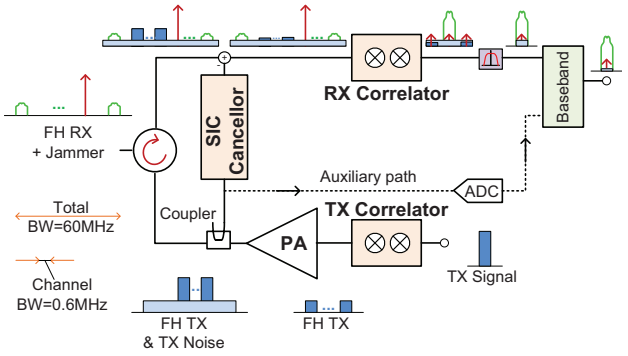

Fig. 2. Signal flow through the overall architecture

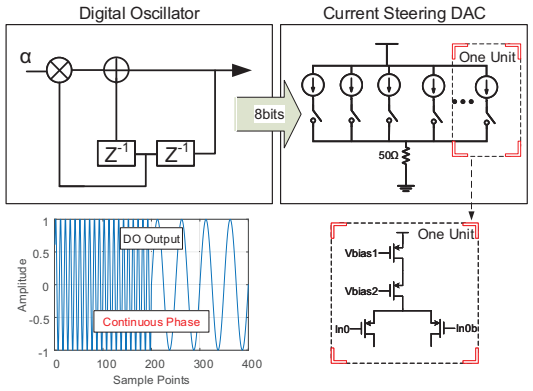

Fig. 3. Top LHS: Structure of DO adapted from [7]. Top RHS: Current-mode 8bit DAC. Bottom LHS: Continuous phase between frequency jumps, Bottom RHS: Current steering DAC details

A. *In-band jammer resistance*

The overall system operation is best understood with the help of Fig. 2 that shows the signal flow throughout the system. It is easiest to follow the signal by starting at the transmitter. The modulated TX signal is frequency hopped (FH) by the fast hopping TX correlator (blue). This signal is amplified by the 2 watt off-chip PA. The PA adds broadband noise due to the finite noise figure of the PA (light blue). A portion of this signal (-25dB down) couples through the duplexer to the RX. The RX sees the FH RX signal (green) plus a narrow-band CW in-band jammer (red). The SIC block cancels the FH TX leakage at the receiver. This signal then passes through the RX correlator where the FH RX sees 20dB of processing gain while the jammer is spread by 20dB. A filtered version of this signal is sent to the baseband where any residual out of channel signal is removed. The broadband TX noise signal can be suppressed in the digital baseband using an axillary path as in [5] and is not included in this prototype design.

This in-band jammer rejection property in frequency hopped systems only exists if there is processing gain. The correlators in our design are passive N-path switched-capacitor circuits and possess good linearity. This signal processing is done in the current domain, which limits the voltage swing at the correlator input due to the blocker, enhancing the jammer handling capability of the receiver. The system can operate effectively with jammers that are 20dB larger than what would have saturated a normal receiver. A quick explanation of the jammer rejection is as follows. Assuming that the receiver visits all the N channels before returning to the channel with the interferer, it only sees the jammer $1/N^{th}$ of the time. However, the signal is seen at each of the N channels. Therefore, effectively, the jammer power after the correlation process is reduced by N times while the signal power is retained. In our design with $N = 100$, i.e., 100 channels, the jammer suppression is $10log(N) = 20dB$.

III. Circuit Design

Next, we describe the circuit details for the fast hopping bandpass filter and the ultra-fast hopping LO generator.

A. *Fast hopping band-pass filter*

The fast hopping band-pass filter is realized using a combination of the well known N-path structure [6] and fast hopping LO generators. We use N=4 here. The 25% duty cycle clocks required to drive the 4-Path filter are realized using flip-flops and logic. The left-hand mixer down-converts the RF signal to DC and the right-hand mixer up-converts the DC baseband signal to a desired fixed RF signal (see Fig. 1). The second mixer is included to take advantage of the ultra-low noise amplifiers available on the market to minimize the overall receiver NF. The project goal was focused on the correlators only but the 2^{nd} mixer can be replaced by baseband circuits to realize a frequency hopped mixer-first receiver. The N-path filter is able to hop from one frequency to another almost instantaneously because of the all digital 25% clock dividers and because the signal history is only maintained at DC on the baseband capacitors. The switches are designed to have 3ohms of series resistance. To enhance linearity, only MIM capacitor are used in this design such that the linearity is only limited by the switches.

B. *Ultra-fast hopping signal generator*

A popular approach to synthesize custom signals is via DDS (direct digital synthesis). The problem with this approach however, is circuit complexity and high power consumption [8]. To mitigate these issues, an all digital sine-wave oscillator (DO) was adapted from [7] which is shown in Fig. 3. The architecture of [7] was not intended for high speed operation and is improved in this work. One additional register is added but the number of integrators and multipliers is halved in comparison to [7]. The output frequency of the DO is centered around $f_s/4$ where f_s is the sampling clock frequency. The value of α sets the output frequency. Setting $\alpha = 0$ results in an output frequency of $f_s/4$. The DO was designed in Verilog and then synthesized using a custom cell library. The digital output of the DO is converted to an analog value using an on-chip current steering DAC. It can be shown that, in this design, an 8 bit DAC is sufficient to maintain the required phase noise for the minimum sensitivity of the receiver when a high-Q fast hopping injection locked bandpass filter is used for filtering [2]. The DAC resolution does however, affect close-in spurs and is discussed later. The high-Q filter is only

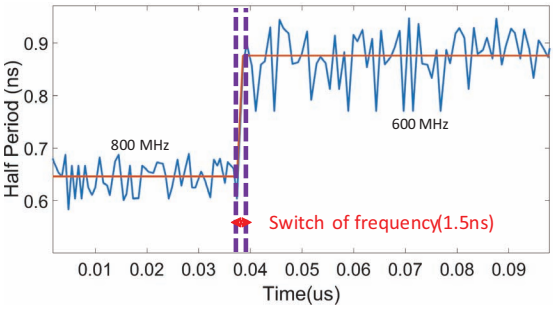

Fig. 4. Measured DO+DAC hopping speed

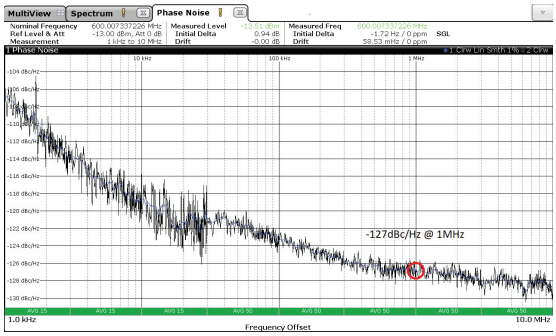

Fig. 5. Measured phase noise of the DO + DAC

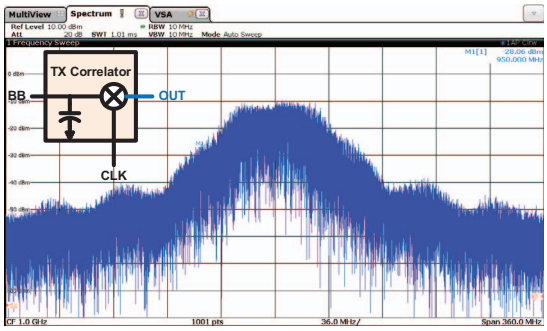

Fig. 6. Fast hopping TX output spectrum

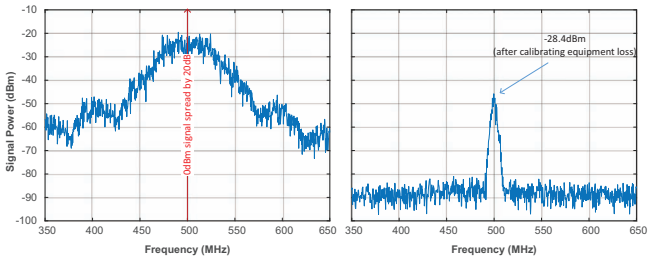

Fig. 7. Self interference cancellation due to orthogonal signaling

required for improved output-of-band performance and was not included in this prototype due to time limitations.

IV. Measurement Results

The front-end was fabricated in TSMC's 65nm RF GP CMOS technology. Fig. 4 shows the measured transient time for the DO + DAC combination from 800MHz to 600MHz. The transient time is primarily due to digital circuits other than the DAC that has a 2GHz signal bandwidth. To measure the frequency switch time we sampled the DAC output with a R&S RS-RTO 1044 20Gsps sampling scope that interpolates the sampled to 100Gsps. The transient sampled output was lowpass filtered with a 100tap FIR filter in Matlab (FIR to maintain linear phase). We then estimated the frequency of operation by evaluating the zero crossings so our time resolution is limited by one-half period, or roughly 0.67ns at 750MHz. The measured transient time from 800MHz to 600MHz is 1.5ns or about 1 clock period within our measurement resolution limits. The measured power consumption for a 1GHz DO output ($F_{clock}/4$) for the DO + DAC is 6mW. The measured frequency accuracy of the digital oscillator is better than 20ppm in this design. Simulations suggest that the accuracy is even better and is limited by the frequency resolution of our measurement technique.

Fig. 5 shows the measured phase noise of the fast hopping clock generation circuit at a fixed frequency of 600MHz. The measured phase noise for the circuit is -127dBc/Hz at 1MHz offset and for the signal source is -140dBc/Hz at 1MHz offset. Experimental explorations suggests that the phase noise deterioration is mainly due to the small DAC termination resistor (limiting signal amplitude) and due to the AM-PM conversion of the source follower buffer (for probing purposes) included after the DAC output. Within the DO, 16 bit resolutions is used throughout to minimize phase noise deterioration. The finite 8-bit resolution of the DAC does not add to the phase noise directly but adds to the tonal behaviour of DO+DAC combination. A higher resolution DAC and dithering techniques can further reduce this tonal behavior. No spurs were seen within the 10MHz bandwidth used for phase noise measurements.

The output spectrum of the TX correlators driven by an arbitrary waveform generator (AWG) is shown in Fig. 6. The AWG was programmed to randomly hop across all 100 channels with a hop-rate of 50MHops/s. The output shows the 20dB spreading that we would expect from this design.

Even though the RX and TX paths use orthogonal channels there is some self interference leakage from the TX to the RX due to the finite out-of-band rejection (1^{st} order) capability of the simple N-path filter. This is seen in Fig. 7 LHS and RHS. Fig. 7 LHS shows a 0dBm TX signal that is spread by 20dB and Fig. 7 RHS shows the measured RX signal after the correlator and filter. The TX-to-RX self interference is suppressed by 33dB with a 50 channel separation, 28.4dB with a 30 channel separation (shown in Fig. 7) and 27.3dB for a 10 channel separation between TX and RX.

Next, the overall system was configured to be a transmitter and receiver pair. The output of the transmitter correlator was fed via a amplifier and attenuator such that a -19.5dBm signal was fed to the correlator inputs. Both correlators were driven by a common random 100 channel frequency hopped LO with a hop-rate of 50MHops/s. In this case there is full synchronization between the TX and RX except for any delay through the LNA, cables and attenuator. The measured 64-QAM received data constellation is shown in Fig. 8. The

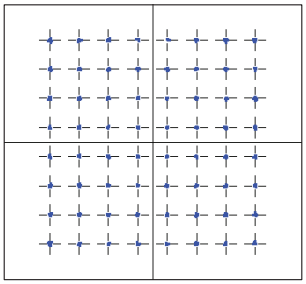

Fig. 8. 64QAM constellation

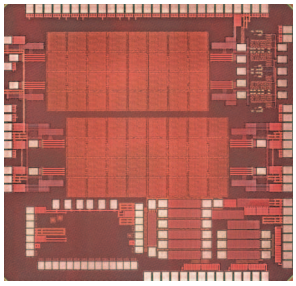

Fig. 9. Chip microphotograph

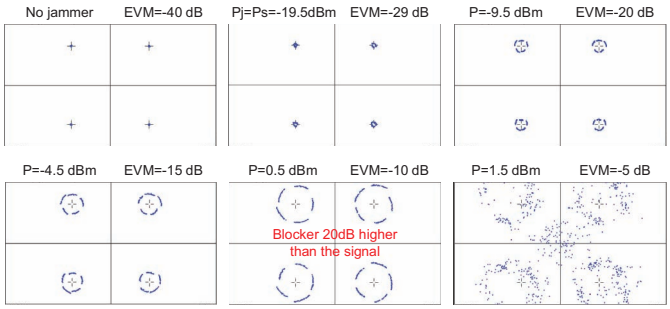

Fig. 10. Measured jammer performance

measured EVM was -38dB. The chip microphotograph is shown in Fig. 9. The total active area is 3.1mm^2. The total power consumption is 24mW for receive and for transmit from a 1V power supply.

In this experiment we use the same setup of the last measurement. However, this time we add an in-band jammer to the RX input to measure it's blocker handling performance. We generated a QPSK signal at the transmitter and measure the constellation of the received signal at the receiver in the presence of a narrow-band in-band CW jammer. The amplitude of the jammer is then varied to see the effect on the constellation. QPSK modulation is chosen for visual clarity. Fig. 10 shows the RX measured constellation and EVM for different jammer powers. As can been seen the receiver can successfully demodulate received symbols even when an in-band jammer is present and is up to 20dB larger than the desired signal. This is a direct consequence of the 20dB processing gain that is realized directly at RF by the fast frequency hopped correlators.

Table I compares this design with other related frequency hopped and direct sequence spread spectrum systems in the published literature. As far as the authors are aware this is the first frequency hopped system with processing gain and the only frequency hopped system with processing gain at RF. This is reflected in the table with zero processing gain for [1] and [9]. We also note that this system has a hopping speed that is 300X faster than prior frequency hopped systems. The data rate also is roughly 3 times faster. Reference [10] provides 18.6dB of TX SIC and [11]d provides 38.5dB of TX SIC.

TABLE I
COMPARISION WITH STATE OF THE ART

Ref	This work	[1]	[9]	[10]	[11]
Method	FH	FH	FH	DS	Code-domain
RF processing gain(dB)	20	0	0	NA	NA
Hopping speed(Mhops/s)	50	0.08	0.16	NA	NA
N-of hops/symbol	100	1	1	NA	NA
Center frequency(MHz)	400-1000	900	915	1000	300-1400
Power(mW)(TX=RX)	24	NA	525	NA	35
RF TX SIC(dB)	33	NA	NA	18.6	38.5

V. CONCLUSIONS

A new ultra-fast hopping transceiver front-end architecture is proposed in this work that provides 20dB of processing gain for the first time. All the signal processing is performed in the RF domain in order to suppress any in-band interfering signals before they reach the first amplification stage in the receiver chain. The design does not rely on any a priori knowledge for jammer suppression and can suppress one or more jammers by 20dB. The system has the highest frequency hop-rate in comparison to the state of the art and only consumes 24mW for RX and 24mW for the TX for a total of 48mW for the transceiver frontend.

ACKNOWLEDGMENT

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