A 5μW-5mW Input Power Range, 0-3.5V Output Voltage Range RF Energy Harvester with Power-Estimator-Enhanced MPPT Controller

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***Abstract*—A 5μW - 5mW input power range, 0 - 3.5V output voltage range RF energy harvester is designed to charge supercapacitors for RFID applications. Voltage protection techniques are used to improve the peak output voltage from 2.5V to 3.5V resulting in a 100% increase in stored energy. An all analog low power maximum power point tracking (MPPT) controller with an embedded power estimator increases the maximum tracking speed by 8x, improves the input power range by 8x, and accumulates 35% more energy during charging transients. The chip is fabricated in TSMC's 65nm GP process, occupies an area of 0.15mm^2, and has a measured peak efficiency of 91%.**

I. Introduction

The emerging internet of things (IoT) will connect many untethered devices, e.g. sensors, RFIDs and wearable devices, that require wireless charging or ambient energy harvesting [1]. The energy would need to be harvested onto a storage device, i.e., a battery or a supercapacitor (supercap [2]). Regardless of the initial energy source, a power management unit (PMU) is necessary to efficiently charge the storage device over a large input power range. This paper proposes an inductive buck & boost DC-DC converter for RF rectifiers to charge a supercapacitor from 0 to full-scale (3.5V).

A supercap is a near ideal power supply for biomedical applications as it has no harsh chemicals, infinite shelf-life and can be recharged nearly infinitely [2]. For this reason, it is intended to be used in our RFID tag as a substitute for a battery. When an RFID reader approaches the tag, a wireless signal is transmitted to the tag and is rectified to a low DC voltage. The proposed harvester up converts this small voltage to a higher voltage to charge the supercap. The goal is to charge a 80mF supercap to 3.5V within 2 minutes, so the harvester needs to be able to handle a maximum input power level of ~5mW. However, the input power incident on the harvester can vary significantly with the distance and the angle between the reader and the RFID. Therefore, to ensure operation in all scenarios the harvester should be able to operate at extremely low powers as well (e.g., ~5μW). To ensure the most efficient use of the incident power we use a fast response high-efficiency maximum power point tracking (MPPT) solution. The overall system includes a reader and one or more RFID tags. This paper focuses on the energy harvester within the RFID tag.

Early MPPT algorithms utilized fractional open circuit voltage methods (FOCV) [3]. This approach was simple and suitable for low power applications, but assumed that the power source was linear, which is not the case for diode based RF rectifiers or photovoltaic harvesters [1]. The perturb and observe (P&O) method or hill climbing, is more promising for use in an MPPT system with nonlinear impedance sources.

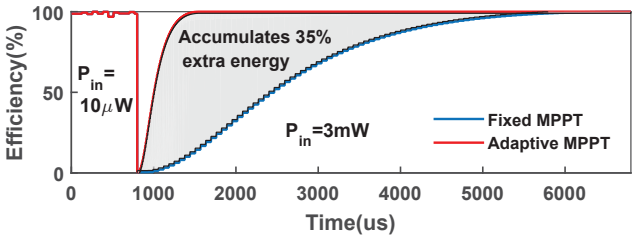

Fig. 1: Transient MPPT efficiency for fixed v.s. adaptive MPPT

Reference [1] proposed a low power time-based power monitor in a P&O algorithm. However, the time-based approximation is only valid for high conversion ratios. Reference [4] achieved a more precise P&O MPPT implementation with pulse integration (PI-MPPT). This approach is able to track well over a small power range (~20x) as it relies on a single capacitor to store the MPP information, which can either be made sensitive or is easily saturated. Reference [5] combines FOCV and P&O to achieve a higher power range, which unfortunately complicates the system design. This paper proposes an adaptive current integration implementation that expands the MPP power tracking range to ~1000x.

A common practice for saving power, is to run the MPPT controller at a frequency that is much lower than the switching frequency [6]. The MPPT frequency is then usually set by the lowest power and significantly reduces the tracking speed. This paper proposes an enhanced MPPT controller that has a built-in power estimator to adaptively tune the MPPT frequency, so that it can save power during low power inputs and accelerate the tracking speed at high power inputs. Fig. 1 shows a system-level simulation of a fixed frequency based MPPT harvester (blue line) and our proposed adaptive MPPT harvester (red

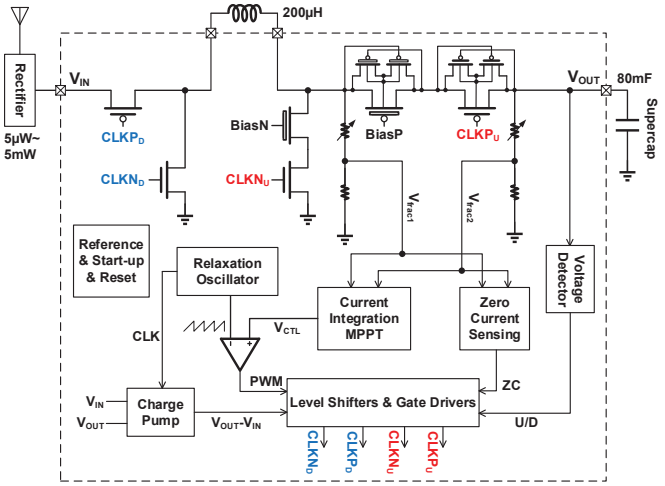

Fig. 2: Proposed RF energy harvester block diagram

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line). In this figure, there is a change in input power from 10μW to 3mW at 1000μS. The new adaptive algorithm rapidly increases the MPPT frequency, resulting in a 8x increase in tracking speed and 35% additional energy being accumulated during the charging transient.

Since the power stored is proportional to V_{SC}^2, a number of previous designs have resorted to either BCD technology or HV-CMOS [4], [7] to increase the output voltage. However, these technologies are more expensive and less integrateable than standard CMOS. This paper proposes new voltage protection techniques for standard 65nm technology and increases the highest output voltage from 2.5V to 3.5V, so that the energy stored increases by nearly 100% ($3.5^2/2.5^2 = 1.96$).

II. Harvester System Architecture

The block diagram for the proposed system is shown in Fig. 2. The power train includes both a buck and a boost converter, with an off-chip 200μH inductor. Pulse width modulation (PWM) is utilized to tune the converter duty cycle, and a fixed frequency, discrete conduction mode (DCM) scheme is implemented. Previous designs have suggested that a single boost converter can be used to chage supercaps [8]. However, this is highly problematic during the initial transient when the supercap (output) voltage is lower than input voltage. In this case, since the left node voltage of the inductor is always higher than the right during both clock phases, the inductor current continues to increase until the power switches are saturated regardless of the PWM signal. This would take it far away from the optimal point. In our design, a zero current sensing (ZC) comparator turns off all switches when it detects that V_{frac1} equals V_{frac2}, to achieve the DCM scheme. Current integration MPPT (CI-MPPT) controller generates a control voltage, V_{CTL}, to tune the converter duty cycle. CI-MPPT details are provided in the next section.

For the boost converter, both of the switches are implemented by stacking one core device and one I/O device (indicated with a thicker gate in Fig. 2), for voltage protection. To turn on the PMOS at the beginning, a negative voltage is generated by a charge pump, through which the lower voltage of $CLKP_U$ is always $V_{OUT} - V_{IN}$. The body of each PMOS power switch is kept connected to the highest

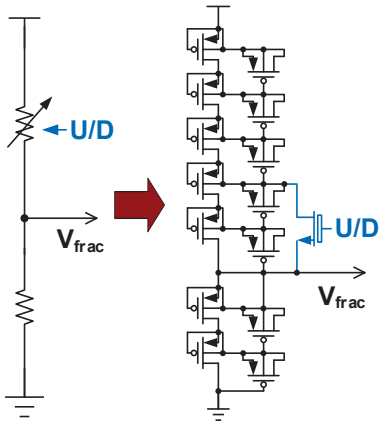


Fig. 3: Resistor ladder implementation

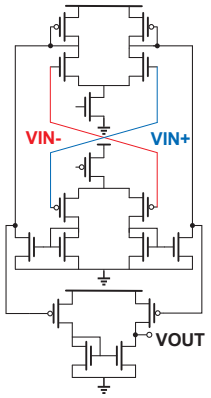


Fig. 4: Rail to rail ZC comparator

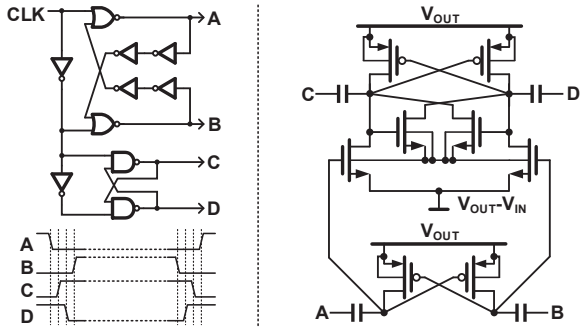


Fig. 5: Low power negative voltage charge pump

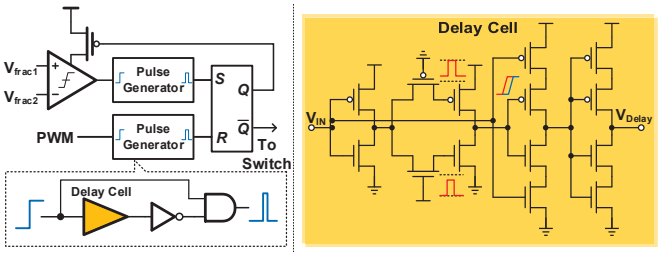


Fig. 6: Low power zero current sensing circuit

voltage node through two PMOS helpers. Unlike designs that insert a resistor in the power train to measure current [4], [9], this design uses the power PMOS switch as the series resistor. As both sides of the series resistor (or PMOS power switch) are potentially high voltage nodes (0∼3.5V), the voltage is divided down by a resistor ladder. A higher voltage ratio is preferred for higher sensitivity during boost conversion, whereas a smaller ratio is required during buck conversion to protect the follow-on circuits from high stress. The resistor ladder ratio is tunable depending on the V_{OUT} voltage level and is implemented using reverse biased diodes to reduce area and quiescent current. Additional bypass MOS caps are added to reduce transients, as is shown in Fig. 3.

The low power charge pump to generate the negative voltage is shown in Fig. 5, where four non-overlapping clock phases are used to prevent short circuit current for better efficiency. The ZC sensing circuit is shown in Fig. 6. Due to the high output voltage range, the common mode voltage of V_{frac1} and V_{frac2} swings from 0V to 1V, so the ZC detector (comparator) has to operate rail-to-rail (Fig. 4). To save power, the comparator is duty cycled. The pulse-generator uses a six-stage low power delay cell which consumes 5x lower power than a simple inverter chain based delay.

III. Current Integration Based MPPT Controller

Conventional MPPTs measure both the voltage and current, and use their product (power) as the optimization target [4]. However, for charging a supercap, because of its large value, the output voltage does not change much during one cycle (max of 1mV at 5mW input power). So the voltage is relatively constant and only the output current needs to be measured and optimized. The MPPT module is shown in Fig. 7. A gm-C integrator converts the fractional voltage from the resistor ladder ($V_{frac1/2}$) to a current and integrates it onto two capacitors (C_A & C_B) alternately. Since $V_{frac1/2}$

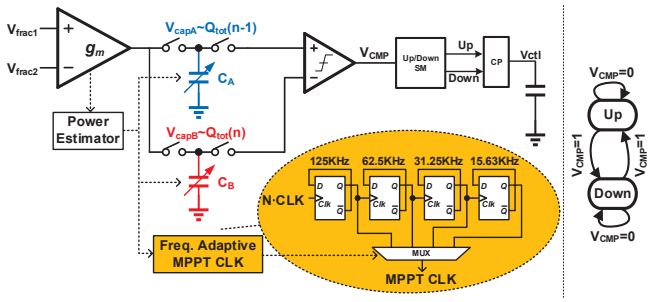
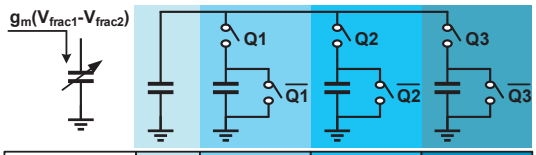


Fig. 7: Proposed analog MPPT controller & state graph

varies between 0∼1V, a rail-to-rail and linear integrator is simultaneously implemented [10]. If the power switch PMOS has an on resistance of R_{on}, the resistor ladder has a ratio of k_{RL}, and the OTA has a transconductance of g_m, we can calculate the voltage on $C_{A/B}$ after one cycle as:

$$V_{capA/B} = \frac{R_{on}k_{RL}g_m}{C_{A/B}} \int_0^T I_L(t)dt = \frac{R_{on}k_{RL}g_m}{C_{A/B}} Q_{tot} \quad (1)$$

where $I_L(t)$ is the load current, and Q_{tot} is the total charge delivered to the supercap in one cycle. Since only the voltage difference between C_A and C_B is critical, any variation of R_{on}, k_{RL} and g_m are common mode and irrelevant. Another important insight from eq. 1 is that, when the capacitance of $C_{A/B}$ is large, the integrated voltage becomes too small to be detected. On the other hand, if the capacitance is too small, it can easily saturate when large power is incident. To solve this problem, a capacitor array is used instead of a single capacitor, as is shown in Fig. 8. Only the smallest capacitor is connected at the start, and every time the voltage reaches V_{th}, an additional capacitor is added and the voltage drops to half of the previous value. Fig. 8 shows the integrated voltage waveform and the switch signal $Q_{1\sim3}$, and a table of the input power range. This structure provides an additional benefit: $Q_{1\sim3}$ shows the input power level – i.e., the "power estimator" block in Fig. 7 just reuses the switch control bits $Q_{1\sim3}$ as a measure of the input power level. At low powers



State	S0	S1	S2	S3
Cap(fF)	200	400	800	1600
Power(μW)	5-600	600-1200	1200-2400	2400-5000
$Q_1Q_2Q_3$	000	100	110	111
f_{MPPT}(KHz)	15.63	31.25	62.5	125

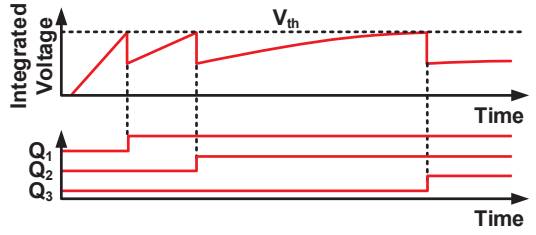


Fig. 8: Capacitor array for large power range and power estimation

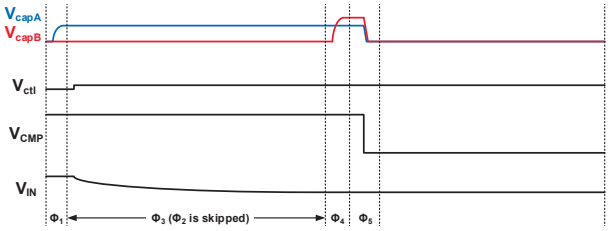


Fig. 9: Critical signals at low power (Q=000, f_{MPPT}∼15KHz)

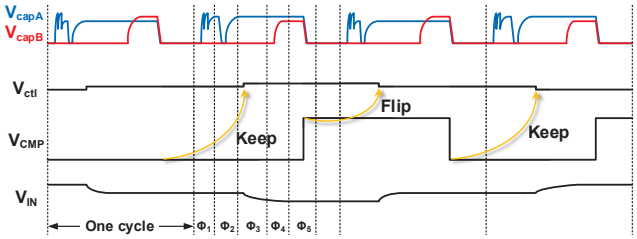


Fig. 10: Critical signals at high power (Q=111, f_{MPPT}∼125KHz)

(Q=000), the MPPT is operated at low speeds (∼15KHz) to save power, at the cost of tracking speed. While at high power (Q=111), the MPPT controller's speed is boosted to ∼125KHz through a MUX, to speed up tracking by ∼8x. There are four frequency possible steps (15.63, 31.25, 62.5 and 125kHz).

Fig. 9 shows the critical signals for the MPPT scheme for low incident powers (Q=000) and Fig. 10 shows them for high incident powers (Q=111). The 5 phases in each MPPT cycle are: power-estimation, pre-power-measurement, perturbation, post-power-measurement and observation. Φ_1 is the power estimation phase and the current is integrated on C_A. At low powers, no switches in the capacitor array are turned on and C_A is retained at its smallest value. So the blue waveform of V_{capA} in Fig. 9 does not have the sawtooth shape as was shown in Fig. 8, while its counterpart at high powers (Fig. 10) does have it. Φ_2 is the pre-power-measurement phase, when C_A is reset and recharged, with the capacitance and the Q values inherited from Φ_1. This phase is necessary to eliminate any charge injection error from Φ_1 for Q=111, but redundant for Q=000, since no switches are turned on. Φ_3 is the perturbation phase, during which V_{CTL} is increased or decreased depending on the previous state. Then the current is integrated on C_B in Φ_4, with the same Q from Φ_1. By comparing the voltages on the two capacitors, namely during the observation phase (Φ_5), the direction of the V_{CTL} perturbation for the next cycle is determined. If V_{CMP}=0, $Q_{tot}(n)$>$Q_{tot}(n-1)$, then the previous perturbation direction is correct and retained, but will be flipped if V_{CMP}=1 (Fig. 10). Thus, V_{CTL} is maintained

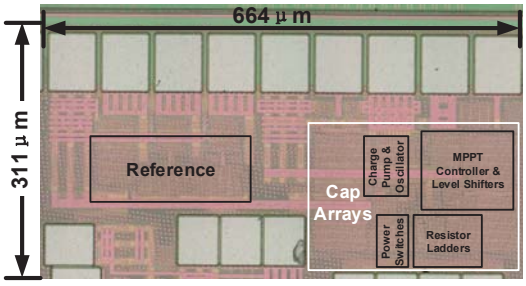


Fig. 11: Die photograph

TABLE I: Measurement result summary and comparison with prior art

Ref	Tech	Input Voltage	Output Voltage	Input Power	Track Time	Architecture	MPPT Algorithm	Peak Efficiency
[3]	0.35μm BCD	1∼7V	1∼8V	33μW∼10mW	20ms	Buck-Boost, PFM	One Cycle FOCV	80%
[4]	0.35μm HV	7∼43V	15V	0.4∼21.1W	350μs	Buck, PFM	PI, Global Search	94.2%
[5]	0.35μm	0.5∼2.4V	3.5V	650μW∼1W	2.9ms	Boost, PWM	AZ-PI, SRE-FOCV	92.6%
[7]	0.25μm BCD	5∼60V	2∼5V	25μW∼1.6mW	800ms	Buck, PFM	VS-P&O	88.9%
[8]	0.25μm	0.5∼2V	0∼5V	5μW∼10mW	–	Boost, PSM	P&O	87%
This Work	65nm	0.6∼1.2V	0∼3.5V	5μW∼5mW	584μs	Buck-Boost, PWM	CI, P&O	91%

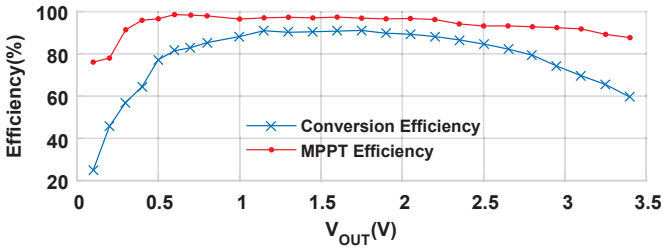


Fig. 12: Efficiency v.s. V_{OUT} @P_{av}=220μW

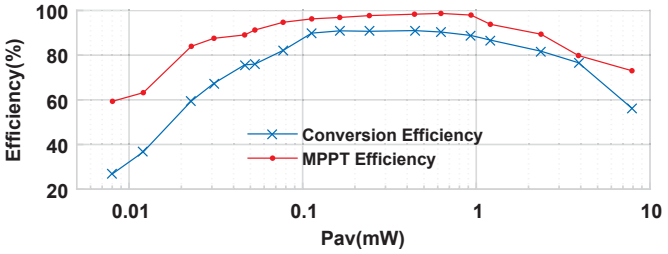


Fig. 13: Efficiency v.s. P_{av} @V_{OUT}=2V

around the maximum power point. The state machine, shown in Fig. 7, implements the MPPT logic.

IV. Measurement Results

The design was fabricated in TSMC's 65nm GP process. The die photograph is shown in Fig. 11. For test purposes, a 2V source in series with a trimmer resistance is used as the power source model. By changing the trimmer resistance, the available power is changed and the harvester can be tested under different conditions. The input impedance of the harvester varies during the charging transient, such that the input voltage seen by the harvester varies between 0.6∼1.2V. Fig. 12 shows the measured conversion efficiency and MPPT efficiency versus V_{OUT}, and Fig. 13 shows them versus P_{av}.

Table I compares this design with prior art. As discussed earlier, it is difficult to simultaneously accommodate a large power range with fast response, e.g., [4] has the fastest track time but has the lowest power range. As was shown in Fig. 1, an MPPT controller that may have high steady state efficiency has a slow track time could significantly reduce overall efficiency during charging transients. So, we have defined a FOM that considers the ratio of max and min power and the inverse of the response time, $FOM = P_{av,max}/(P_{av,min}T_{track})$. This design has the highest FOM (see Fig. 14)and the largest output voltage in standard CMOS while maintaining high efficiency. The power train switches operate at 1MHz, while the MPPT frequency is adapted between 15∼125KHz. The chip occupies an active area of 0.15mm^2.

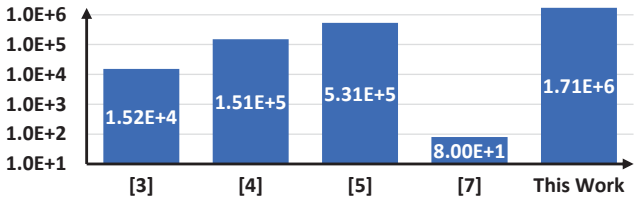


Fig. 14: $FOM = P_{av,max}/(P_{av,min}T_{track})$ (log scaled)

V. Conclusions

This paper describes an inductive buck-boost DC-DC converter with an adaptive MPPT controller for energy harvesting. A built-in power estimator adapts the MPPT frequency and sampling capacitors with the input power level. This improves the input power range to 1000x, reduces the track time by 8x and improves transient efficiency. Voltage protection techniques extend the maximum output voltage to 3.5V (in a 65nm CMOS GP process), resulting in a 100% increase in the stored energy. The circuit has a peak conversion efficiency of 91%, and an MPPT efficiency of 98.7%.

Acknowledgements: Research supported by US Army TATRC.

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