A Sub-1V, 2.8dB NF, 475μW Coupled LNA for Internet of Things Employing Dual-Path Noise and Nonlinearity Cancellation

Mustafijur Rahman and Ramesh Harjani
University of Minnesota, USA

***Abstract*— A 0.7V low power LNA combines a 1:3 frontend balun with dual-path noise and non-linearity cancellation for improved noise performance at low power. In traditional techniques only the noise of the main path is cancelled while the noise of the auxiliary path is minimized by using high power. In the proposed design, the noise and non-linearity of both the main and the auxiliary paths are mutually cancelled allowing for low power operation. The 2.8dB NF, -10.7dBm IIP3 LNA in TSMC's 65nm GP process consumes 475μW of power resulting in an FOM of 28.8dB which is 8.2dB better than the state of the art.**

***Index Terms*— WBAN, noise cancellation, nonlinearity cancellation, low power, LNA, IoT.**

I. Introduction

Low power radios are becoming increasingly important for IoT, WBAN and next generation 5G [1]–[3]. The scaling of the power supply (Vdd) with technology rapidly reduces power consumption in digital circuits where the power consumed can be expressed as $CVdd^2f$. This facilitates power reduction in modern radios that have large digital blocks. Therefore, it is preferable to employ sub-1V circuits in order to reduce power and accommodate technology scaling. However, a low Vdd degrades the SNR of the RF frontend which can be partially restored using noise cancelling techniques. Unfortunately, traditional noise cancelling LNAs are power hungry and are not well suited for low power operation [4]–[6].

Traditional noise cancelling techniques are based on the availability of two suitable nodes X and Y in the circuit where the signals are in phase but the noise of the main path is out of phase at these nodes as shown in Fig. 1a. Noise canceling LNAs have been realized as either common source (CS) [5] or as common gate (CG) [4] amplifiers. For both designs the input impedance is provided by the input transistor M1 as Zin=1/gm_1. For a Zin=50Ω the required gm is 20mS which necessitates that the power is greater than 1.5 milliamperes even for a low $\Delta V_{GS} = 150mV$. A larger ΔV_{GS} is required for higher linearity but results in increased power. Further, the noise of the auxiliary path (M2) does not get cancelled and therefore to improve the overall NF, gm_2 is increased at the cost of higher current (Fig. 1b and Fig. 1c). Mutual noise cancellation has been reported in nonlinearity mixer based RF frontends [7], [8] where the noise of both the main and auxiliary paths are cancelled by virtue of the mutual inductance of a differential inductor but is not easily portable to other designs. This paper focuses on mutual noise cancelation in the LNA itself making it more versatile.

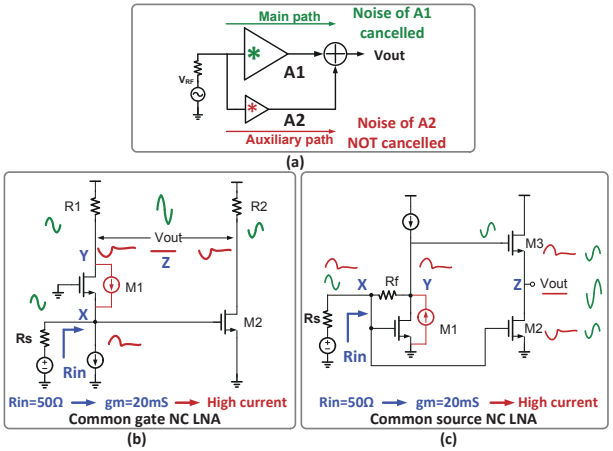

Fig. 1. Traditional common-source and common-gate noise cancelling (NC) LNAs and their shortcomings

II. Circuit Design

We propose a dual-path noise cancelling LNA which is a hybrid of the CS and the CG noise cancelling LNAs coupled together using the two secondary turns of a step-up balun as shown in Fig. 2. The CG stage acts as the auxiliary path for the CS stage and vice versa. As a result, the noise of both stages get cancelled. The input stage consists of a 1:3 balun. The secondary S1 is connected to a class AB inverter stage consisting of transistors M1a and M1b acting as a CS amplifier (A1). The secondary S2 is connected to a CG stage formed by M2 (A2).

CS noise cancellation: As shown in Fig. 3(a), for CS cancellation M1a/M1b forms the main path and M2 forms the auxiliary path. The noise current of M1a and M1b flows through Rf and Rs1, where Rs1 is the impedance transformed input source resistance at S1. This results in two in-phase instantaneous noise voltages at Y1 and X1. The noise voltage at X1 is inverted at Z by M2. Note, M2 is a gm-boosted stage as the two secondary terminals of the balun i.e., S1 and S2 provide opposite signal phases. The noise voltage at Y1 appears in phase at Z due to the source follower formed by M3. Since the noise voltages from the main and auxiliary paths are out of phase, they get cancelled at the output Z (Fig 3(a)).

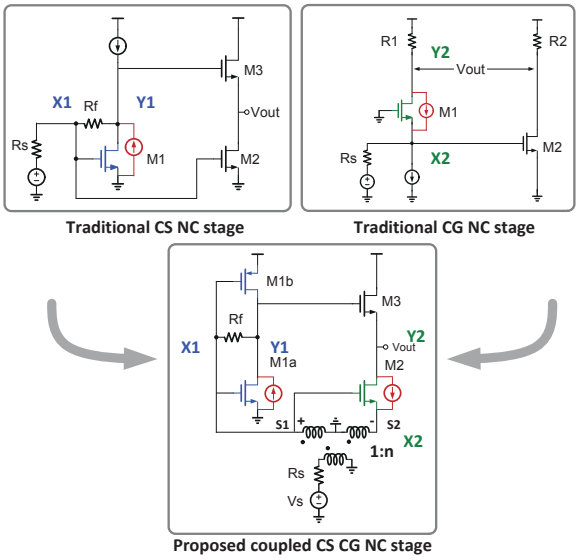

Fig. 2. Coupling of traditional CS and CG noise cancelling (NC) LNA stages to form a coupled CS-CG NC LNA

CG noise cancellation: For CG noise cancelling (Fig 3(b)) M2 forms the main path and M1a/M1b form the auxiliary path. The noise current of M2 flows through Rs2, which is the impedance transformed input source resistance seen at S2. This current is also drawn through M3. As a result, the noise voltages at node X2 and Z are inversely correlated. The noise voltage at the input X2 undergoes phase inversion at node X1 because S1 and S2 form an inverting transformer. This noise at X1 is inverted by M1a/M1b and propagated by the source follower (M3) to cancel the primary path noise. On the other hand, the signal voltages from the two paths are in phase at the output Z and get added. The signal voltage is inverted at Z after passing through the path formed by S1, the inverter and the source follower. The signal voltage is also inverted at Z after passing through the path formed by S2, and the CG stage. The mutual coupling between the two stages using the mutual inductance of S1 and S2 of the balun facilitates dual-path noise cancellation. In addition to noise, the nonlinearity of the input transistors M1a/M1b and M2 are also cancelled. This is because, similar to noise, the nonlinearity in the drain current due to gm / gds can be modeled as dependent current sources between the drain and the source [4].

Zin: The 1:3 balun transforms the source resistance Rs=50 ohm to 450 ohm reducing the required effective gm for matching by 9X. The simulated insertion loss of the balun is 1.4dB and coupling coefficient (k) between two secondaries is 0.83. The voltage gain provided by the 1:3 balun would normally have hurt the linearity by $\approx$ 9.5dB; however, the nonlinearity cancellation inherent

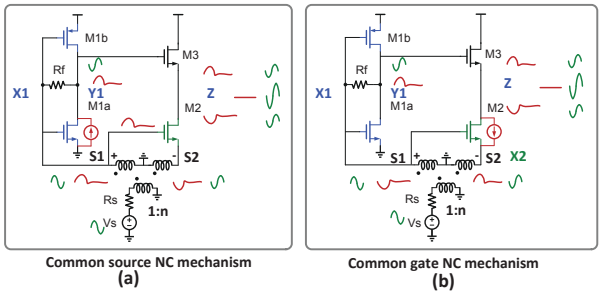

Fig. 3. Noise cancellation mechanism in proposed LNA

to these cancellation techniques partially makes up for it. The CS stage is a current-reuse class AB amplifier which achieves 2X the gm for the same current. The two secondary terminals S1 and S2 that are connected to the gate and source of M2 acts as an inverting transformer and boosts the gm by 2X for the same current. Therefore, the "effective gm" requirement for M2 is reduced by 18X. The secondary impedances seen by the left-hand side (S1) and the right-hand side (S2) of the balun are made equal in the balanced condition, i.e., $2 \cdot gm_2 = gm_1 = gm_{1a} + gm_{1b}$ such that $Zin = 2/(9gm_1)$.

III. Signal and Noise Path Analysis

The theoretical analysis for signal addition and noise cancellation are performed under the assumption that the inductances associated with the balun terminals have been resonated out with appropriate capacitances at RF.

A. Signal Path

The signals through both feed-forward paths are in phase and get added to each other and can be expressed as follows where n is the passive voltage gain from the balun.

$$Av = Av1 + Av2 = n\left(1 - gm_1 Rf + \frac{2gm_2}{gm_3}\right) \quad (1)$$

B. Noise Path

The circuit has been designed to completely cancel the noise of M1a and M1b. Under this condition the gain requirement [5] of the auxiliary path formed by M2 is as follows where Rs_1 is the impedance transformed input source resistance at S1 and $gm_1 = gm_{1a} + gm_{1b}$.

$$Av2 = 1 + Rf/Rs_1 \quad (2)$$

Let us now focus on the noise cancellation mechanism of M2 as shown in Fig. 4. The residual noise voltage Vno of M2 at the output after cancellation can be expressed as Vno where Vn_main is the path noise of M2 appearing at the output and Vn_aux is the path noise at the output

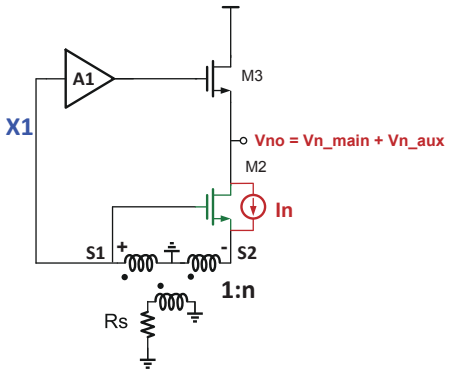

Fig. 4. Simplified model for noise cancellation of M2

due to M1a and M1b.

$$Vno = Vn\_main + Vn\_aux \quad (3)$$

$$Vn\_main = (3In/4)(1/gm_3) \quad (4)$$

$$Vn\_aux = -(InRs1/4)Av1 \quad (5)$$

Further, the requirement on gm_2 for matching can be expressed as follows where the factor 2 accounts for the gm-boosting of M2.

$$gm_2 = (1/2)Rs2 \quad (6)$$

Using these equations, the residual noise (Vno^2) of M2 at the output can be expressed as $(1/4)Vn^2$. Therefore, if the circuit is designed for 100% cancellation of A1 (M1a and M1b) then under perfect matched conditions 75% noise cancellation of A2 (M2) can be achieved.

IV. Measurement Results

The prototype was implemented in TSMC's 65nm CMOS GP technology and occupies an area of 0.42mm^2. The die-micrograph is shown in Fig. 5. For an ideal apples-to-apples comparison we would have preferred to have two designs, one with noise cancellation and one without. However, it was not possible to have "no noise cancellation" without changing the topology. So, the only fair comparison is to use the FOM for LNAs. However, as a compromise we implemented a separate design in silicon where we grounded the source of M2 (in A2) such that the dual path noise cancellation mechanism was partially suppressed and only CS cancellation mechanism was active. Fig. 6 shows the measured and simulated NF with noise cancellation and with partial noise cancellation. The measured results match quite well with simulations in both cases. The full cancellation technique improves on the partial cancellation design by reducing the NF by 2 dB. The measured NF at 2.3 GHz is 2.8 dB. The residual NF is mainly due to insertion loss of the balun, residual noise of M2 (25%) and the uncancelled noise of Rf and M3. The noise contribution of balun, Rf and M3 are respectively

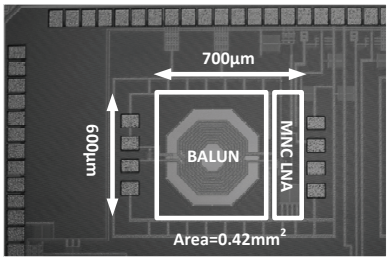

Fig. 5. Die-micrograph of the LNA

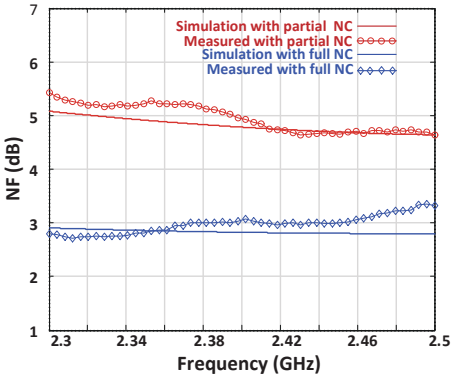

Fig. 6. Measured & simulated NFs with full and partial NC

29%, 6% and 38% in simulation. The measured gain at 2.3 GHz is 17.4 dB and the S11 is better than -13.5 dB throughout the frequency range as shown in Fig. 7. Fig. 8 shows the measured two tone test output with cancellation and with partial cancellation. In comparison to partial cancellation, the full cancellation technique improves the IIP3 of the LNA by 3.4 dB. The performance of the LNA is summarized and compared with state of the art designs in Table I. The proposed design has the lowest power of 475 µW and the highest FOM [9] of 28.8 dB which is 8.2 dB higher than the state of the art. For a fair comparison the FOM is the best mechanism and an improvement in the FOM by 8.2dB is very significant. This design has nearly 2dB better NF and 10dB better IIP3 than [10] while consuming half the power by virtue of mutual noise and nonlinearity cancellation. It has similar NF, 3.7dB lower IIP3 but 26.5X lower power than [10]. Fig. 9 shows a 3D bar chart of the various designs displaying FOM, power and noise figure. It is clearly visible that the proposed design improves on linearity, noise figure and power.

V. Conclusion

We have proposed a dual-path mutual noise cancellation technique that improves the NF, non-linearity and power consumption of fully integrated LNAs with on-chip matching suitable for sub 1V operation. In traditional techniques the noise of the auxiliary path is suppressed by burning significant power. In contrast, we have proposed

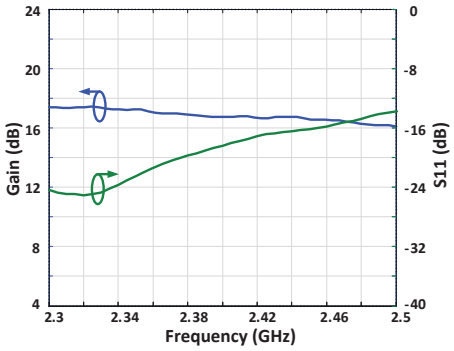

Fig. 7. Measured gain and S11 of the LNA

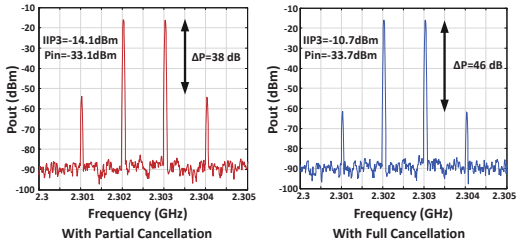

Fig. 8. Two tone output spectrum with full and partial cancellation

a dual-path noise cancelling technique which mutually cancels the noise and non-linearity of both the main (A1) and auxiliary paths (A2). This is achieved by using a balun whose secondary acts as an inverting transformer and passively couples noise from both paths by virtue of its reciprocity. The step-up balun provides voltage gain and relaxes the gm requirement for matching of the input transistors thereby reducing power. The loss in IIP3 due to passive voltage gain is compensated by nonlinearity cancellation. The circuit exploits current reuse and gm-boosting for low power. This design shows that low power noise cancellation techniques are feasible.

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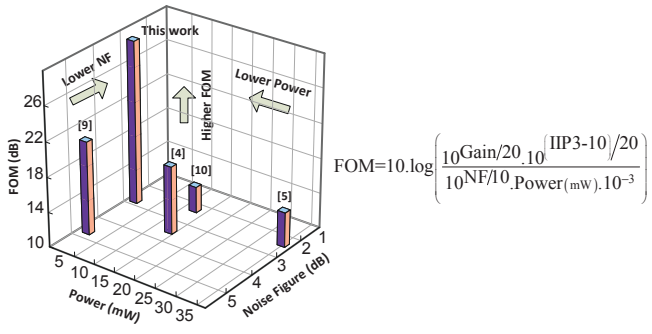

Fig. 9. FOM, power and noise figure comparison

TABLE I
PERFORMANCE COMPARISON

Ref. No.	Freq. [GHz]	NF [dB]	NC [Y/N]	Gain [dB]	IIP3 [dBm]	Power[1] [mW]	FOM [dB]
[5]	2	2.4	Y	13.7	0	35	14
[4]	5.2	3.5	Y	15.6	0	14	17.8
[11]	3	2.3	N	9.8	-7	12.6	13
[10]	2.46	4.7	N	20.2	-20	0.93	20.7
[6]	2.7	1.9	Y	72	13.5	78	
Ours	**2.4**	**2.8**	**Y**	**17.4**	**-10.7**	**0.475**	**28.8**

[1] Includes LNA core power only

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