A Jitter-Resilient Sampling Technique for High-Resolution ADCs in Wideband RF Receivers

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***Abstract*—In this paper, we analyze a novel sampling technique that addresses the clock jitter problem in high resolution wideband ADCs. The proposed sampler shapes the jitter-induced error in a manner similar to a $\Delta\Sigma$ ADC, which normally shapes the quantization noise. The clock jitter at the sampler is suppressed by the loop filter, and the impact of feedback pulse jitter is reduced through use of switched-capacitor feedback. As opposed to prior studies, we show that the a $\Delta\Sigma$ sampler suppresses the jitter error by more than 10X even at low OSR. As an example, a 2nd-order $\Delta\Sigma$ sampler increases the SJNR by 22 dB at OSR=5, corresponding to more than 3-bit improvement in the achievable SNR. Analysis indicates that increasing the loop order and/or OSR improves the amount of jitter suppression. In addition, the $\Delta\Sigma$ sampler provides the clock programmable anti-aliasing properties of an integration sampler. The analysis was validated via macro-model simulations in MATLAB and circuit simulation in Cadence.**

I. Introduction

With advances in CMOS technology, which enables robust digital signal processing, ADC performance has rapidly become the bottleneck for high speed, high resolution systems. Wideband ADC performance is ultimately limited by the clock jitter, which causes an uncertainty in the sampled value. The jitter-induced error increases linearly with the input signal frequency, imposing stringent requirements on clock jitter in high-speed high-resolution ADCs. For example, to achieve 13-bit accuracy for a 1-GHz input bandwidth, the rms jitter must be smaller than 15 fs, an exceedingly low value. Currently, the typical rms clock jitter of integrated CMOS synthesizers is in the range of 200 fs to 2 ps [1].

The integration sampler that was recently introduced is often used in software defined radios (SDRs), as both the sampling and anti-aliasing functions track each other and are clock programmable [2]. However, in comparison to traditional impulse sampling, integration sampling is more sensitive to clock jitter for $f_{in} < f_s/2$, and the resulting SJNR is almost independent of the input frequency in this range.

One approach to jitter suppression in integration samplers was introduced in [3], where the jitter error is compensated by subtracting the same error at the sampler's input via an auxiliary estimation path. This approach improves the SJNR of integration samplers, and even surpasses impulse samplers by 4 dB at Nyquist frequency, but the amount of jitter suppression decreases as OSR goes up, and at OSR$\geq$6 the SJNR is less than for impulse sampling.

Another approach was introduced in [4], where a first-order $\Delta\Sigma$ loop was used to *shape* the jitter error of an impulse sampler. The improvement in SJNR was reported to be limited to 4.75 dB and independent of OSR (OSR$\geq$6).

In this paper we re-analyze the jitter shaping properties of the $\Delta\Sigma$ sampler introduced in [4], and show that by a proper choice of loop order and loop coefficients, a low-OSR $\Delta\Sigma$ sampler can relax the jitter requirements of the sampler significantly. In addition, we shed light on the similarities between a first-order $\Delta\Sigma$ sampler and an integration sampler.

The paper is organized as follows: Section II describes jitter and its impact. In Section III, we describe and analyze the $\Delta\Sigma$ sampling technique. The proposed 2nd-order $\Delta\Sigma$ sampler is presented in Section IV. Section V concludes the paper.

II. Clock Jitter and Sampling

A. Sources of Jitter

On-chip frequency synthesizers typically use PLLs to generate a wide range of frequencies from an accurate reference source. There are multiple sources of jitter in a PLL but up to the loop bandwidth the phase noise is typically dominated by the VCO [5]. However, in wideband ADCs where the clock frequencies are in the GHz, while the loop bandwidths are in the MHz, the overall jitter is dominated by the thermal noise of the clock buffers and clock distribution circuits [6]. So, for our analysis we shall assume that the jitter is white.

B. Jitter-induced Sampling Error

For a single-tone input, the jitter-induced sampling error in an impulse sampler is given by Eqn (1) [7].

$$SJNR_{sine} = 20log_{10}\left(\frac{1}{2\pi f_{in}\sigma_j}\right) \quad (1)$$

In discrete-time (DT) $\Delta\Sigma$ ADCs, the in-band jitter noise is reduced only by the oversampling ratio (OSR), as the sampler is at the input of the loop. On the other hand, in continuous-time (CT) $\Delta\Sigma$ ADCs sampling occurs at the quantizer, hence the jitter-induced error gets shaped by the loop in the same way as quantization noise [8]. However, CT $\Delta\Sigma$ ADCs suffer from an additional source of jitter, i.e., the clock jitter in the feedback path, which changes the feedback pulse width. The error caused by feedback pulse variation depends on the feedback pulse shape as well as the noise transfer function (NTF), and in some cases it can be even more severe than the sampling error in regular ADCs [9]. This problem in CT $\Delta\Sigma$ ADCs has been addressed by using a switched-capacitor (SC) feedback mechanism [10]. The advantage of the SC pulse comes from the rapid decrease in the area under the pulse

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which reduces the voltage error caused by the jitter, as shown in Eqn (2), where τ is the time constant of the feedback.

$$\sigma^2_{e_{j,SC}} = \sigma^2_{e_{j,NRZ}} \left(\frac{T_s}{2\tau}\right)^2 e^{\frac{-T_s}{\tau}} \tag{2}$$

It is important to note that although SC feedback reduces the jitter error, it does not necessarily enhance the jitter sensitivity of CT $\Delta\Sigma$ ADCs compared to other ADCs. Besides, high-resolution CT $\Delta\Sigma$ ADCs often require high OSRs, making them less desirable for high-frequency applications. In contrast, we will show that a $\Delta\Sigma$ sampler has good performance even with low OSRs.

III. $\Delta\Sigma$ Sampling

A $\Delta\Sigma$ sampler is essentially a continuous-time $\Delta\Sigma$ modulator without a quantizer and DAC. This is illustrated conceptually in Fig 1. Since in a multi-bit $\Delta\Sigma$ modulator the transfer function from the input of the quantizer to the output of the DAC is ideally 1, removing these blocks does not change the input-output characteristic. The only difference is that there is no quantization noise in the output of the $\Delta\Sigma$ sampler. The modulatro is followed by an analog FIR filter and decimator.

A. Sampling Jitter

We shall continue the discussion based on the 1st-order structure depicted in Fig. 2a, where we first assume a *continuous* feedback pulse, i.e., an NRZ feedback for simplicity. The impact of feedback pulse jitter will be discussed later.

First, note that V_{out} is the sampled and held value of V_1 (the integrator output), and we have

$$V_{out_j}(s) = H_{SH} \sum_{n=0}^{\infty} e^{-snT} V_1\left[nT + \Delta T_j(n)\right] \tag{3}$$

where $H_{SH} = \frac{1-e^{-sT}}{sT}$.

The jitter induced sampling error can now be calculated using Eqn (3) and the ideal value of V_1.

$$\begin{aligned} E_{j,out}(s) &= H_{SH} \sum_{n=0}^{\infty} e^{-snT} \left(V_1\left[nT + \Delta T_j(n)\right] - V_1\left[nT\right]\right) \\ &= H_{SH}\left(sV_1(s) * J(s)\right) \end{aligned} \tag{4}$$

where J(s) is the spectrum of the clock jitter. In the case where jitter is white, $J(s) = \sigma_j \delta(s)$, thus

$$E_{j,out}(s) = \frac{1-e^{-sT}}{sT} sV_1(s)\sigma_j \tag{5}$$

Therefore, the jitter-induced noise can be modeled as an additive noise source $E_j(s) = sV_1(s)\sigma_j$ before the sampler. We can now find the input-output characteristic of the $\Delta\Sigma$ sampler based on the model in Fig. 2b.

$$\begin{aligned} V_{outj}(s) \approx & \frac{H_{SH}(\frac{f_s}{s})}{1 + H_{SH} a_1(\frac{f_s}{s})} V_{in}(s) \\ & + \frac{H_{SH}(\frac{f_s}{s}) s\sigma_j}{\left(1 + H_{SH} a_1(\frac{f_s}{s})\right)^2} V_{in}(s) \end{aligned} \tag{6}$$

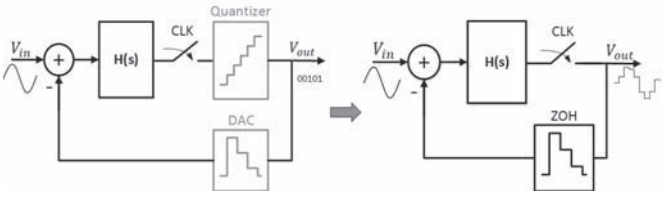

Fig. 1: Conceptual diagram for a $\Delta\Sigma$ converter and a $\Delta\Sigma$ sampler.

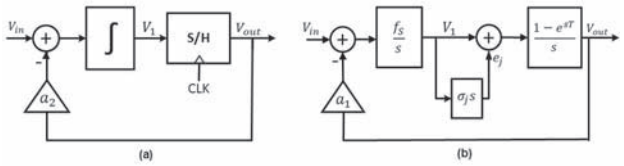

Fig. 2: Block diagram and equivalent model of the 1st-order $\Delta\Sigma$ sampler with NRZ feedback.

The approximation holds for $s\sigma_j \ll 1$.

The SJNR for a single-tone input at f_0 can be calculated by taking the ratio of the signal power to integrated jitter noise, as shown in Eqn (7):

$$SJNR = \frac{\left|\frac{H_{SH}(\frac{f_s}{2\pi f_0})}{1+H_{SH}a_1(\frac{f_s}{2\pi f_0})}\right|^2}{2 \cdot T_s \cdot f_s^2 \cdot \sigma_j^2 \int_0^{f_0} \left|\frac{H_{SH}}{\left(1+H_{SH}a_1(\frac{f_s}{s})\right)^2}\right|^2 df} \tag{7}$$

Eqn (7) is plotted in Fig. 3 for a_1=1, f_0=500 MHz, and σ_j=1ps. The figure shows that the SJNR of the $\Delta\Sigma$ sampler ($\Delta\Sigma$) is always higher than simple oversampling (Regular), and it increases 9 dB for every doubling of OSR. This is in contrast to what was concluded in [4]. In the next section, we show that the discrepancy is due to the feedback mechanism.

B. Feedback Pulse Jitter

So far, we have only considered the sampling jitter in the forward path, but the $\Delta\Sigma$ sampler is also susceptible to feedback pulse jitter. The error caused by feedback pulse variations in a CT $\Delta\Sigma$ ADC with NRZ feedback is given by Eqn (8), where N is the number of bits in the quantizer, and σ_Q is the area under the noise transfer function [9].

$$\sigma^2_{e_j,ADC} = \frac{(2\pi f_{in}\sigma_j)^2}{OSR} + \frac{\sigma_Q^2 f_s^2 \sigma_j^2}{3(2^N-1)^2} \tag{8}$$

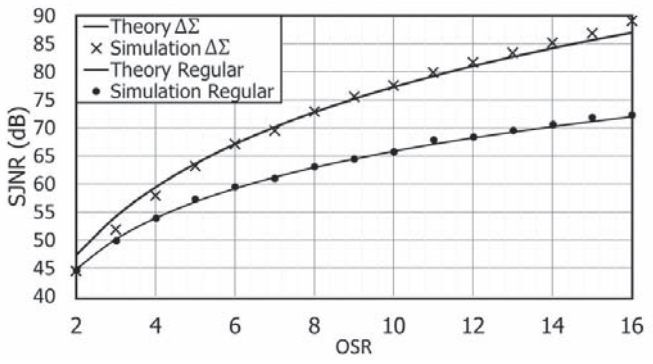

Fig. 3: The SJNR of the 1st-order $\Delta\Sigma$ sampler with NRZ feedback in comparison with simple oversampling.

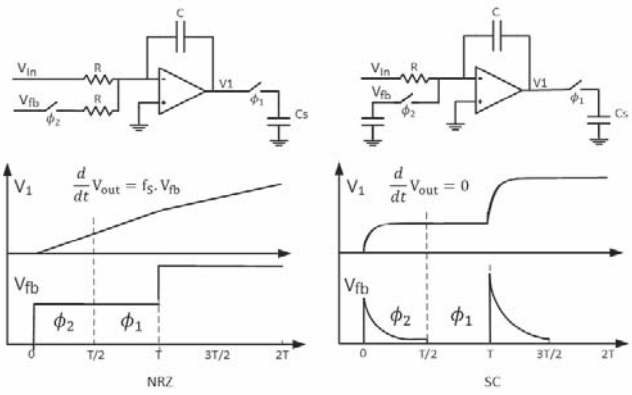

Fig. 4: Comparison of SC and NRZ feedback in a $\Delta\Sigma$ sampler.

In Eqn (8), the first term shows the jitter error due to input signal, and the second term accounts for the NTF-dependence of the error. In order to find the error in a $\Delta\Sigma$ sampler, we let N$\rightarrow\infty$. This results in Eqn (9) which is equal to the sampling error in a regular oversampling sampler.

$$\sigma^2_{e_j,sampler} = \frac{(2\pi f_{in}\sigma_j)^2}{OSR} \tag{9}$$

This highlights an important difference between the $\Delta\Sigma$ sampler and a CT ADC. In contrast to a $\Delta\Sigma$ ADC, there is no quantization noise in the output of the $\Delta\Sigma$ sampler, and the feedback jitter error does not depend on the NTF. Therefore, the jitter error in the $\Delta\Sigma$ sampler is lower than in a $\Delta\Sigma$ ADC, and there is no trade-off between noise shaping and feedback pulse jitter. Nonetheless, as indicated by Eqn (9), the feedback error is still large and must be suppressed.

The pulse width jitter can be suppressed by using SC feedback. However, changing the feedback pulse shape also affects the sampling error. As shown in Fig. 4, an NRZ pulse is constant throughout the clock period, which causes the integrator's output to change at the sampling instance. In contrast, a SC pulse is transferred during ϕ_2, thus it appears only as a DC shift in the integrator's output at the sampling instance. Note, the sampling error is only affected by the slope of V_1 and not a DC shift. Therefore, as shown in Eqn (10b), the sampling error with NRZ feedback is determined by the difference between the input and feedback signals, but it only depends on the input signal when SC feedback is used.

$$e_{j,NRZ} = (V_{in}[nT] - V_{fb}[nT]) \cdot f_s \cdot \Delta T_j[nT] \tag{10a}$$
$$e_{j,SC} = V_{in}[nT] \cdot f_s \cdot \Delta T_j[nT] \tag{10b}$$

The SJNR of the $\Delta\Sigma$ sampler with SC feedback can be calculated using the modified model in Fig. 5.

$$SJNR = \frac{\left|\frac{H_{SH}(\frac{f_s}{2\pi f_0})}{1+H_{SH}a_1(\frac{f_s}{2\pi f_0})}\right|^2}{2\cdot T_s \cdot f_s^2 \cdot \sigma_j^2 \int_0^{f_0} |H_{SH}|^2 \, df} \tag{11}$$

We have plotted the SJNR advantage of the $\Delta\Sigma$ sampler in comparison to simple oversampling in Fig.6. The results indicate that with SC feedback, the advantage of the 1st-order $\Delta\Sigma$ sampler is less than 5 dB, and it does not improve with OSR, as was concluded in [4].

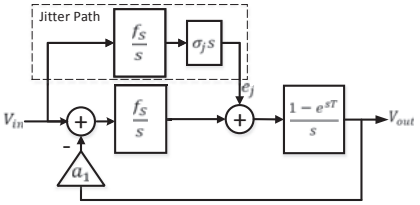

Fig. 5: Equivalent model of the 1st-order $\Delta\Sigma$ sampler with SC feedback.

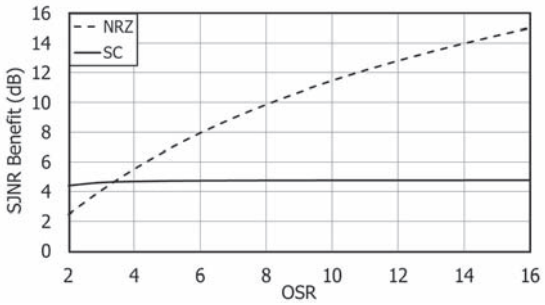

Fig. 6: SJNR benefit of the 1st-order $\Delta\Sigma$ sampler with NRZ and SC feedback.

IV. The Proposed 2nd-Order $\Delta\Sigma$ Sampler

In order to retain the noise shaping properties of the $\Delta\Sigma$ loop while still using SC feedback, we propose a 2nd-order $\Delta\Sigma$ sampler. The 1st derivative dependence of the jitter error cancels one order of the $\Delta\Sigma$ loop. By adding a second integrator, the feedback pulse at the output of the first integrator causes a ramp at the output of the 2nd integrator, similar to the case of NRZ feedback in the 1st-order sampler.

Fig. 7 shows the equivalent model of the sampler. Note that, with an SC feedback mechanism, the feedback to the second integrator does not affect the sampling jitter, thus it is removed from the jitter path. We can now find the signal and noise transfer functions from Eqn (12).

$$\begin{aligned} V_{outj}(s) \approx & \frac{H_{SH}(\frac{f_s}{s})^2}{1+H_{SH}(a_1(\frac{f_s}{s})^2 + a_2(\frac{f_s}{s}))} V_{in}(s) \\ & + \frac{H_{SH}(\frac{f_s}{s})^2}{\left(1+H_{SH}(a_1(\frac{f_s}{s})^2 + a_2(\frac{f_s}{s}))\right)^2} E_{j2}(s) \end{aligned} \tag{12}$$

where $E_{j2}(s) = \left(1 + H_{SH}a_2(\frac{f_s}{s})\right) s\sigma_j$.

In order to verify the analysis, the second-order $\Delta\Sigma$ sampler was simulated in Simulink and in Cadence. Fig. 8 shows the Simulink model of the sampler. In the forward path, the sampling error is generated similar to Fig. 7, and the feedback pulse jitter is modeled for NRZ-SC feedback structure, where the error depends on the pulse *period*, rather than pulse edge.

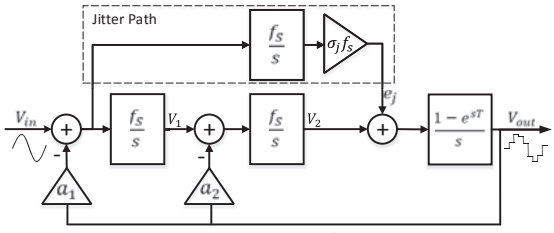

Fig. 7: Equivalent model for the 2nd-order $\Delta\Sigma$ sampler and sampling jitter.

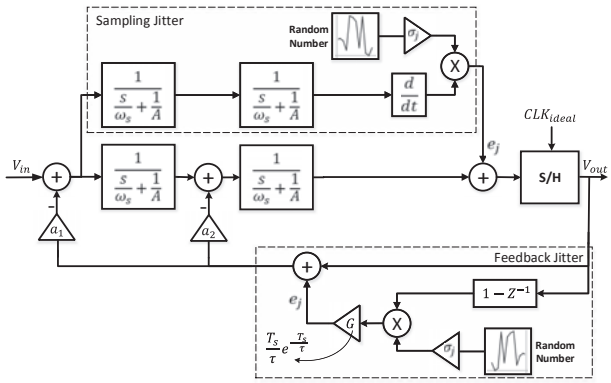

Fig. 8: Simulink model for the sampler with sampling and feedback jitter.

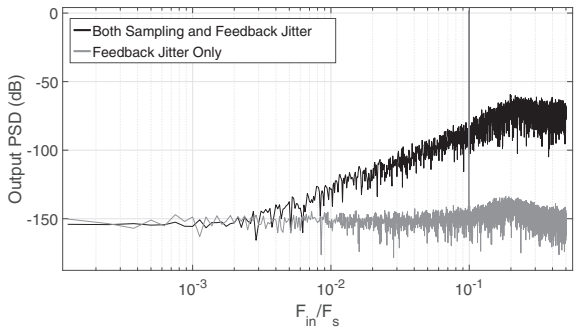

Fig. 9: 5000-point output FFT of the simulated $\Delta\Sigma$ sampler for OSR=5.

In Cadence, the sampler was simulated in the time-domain using using ideal integrators and switches. The jittery clock was generated in MATLAB and exported to Cadence. In all simulations, a_2=1, σ_j=1 ps, and f_{in}=500 MHz. The output spectrum of the sampler in Cadence with OSR=5 is shown in Fig. 9. It can be clearly seen that the sampling jitter is shaped by the $\Delta\Sigma$ loop, whereas the feedback jitter appears as a flat noise level in the spectrum.

As in $\Delta\Sigma$ ADCs, increasing a_1 improves the jitter-shaping at the expense of out-of-band peaking. At OSR=5, the SJNR is 67 dB with a_1=1 and 72.6 dB with a_1=2, whereas the SJNR of simple oversampling is limited to 50 dB, and oversampling only improves the SJNR by 7 dB. The simulated and calculated SJNR with a_1=1 are compared for different oversampling ratios in Fig. 10. There is good agreement between theoretical analysis the simulations in Cadence. The results show that, unlike a 1st-order sampler, the SJNR of the 2nd-order $\Delta\Sigma$ sampler improves with OSR.

In summary, we would like to highlight the following points:

- A $\Delta\Sigma$ sampler shapes the jitter-induced error in the same way that a CT $\Delta\Sigma$ ADC shapes the quantization noise.
- Unlike quantization noise, the jitter-induced sampling error depends on the derivative of the last integrator's output. Therefore, any modifications in the feedback pulse affects the jitter-induced sampling error.
- SC feedback reduces the feedback jitter error, but it impairs the jitter-shaping properties of the $\Delta\Sigma$ sampler. In fact, a L^{th}-order sampler with SC feedback provides $(L-1)^{th}$-order noise shaping. This is why a 1st-order $\Delta\Sigma$ sampler with SC feedback has limited benefit.

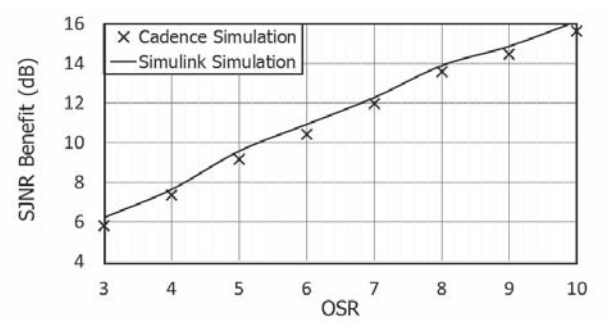

Fig. 10: The additional SJNR benefit of the 2nd-order $\Delta\Sigma$ sampler compared to a regular oversampling sampler.

- The SJNR of a 2nd-order $\Delta\Sigma$ sampler increases 9 dB with every doubling of OSR (i.e., 1.5bit per octave).
- The $\Delta\Sigma$ sampler retains properties of an integration sampler and provides programmable anti-aliasing filtering.

V. Conclusions

In this paper, we analyzed the $\Delta\Sigma$ sampling technique and show that it is possible to effectively suppress the jitter-induced error by using a low-OSR 2nd-order $\Delta\Sigma$ sampler. A $\Delta\Sigma$ sampler, inherits the anti-aliasing properties of an integration sampler. At an OSR=5, the effective jitter at the output of the $\Delta\Sigma$ sampler with 100fs rms clock jitter is less than 15fs, enabling a 1-Gsps ADC to achieve more than 13-bit accuracy. The analytical framework developed here was verified via simulations in Matlab and in the time-domain in Cadence.

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